ISSN 0002-306X. Proc. of the RA NAS and NPUA Ser. of tech. sc. 2017. V. LXX, N 2.

UDC 681.3.07 RADIOELECTRONICS

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THE QUALITY CHARACTERISTICS ESTIMATION METHOD FOR THE NANOSCALE RTL COMPILERS

For STAR Memory System (SMS) network, one of the most important design constraints is area and power consumption. This paper presents the quality characteristics estimation methodology of SMS network infrastructure for the case of FinFET technology. We present the quality characteristics comparative evaluation for the cases of FinFET and MOSFET technologies.

Keywords: area, power consumption, FinFET, RTL compilers, estimation.

Introduction. Nowadays, system-on-chip (SoC) consists of several embedded IP cores. The number of embedded memories in SoC increased dramatically by having enormous influence on the manufacturing yield of entire SoC. To improve the yield of embedded memories test and repair methodology is needed [1]. Built-in-Self-Test solution is preferable for embedded memories test and repair, because it does not require expensive Automatic Test Equipment (ATE) [2]. Synopsys DesignWare Self-Test and Repair (STAR) Memory System is a complete, cost-effective solution for test and repair of repairable and non-repairable embedded memories. Test and repair infrastructure of SMS network is generated via hierarchy of Register Transfer Level (RTL) compilers [3].

Gate count and power consumption have become key design constraints in STAR Memory System (SMS) network design. Traditional gate count and power consumption estimation methodologies which are based on synthesis tools are inefficient for the case of SMS network [4]. In papers [5-7], we presented quick gate count and power consumption estimation methodologies for SMS network, that are based on linear and polynomial interpolation.

For a long while, in SoC embedded memories were used built with conventional planar MOSFET technology. As embedded memories will continue to consume a large part of the SoC area, the scaling of embedded memories density must continue with the scaling trends of logic. It is now almost impossible to build embedded memories with scaling down parameters by using the traditional MOSFET technology without negative consequences. Therefore, FinFET - based memories have been developed to improve embedded memories scalability. FinFET is one of the most promising device technologies for extending Moor's law to 20 *nm* and beyond [8]. SMS network must be able to test and repair embedded memories built with the FinFET technology.

Technological changes lead to the need to redesign RTL compilers. Consequently, there will be timing, power, area and other characteristics' changes in the infrastructures of the SMS network. Hence, the quality characteristics of RTL compilers must be reconsidered for the case of the FinFET technology.

The paper [9] authors had presented power and area (gate count) analysis of 45 *nm* and 15 *nm* technologies. For that purpose, the RTL design of IEEE 754 Single Precision Floating-Point Unit was analyzed for the case of the 45 *nm* and 15 *nm* technologies. The experimental results had proven that 15 *nm* technology suggests 4 times improvement in power consumption and about 30% improvement in the area compared with the 45 *nm* technology. Gate count numbers remain almost the same for the 45 *nm* and 15 *nm* technologies.

According to paper [9], there are significant changes in RTL design characteristics when moving from the 45 *nm* technology to the 15 *nm* one. As RTL compilers also generate RTL descriptions, and they are regular and parameterized, in this paper we would like to expose how quality characteristics of the SMS network will change when migrating from MOSFET to FinFET.

1. Planar vs FinFET technology. To understand FinFET architecture we should compare it with the architecture of a planar transistor [10].

MOSFET transistors have been the core of SoC for several decades, and during this time the size of transistors decreased. MOSFET has a single gate that controls the conductive channel. The gate in a planar transistor has not a good electric field control, and there is leakage current between the source and the drain even when the gate is off. Hence, planar transistors suffer from an undesirable short-channel effect that increases the power required by SoC [10].

To solve the short-channel effect problem, different transistor architectures were proposed, among them the FinFET technology is considered one of the best approaches [11].

In FinFET, the transistor conducting channel is wrapped by a thin silicon "fin" that forms the body of the transistor. The effective channel length of the transistor is defined by the thickness of the fin. The gate fully depletes the channel of carriers. This gate structure controls the channel in a better way, reduces short-channel effects and leakage current. The most important parameters of FinFET are its width, height and channel length [10].

The move from the planar to the FinFET technology causes changes in the performance, area, power, cost and yield [12].

Recent research shows that it is possible to gain 30% performance improvement when moving from a 28 *nm* planar to a 16 *nm* or a 14 *nm* FinFET process [12].

There is a significant improvement in power consumption. The leakage power is two times smaller compared with that of the planar technology. Dynamic

power has also come down along with the nominal voltage, however dynamic power is now the bottleneck to achieving lower power [12]. According to paper [9], there is 4 times power improvement when moving from the 45 *nm* technology to the 15 *nm* technology.

The area savings also are essential. There is around 35% to 40% savings when moving from the 28 *nm* planar to the 16 *nm* FinFET technology [12]. According to paper [9] there is about 30% area saving when moving from the 45 *nm* technology to the 15 *nm* technology.

The manufacturing cost is higher compared with the planar technology because of manufacturing complexity related to the FinFET technology [12].

Failure mechanisms in FinFET's are different from those of planar transistors. Therefore, the BIST algorithms for the planar technology will not be effective for FinFETs. To catch FinFET-specific faults new algorithms for memory based solution were developed in the SMS network. These algorithms help to improve overall yield [10].

2. Methodology. In papers [5-7], we presented a quick gate count and power consumption estimation methodology of the SMS network infrastructure for the case of the MOSFET technology.

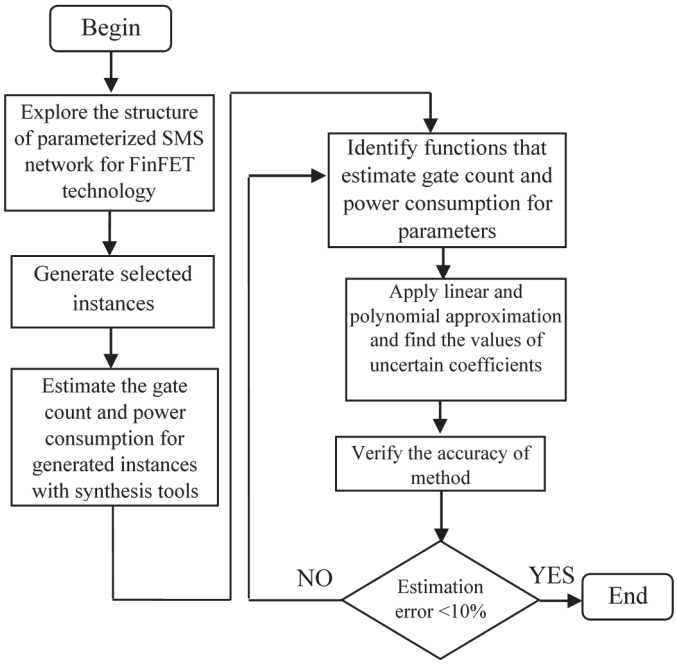

Fig. 1. The Block diagram of the gate count and power consumption estimation methodology of the SMS network infrastructure for the case of the FinFET technology

According to the information gained after research, the hierarchy of RTL compilers generates parameterized and regular descriptions. These parameters bring structural or functional changes of schemes. Hence, the quality characteristics of the SMS network design are changed. There are functional dependences between the quality characteristics of schemes generated by RTL compilers and input parameters. The experimental results show that the behavior of the SMS network parameters is linear or polynomial. The analytical representations of functions are unknown. Therefore, we developed the quick gate count and power consumption estimation methodologies which are based on approximation.

Our recent research shows that the behavior of the SMS network parameters for the FinFET technology is also linear or polynomial, but there is sufficient reduction in the area and power consumption data. Consequently, the analytical representations of functions for the FinFET technology differ from that of the MOSFET's.

Fig. 1 shows the block diagram of the gate count and power consumption estimation methodology of the SMS network for the FinFET technology.

To estimate the gate count and power consumption of the SMS network for the FinFET technology, we implement the following steps:

- To explore the structure of the parameterized SMS network for the FinFET technology, the parameters that cause drastic variations in the gate count and power consumption of the SMS network are figured out.
- To generate selected instances for each selected parameter, we choose and generate a number of instances.
- To estimate the gate count and power consumption for generated instances with synthesis tools, we estimate the gate count and power consumption data for selected instances of each parameter with synthesis tools.
- To identify the functions that estimate the gate count and power consumption for parameters, the behavior of parameters is considered according to the real gate count and power consumption estimation data.
- To apply linear and polynomial approximation and find the values of uncertain coefficients, we apply linear or polynomial interpolation to get formulae that describe the behavior of parameters.
- To verify the accuracy of the method, we compare the real and estimated gate count, power consumption data. The maximum achieved estimation error must be 10%.

3. SMS network infrastructure for the case of the FinFET technology. SMS network provides automated test and repair strategy for embedded memories within SoC. SMS has hierarchical structure as shown in Figure 2. It

contains several hardware components, including: STAR Processors, Wrappers, Server, Fuse Box, TAP controller and memories [1] (Fig. 2 [7]).

SMS generates wrappers around each memory. Wrappers work with Processors to test and repair embedded memories. A single wrapper is able to work with several memories [1].

A group of Wrappers connects to a Processor. A single Processor can test and repair several memory instances. The Processor performs all test and repair functions by using memory specific test algorithms. It interacts with memory, finds out the defects, and if the memory is repairable, generates the repair signature.

The repair signature is then transferred to Laser Fuse box, which blows laser fuses corresponding to the defective memories [1].

The processor in turn connects to the Server which generates a top level design of the network and passes the SMS network signals to the JTAG port through the TAP controller.

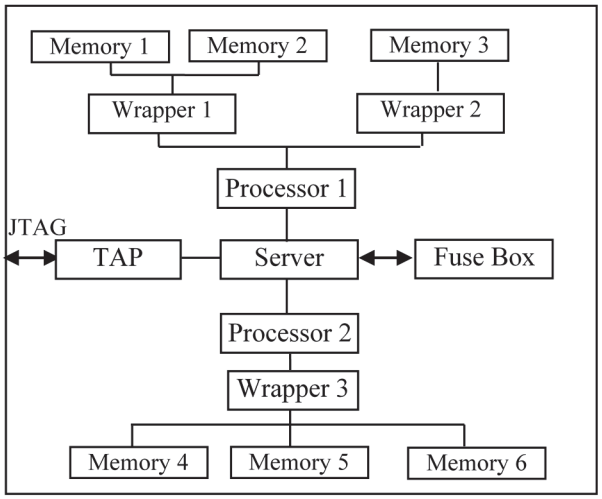

Fig. 2. A SMS network infrastructure example

To test and repair different defects, there are fault detection and repair algorithms. As there is an enormous difference in the structures of the FinFET and MOSFET technologies, the set of defects for FinFET differs from the MOSFETs. In paper [8], the authors have mentioned that the methodology was developed for an automated test and repair of defects in the FinFET - based memories with different algorithms. These algorithms are embedded in the hierarchy of SMS network.

4. Experimental Results. Experimental results show that the behavior of the SMS network's parameters for the case of the FinFET technology is linear or polynomial, but the area and power consumption data sufficiently differ from those of the MOSFET technology. The gate count data are almost the same for the FinFET and MOSFET technologies.

We figure out those parameters that cause drastic variations in the gate count and power consumption data of the SMS network. Several values of the parameters were chosen and used as an interpolation points. The real gate count and power consumption data have been obtained through logic synthesis. We use 28 *nm* and 16 *nm* target library for logic synthesis. By applying linear or polynomial interpolation, we have got formulae that describe the behavior of the quality characteristics of the SMS network for the cases of the MOSFET and FinFET technologies.

Experimental results show that there is a 36% area improvement of the SMS network when moving from the MOSFET to the FinFET technology.

Fig. 3 presents the gate count comparative data of Wrapper Compiler for the cases of 28 *nm* (MOSFET) and 16 *nm* (FinFET) technologies, where NB is the Number of Bits of appropriate memory.

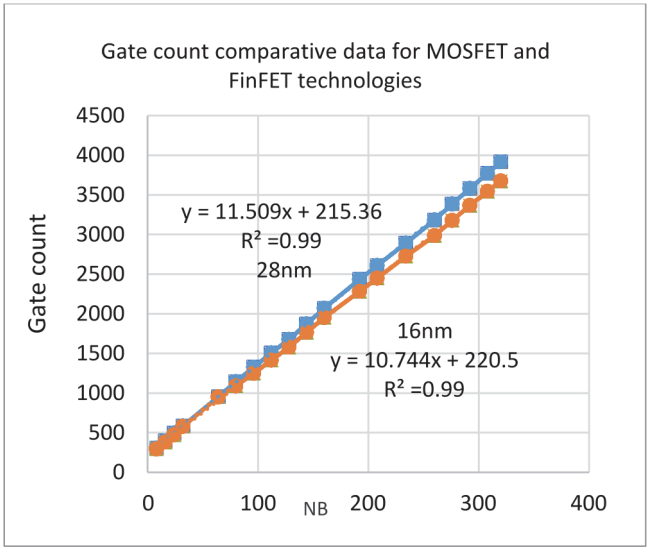

Fig. 3. The gate count comparative data for the MOSFET and FinFET technologies

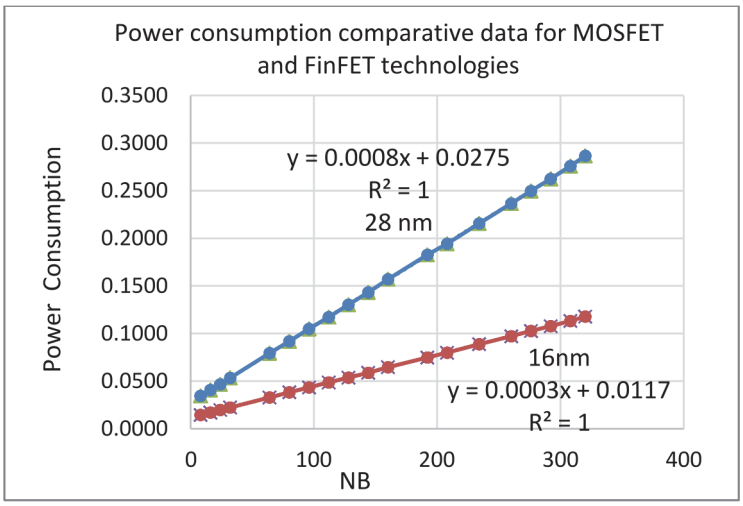

Fig. 4. The power consumption comparative data for the MOSFET and FinFET technologies

It is obvious from the added graphs that the gate count behavior changes for the MOSFET and FinFET technologies are almost the same, and the values of uncertain coefficients hardly differ from each other. Therefore, there is no need to estimate the gate count of the SMS network for the FinFET technology separately. The behavior of the gate count for the case of the FinFET technology can be described with the same formulae as in the MOSFET technology.

Fig. 4 presents power consumption comparative data for the case of 28 *nm* (MOSFET) and 16 *nm* (FinFET) technologies for Wrapper Compiler. The graph shows that there is a huge difference of the power consumption data for the case of the MOSFET and FinFET technologies.

According to the experimental results, there is 50% power improvement when moving from MOSFET to FinFET. Hence, power consumption must be estimated separately for the FinFET technology.

Conclusion. The behavior of the SMS network parameters was exposed for the case of the FinFET technology. Quick quality characteristics estimation methodology was developed for the FinFET - based SMS network. Experimental results proved that there are 36% area and 50% power consumption improvements of the SMS network when migrating from MOSFET to FinFET. The gate count data remain almost the same for the MOSFET and FinFET technologies.

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National Polytechnic University of Armenia. The material is received on 15.03.2017.

Լ.Ա. ՄԱՐՏԻՐՈՍՅԱՆ

ՆԱՆՈՉԱՓԱՅԻՆ RTL ԿՈՄՊԻԼՅԱՏՈՐՆԵՐԻ ՈՐԱԿԱԿԱՆ ԲՆՈՒԹԱԳՐԵՐԻ ԳՆԱՀԱՏՄԱՆ ՄԵԹՈԴ

STAR հիշողության համակարգերի ցանցի համար նախագծային սահմանափակումներն են մակերեսը և հզորության սպառումը: Ներկայացվել է առավել կարևոր որակական բնութագրերի գնահատման մեթոդը՝ STAR հիշողության համակարգերի ցանցի համար FinFET տեխնոլոգիայի դեպքում, ինչպես և որակի բնութագրերի համեմատական գնահատականը՝ FinFET և MOSFET տեխնոլոգիաների դեպքում:

Առանցքային բառեր. մակերես, հզորության սպառում, FinFET, RTL կոմպիլյատորներ, գնահատում:

Л.А. МАРТИРОСЯН

МЕТОД ОЦЕНКИ КАЧЕСТВЕННЫХ ХАРАКТЕРИСТИК НАНОРАЗМЕРНЫХ RTL КОМПИЛЯТОРОВ

Для сети SMS одними из наиболее важных конструктивных ограничений являются площадь и энергопотребление. Представлена методика оценки качественных характеристик SMS сети для технологий FinFET. Дана сравнительная оценка качественных характеристик при FinFET и MOSFET технологиях.

Ключевые слова: площадь, потребляемая мощность, FinFET, RTL компиляторы, оценка.