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A RELIABLE PMOS-BASED CHARGE PUMP ARCHITECTURE

The design of the charge pump circuit with two different PMOS and NMOS architectures has been done, so that the output will receive 1.5 times the voltage of the power supply. The surfaces, speed and reliability of the two circuits were evaluated. In the proposed PMOS structure, two key transistors have no reliability problem as opposed to the NMOS structure, which is due to the difference of the transistors' bulk-source terminal voltages. The variation of the output signal of the proposed PMOS scheme is less than in the NMOS scheme but the area is 1,26 times larger.

Keywords: Charge pump, Dickson's charge pump, low power design, DC/DC converter, aging.

Introduction. In modern integrated circuits technological processes continue to shrink the channel length of transistor' up to 5nm. It gives an opportunity to provide more functionality by increasing the device density in the unit area of die.

Due to low power consumption requirement the supply voltage values also have decreased. Another problem which should be solved during the design process of integrated circuits is the transistors' protection from over-voltages and possible stress situations, which could cause degradation of the threshold voltage during operation.

There are devices which require operation voltages higher than the nominal supply voltage (for example low power flash memories). So, circuits which could offer voltage higher than supply voltage are needed. For this type of operations charge pumps are widely used. A charge pump can provide voltage higher than the supply voltage, acting as a DC/DC voltage converter. The output voltage value of the charge pump could be a number of times higher than the nominal supply voltage. The key devices in the charge pump's structure are capacitors which are used as energy collection storages.

Dickson's charge pump (Fig.1) is one of the well-known charge pump architectures, which is used in modern integrated circuits. The circuit works with two differential clock signals, whose amplitude is equal to the nominal supply voltage (V_{supply}) [1]. The NMOS diode-connected transistors in Dickson's charge pump architecture are used as switches for every stage of the circuit. The current flows through the NMOS transistors charging the output

capacitors for each stage, which are connected parallelly. It gives an opportunity to have a higher DC voltage after each stage.

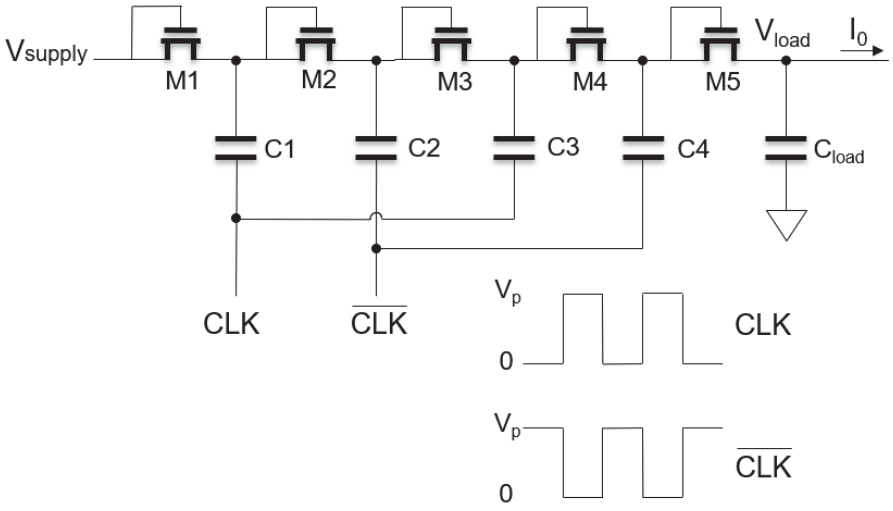

Fig.1. Dickson's charge pump architecture

The circuit uses the Vsupply as an input voltage, and the output of each stage differs from the previous one by constant Vd voltage, which, in the ideal case, is equal to the Vsupply. By using equation (1), the number of the required stages (N) could be calculated [1]:

$$\mathrm{N} = \frac{V_{load} - V_{in}}{V_d} \ . \qquad (1)$$

The main disadvantage of Dickson's charge pump is the body effect of NMOS transistors which causes gain degradation for higher N values.

The proposed Charge Pump. The schematic view of the proposed charge pump is shown in Fig 2. The architecture is based on NFET transistor with a single supply. The charge pump works with two differential clock signals to control the settling time of the circuit. The M1 and M2 NFET transistors are in positive feedback, which decreases the charging time of the capacitors.

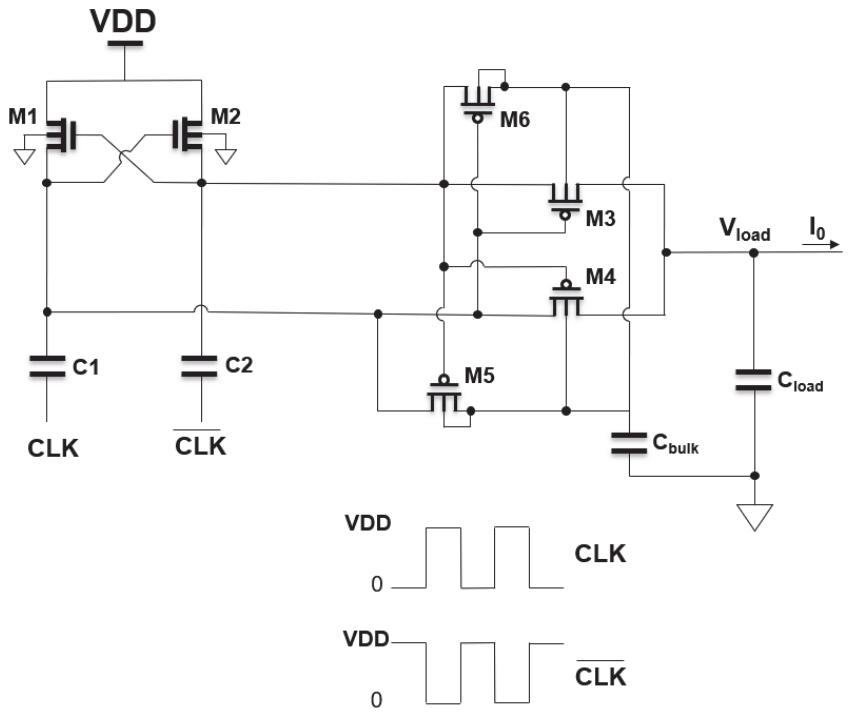

Fig.2. The proposed charge pump with a NFET architecture

The M3 and M4 transistors are used as pass devices to formulate the output voltage. Charging the Cbulk capacitor with M5 and M6 transistors helps to cancel the bulk effect for the M3 and M4 devices. The circuit provides 1.5 times higher voltage than the supply, when the load is enabled.

The charge pump circuit could be used in analogue architectures to supply voltage regulators, voltage-controlled oscillators (VCO), etc. The main disadvantage of such a structure is the gate-bulk voltage value of the M1 and M2 transistors. During operation, when the load is disabled, for ideal case the output voltage is equal to 2VDD and the M1 and M2 transistors work under stress conditions. This can affect the threshold voltage and the drain source current of transistors, which will lead to the output voltage value degradation.

By using high voltage input transistors, it is possible to solve the gate-bulk voltage issue, and transistors will operate without stress, as the allowed gate-bulk voltage for high voltage transistors is higher than 2VDD. But the disadvantage of this structure is that it is not reasonable to use high voltage input transistors in VDD domain [2]. Simulation results show that the output in such a structure will be degraded (Fig. 3).

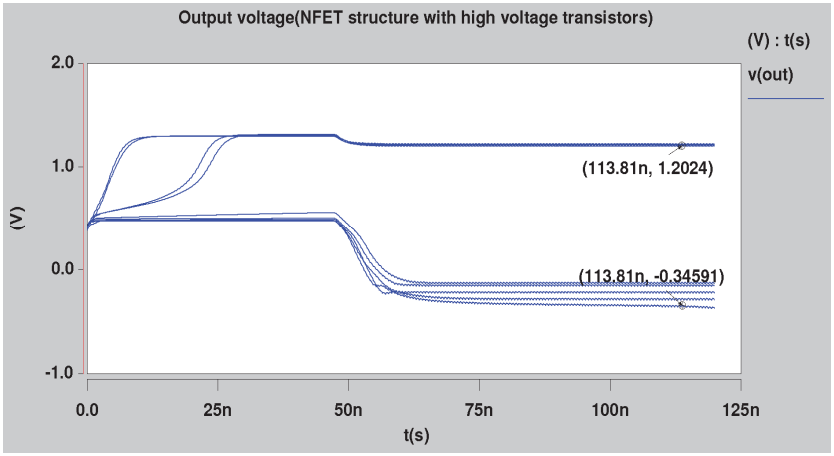

Fig.3. The output voltage for the NFET structure with hv transistors

The problem described above is solved by using the PMOS structure which is shown in Fig 4. The bulks of the M1 and M2 PFET transistors are connected to node V_Cbulk, hence excluding the stress possibility for them. The Cbulk capacitance charges to 2VDD-Vth level during the operation of the circuit. It gives an opportunity not to have a higher voltage than the power supply between any two terminals of the transistors.

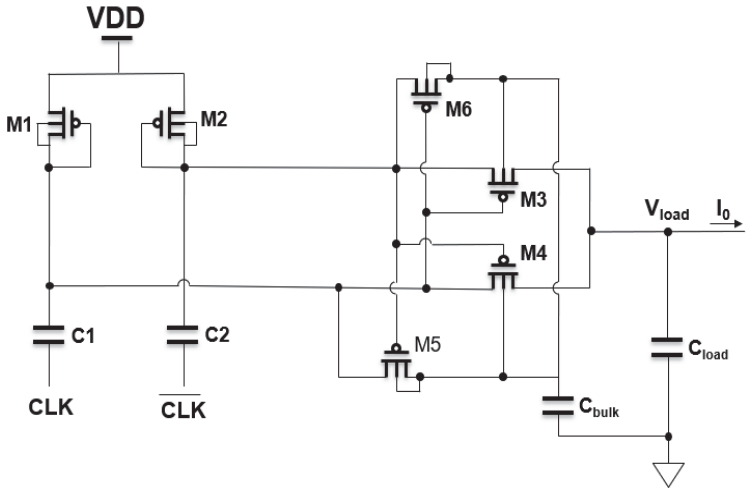

Fig.4. The proposed charge pump with a PFET architecture

Simulation Results. Both circuits have been designed by using the SAED 14 *nm* [3] technology and the Custom compiler design tool [4], and simulated by the HSPICE simulation tool [5]. An input voltage has been set to 0.8V expecting 1.2V in the output of the circuit.

Fig. 5 and Fig. 6 show the output voltage numbers during the process variation. Typical (TT), slow (SS), fast (FF), slow-fast (SF) and fast-slow (FS) models of transistors have been used. -40 ^{0}C and 125 ^{0}C have been used as bound numbers for temperature.

For the NMOS structure the output voltage variation is 1.2V+/-7.25% and for the PMOS- 1.2V+/-4.2%. The area of the PMOS charge pump is 26% larger than that of the NMOS.

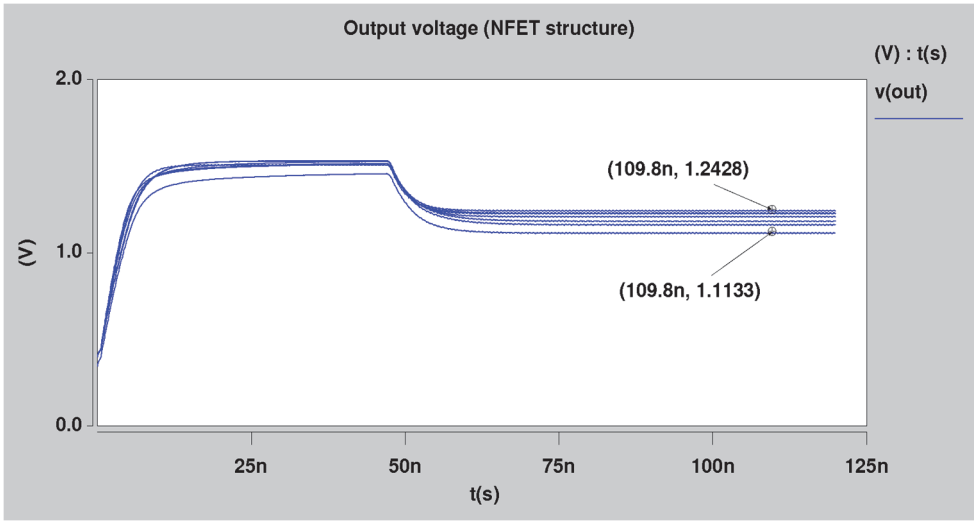

Fig.5. The output voltage for the NFET structure

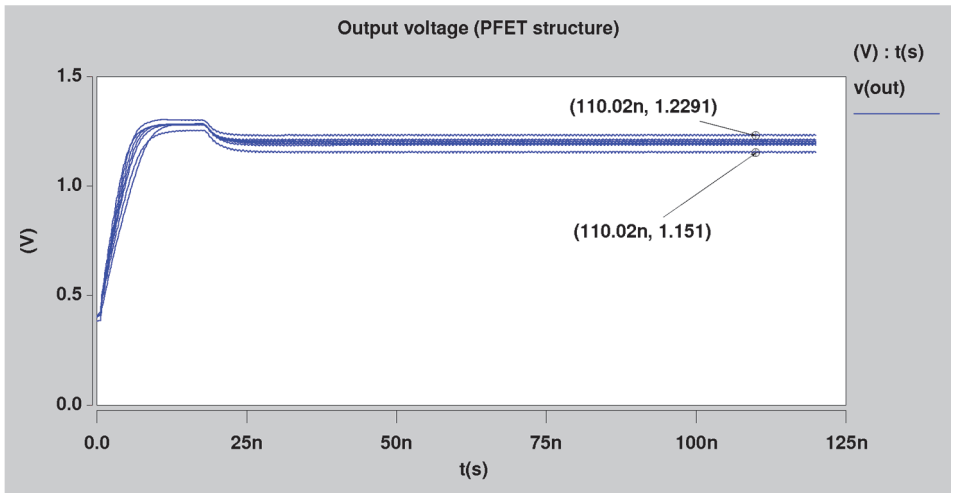

Fig.6. The output voltage for the PFET structure

The table below shows the occupied area of the PFET and NFET structures and the output voltage measurements during temperature and process variations. The advantages of the PFET structure is the noise immunity and the less output voltage spread, and the disadvantage is the area occupied.

Table

Output voltage numbers during temperature and process variations

Process	Temperature, (T ^{0}C)	Output voltage (PFET)	Output voltage (NFET)
TT	25	1.21	1.21
SF	-40	1.24	1.23
SF	125	1.2	1.23
FS	-40	1.2	1.11
FS	125	1.15	1.18
SS	-40	1.22	1.1
SS	125	1.19	1.16
FF	-40	1.22	1.24
FF	125	1.17	1.23

Conclusion. The charge pump architecture has been developed by mixing Dickson's and cross-coupled structures. The proposed circuit successfully provides 1,5 times higher input voltage at the output with a 4.2% voltage variation.

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Պ ՏԻՊԻ ՄԵՏԱՂ - ՕՔՍԻԴ ԿԻՍԱՀԱՂՈՐԴԻՉ (ՄՕԿ) ԿԱՌՈՒՑՎԱԾՔՈՎ ԲԱՐՁՐ ՀՈՒՍԱԼԻՈՒԹՅԱՄԲ ԼԻՑՔԻ ՊՈՄՊԻ ՍԽԵՄԱ

Կատարվել է երկու տարբեր ՊՄՕԿ և ՆՄՕԿ կառուցվածքներով, լիցքի պոմպով լարման կրկնապատկիչի սխեմաների նախագծում այնպես, որ ելքում ստացվի սնման լարումից 1,5 անգամ մեծ լարում: Գնահատվել են երկու սխեմաների մակերեսները, արագագործությունը և հուսալիությունը: Առաջարկվող ՊՄՕԿ կառուցվածքով նախագծված սխեմայում երկու առանցքային տրանզիստորներ չունեն հուսալիության խնդիր՝ ի տարբերություն ՆՄՕԿ կառուցվածքով տրանզիստորների, որը պայմանավորված է տրանզիստորների հարթակ-ակունք պոտենցիալների տարբերությամբ: Առաջարկվող սխեմայի ելքային ազդանշանի վարիացիան ավելի քիչ է, քան ՆՄՕԿ կառուցվածքով սխեմայում, սակայն մակերեսը 1,26 անգամ մեծ է:

Առանցքային բառեր. լիցքի պոմպ, Դիքսոնի լիցքի պոմպ, ցածր էներգասպառմամբ կառուցվածք, հաստատուն լարման փոխակերպիչ, ծերացում:

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СХЕМА ПОМПЫ ЗАРЯДОВ НА ОСНОВЕ МЕТАЛЛ-ОКСИД-ПОЛУПРОВОДНИКОВ П ТИПА С ВЫСОКОЙ НАДЁЖНОСТЬЮ

Спроектированы два разных умножителя напряжения с помпой зарядов на основе металл-оксид-полупроводников п типа (ПМОП) и металл-оксид-полупроводников н типа (НМОП) так, чтобы напряжение на выходе получилось в 1,5 раза больше питания. Дана оценка площади, быстродействия и надежности двух схем. В отличие от НМОП структуры, в предлагаемой ПМОП структуре указанные два транзистора не имеют проблему старения, что обусловлено напряжением между подложкой и истоком транзисторов. Вариация на выходе в предлагаемой схеме меньше, чем в схеме на основе НМОП структуры, но площадь больше в 1,26 раза.

Ключевые слова: помпа зарядов, помпа зарядов Диксона, архитектура с низкой энергопотребностью, преобразователь постоянного напряжения, деградация.