ՀԱՅԱՍՏԱՆԻ ԳԻՏՈՒԹՅՈՒՆՆԵՐԻ ԱԶԳԱՅԻՆ ԱԿԱԴԵՄԻԱ
НАЦИОНАЛЬНАЯ АКАДЕМИЯ НАУК АРМЕНИИ
NATIONAL ACADEMY OF SCIENCES OF ARMENIA
ДОКЛАДЫ ԶԵԿՈՒՅՑՆԵՐ REPORTS

Հատոր Том Volume 115 2015 № 4

INFORMATICS

УДК 519.688

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Built-In Test Flow for FinFET-based Memory Devices

(Submitted by academician S.K.Shoukourian 10/VIII 2015)

Keywords: *FinFET, defect, fault modeling, test algorithm.*

1. Introduction. For many years on memory devices built with conventional planar MOSFET transistor technology hold the considerable market share in embedded semiconductor industry [1]. Nevertheless growing short-channel and current leakage problems of this type of transistors make it almost impossible to continue further scaling down the feature sizes without negative consequences [2, 3]. This means that the planar technology gets closer to its limit and in order to keep up with the Moore's law, there is a need to use the third dimension for constructing the transistors for future System-on-Chips (SoC) [1, 2]. Thereby several approaches have been proposed recently among which FinFET technology is considered as having all the necessary preconditions to become the long-term MOSFET successor [1-4]. Unique structure of FinFET transistors among the other useful features allows significantly reducing short-channel effects making them highly demanded in the modern semiconductor industry [2, 3].

Fig. 1 shows the three dimensional structure of FinFET according to its definition in literature and displays several of the most important FinFET parameters: height of the Fin (HFin), its width or body thickness (TFin), and FinFET channel length (Lg) [1-4]. Due to its structure FinFET have several more advantages over MOSFET including controlled fin body thickness, low threshold-voltage variation and lower operating voltage [2, 3]. Nevertheless it is important to mention that despite the significant power and performance benefits, FinFET design and manufacturing doesn't come at the same cost as MOSFET and is still a challenging task [5].

Despite the importance of the problem of developing embedded test solutions for FinFET-based memory devices, relatively small number of research activities has been done in this area so far. In most of the related works the focus was set on separate aspects of FinFET testing and suggesting local solution for each individual situation.

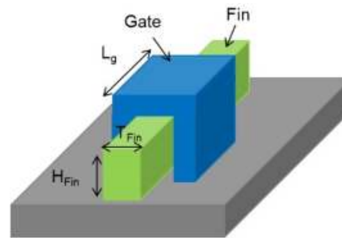

Fig. 1. FinFET structure.

For instance, in [6] and [7], several types of open and short defects in FinFET logic circuits have been investigated and showed that an open defect on the back gate causes delay and leakage problems unique to FinFETs.

In [8] stuck-open faults (SOF) for FinFET-based memory devices were examined and two new vector strategies were proposed for increasing the possibility of SOF defects detection.

Finally in [9], stuck-open, stuck-on and gate oxide short defects on different number of Fins within one FinFET transistor have been investigated. According to the results if this number is large enough, the defect can be modeled with stuck-open or delay faults.

Taking into account the novel structure of FinFET-based memory devices, the traditional test development flow [10], which is typically used for planar memory devices, cannot be applied to FinFETs in its primary form. This paper describes the way how each of the steps of the flow needs to be tuned in order to take into consideration all the specifics of FinFETs.

2. Test development flow. The requirements for different aspects of embedded memories testing change with the shrinking of transistor technology, which is used in memory devices. It is a natural process since each generation of the transistors can have structural and behavioral differences compared to the previous one. Thus, the test development flow can differ among different transistor technology generations. During the recent years this process was mainly stabilized since the usage of MOSFET transistor technology in the embedded memory devices became prevailing. The scalability of MOSFET technology allowed constantly shrinking the technology without serious impact on memory Built-in Self-Test (BIST) solution used. The typical test development flow [10] looks like pictured in Fig. 2. With each technology change the following major steps should be completed to obtain the upgraded BIST solution for embedded memories:

1. *Technology Node Selection*: Each time new technological node is available it needs to be investigated in order to construct the accurate embedded test and repair solution for it.
2. *Defect Injection*: The characteristics of the arriving technology node are analyzed and based on the results new defect types are identified specific for the technology. These defects are then injected into memory in order to investigate their behavior.

3. Fault Extraction: As the next step, for the set of injected defects the corresponding memory fault models need to be extracted, which reflect the behavior of the defects at functional level.

4. *Test Solution Construction*: For the set of identified fault models the optimal test solution is constructed which detects the faults in the optimal period of time.

5. *BIST Solution Upgrade*: Finally the constructed test solution is integrated into the memory BIST for providing the high fault coverage.

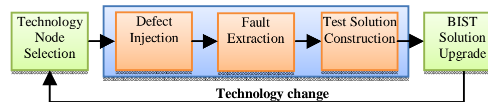

Fig. 2.Typical test development flow for embedded memories.

Using this flow a set of MOSFET technology specific defects was well investigated and corresponding fault models were developed with the shrinking of the technology. Nevertheless, for the latest generation of MOSFET transistors, especially starting from around 65nm and down to 20nm, this flow was mainly used to define the probability of the faults occurrence since no new types of faults were being identified any more.

However, the situation extremely changes with the MOSFET technology coming to its limits at 20nm. In order to cross this border new technological solutions come to the action and the established test development flow need to be accustomed to them. This especially applies to FinFETs since the spatial structure of FinFET transistors opens the doors for occurrence of new types of defects and thus leading to new fault models and possibly new test algorithms for their detection. Hence there is a need to reconsider the steps of the flow (highlighted with the blue box in Fig. 2), namely “Defect Injection”, “Fault Extraction” and “Test Solution Construction” for FinFET-based memory devices. In Section 4the effect of the technology change from MOSFET to FinFET on each of the mentioned steps in the test development flow is demonstrated.The experimental results are presented which show the effectiveness of the proposed enhanced flow.

3. FinFET defect models. As mentioned above, the acute distinction in structures of planar MOSFET and non-planar FinFET technologies mean that the same set of defects that was considered for MOSFETs cannot be applied to FinFETsas is. Fig. 3 shows the basic set of defect types which were considered for FinFETs in the “Defect Injection” step. This list includes the defects specific to FinFETs as well as defects common for both technologies:

(a) Fin Open – Full and resistive open defects on Fin;

(b) Gate Open – Full and resistive open defects on Gate;

(c) Fin Stuck-On – Full and resistive short defects between Source and Drain;

(d) Gate-Fin Short – Full and resistive short defects between Gate and Fin;

(e) Fin-VDD/VSS Short – Full and resistive short defects between Fin and VDD or Fin and VSS.

(f) Process Variation – Variations in FinFET parameter values.

4. Defect injection, fault modeling and test algorithm synthesis. After the set of defects going to be investigated was fixed, the next step was to inject the defects into the FinFET-based memory and model the resulting faults.

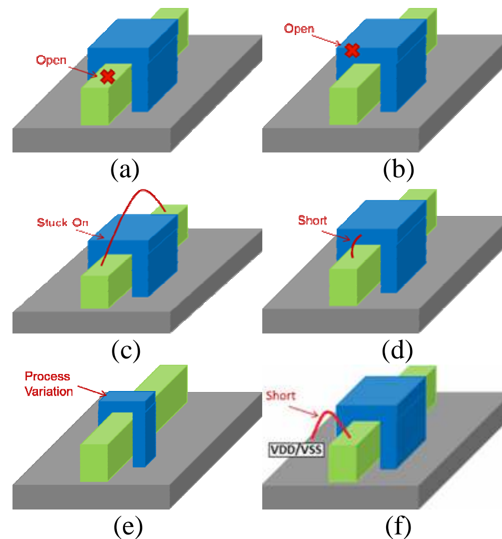

Fig. 3. Defect models considered for FinFETs.

For making this process more systematic and less time consuming an automated flow was developed (see Fig. 4). It made the investigation of FinFET defects a lot faster and more effective in terms of finding new faults specific to FinFETs. As an input, the flow receives a set of defects through Defect LIB and Simulation Setup containing a set of test sequences, with their test conditions (frequency, voltage, temperature), in case of resistive defect also the range of resistance magnitude. A defect is injected either in GDS or in SPICE Net-list depending on which one is more preferable in the particular case. Then two SPICE Simulations (defect-free and defect injected) are run with given Simulation Setup and for each simulation PASS/FAIL information and correspondding Waveforms of applied test operations are obtained. If FAIL is obtained for defective SPICE Net-list then it means that current Simulation Setup is correct and at least one of the provided test sequences detects the fault. Otherwise, if PASS is obtained then it means that the defect is not detected by the given test sequences and the simulation setup needs to be updated and the same process should be repeated with the new setup. This part is done by the user (test engineer or other relevant person) following some special rules. The process continues until the satisfactory test sequence(s) are found. Based on the received test sequences the fault models are extracted automatically.

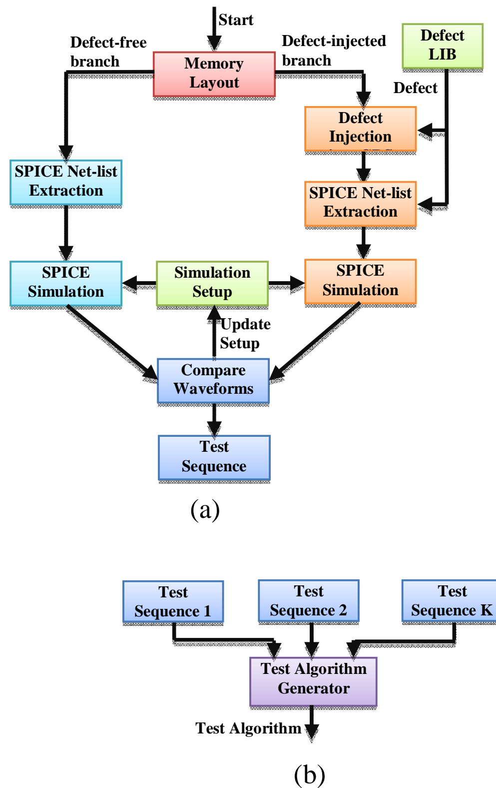

Fig. 4. (a) –Defect Injection and Fault Modeling Flow; (b) – Test Algorithm Synthesis Flow.

The next major step after the fault models and the corresponding test sequences are identified is the construction of a test algorithm for detection of a given set of faults. This step of the flow was also automated to take as an input a set of obtained Test Sequences and generate the optimal test algorithm. The advantage of this approach is that the flow becomes more generic since there is no dependency on fault types. Besides it becomes more efficient as the output test sequences of the described flow become direct inputs for the algorithm generation flow and all these happens automatically without any need for human intervention. It is also important to note that according to the experiments if the given Test Sequences have minimal lengths in terms of detecting the given defects/fault models, then Test Algorithm Generator will synthesize minimal test algorithms [11].

5. Experimental results. The proposed enhanced flow was validated on several FinFET-based memory devices obtained from different foundries. The results of the performed huge number of SPICE

simulations proved the viability of the described solution and led to some interesting results summarized in [12] and [13].Each defect was injected into pass-gate (PG), pull-down (PD) and pull-up (PU) transistors one at a time and furthermore multiple defects were injected simultaneously in the same memory cell. The same defects were also injected into planar 28nm and 45nm memory devices in order to compare the obtained results.

Some of the most important statements derived are listed below:

- FinFET-based memory devices are more prone to dynamic faults than planar-based memories.
- FinFET-based memory devices are more stable to process variation faults.
- Static single-cell and coupling faults are typical for both FinFET- and planar-based memory devices.

Fig. 5 presents two examples of simulation waveforms, which were obtained for two different types of defects injected into the memory cell under the different test conditions.

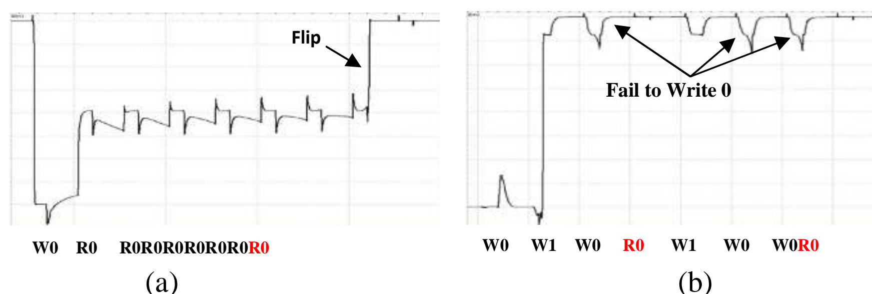

Fig. 5. (a)– Resistive Fin Open defect in PD transistor; (b) – Resistive Gate Open defect in PG transistor.

In the figure (a) the simulation output is depicted for the case when a resistive Fin Open defect is injected into a pull-down transistor of a FinFET-based memory cell. It results in seven-operation dynamic Deceptive Read Destructive Fault dDRDF0-7, where the 7th R0 operation is flipping the content of the cell without reporting a mismatch while the 8th R0 operation detects the fault. So Test Sequence = {W0, R0, R0, R0, R0, R0, R0, R0, R0} and the corresponding fault model is dDRDF0-7 = <0R07/1/0>.

Meanwhile the figure (b) shows the result in the case when a resistive Gate Open defect is injected into a pass-gate transistor of a FinFET-based memory cell. It results in a well-known transition fault TF0 = <1W0/1/-> and the corresponding Test Sequence = {W1, W0, R0} or {W1, W0, W0, R0}.

6. Conclusions. This paper describes the way how a commontest developmentflow can be tuned for FinFET-based memory devices. Each of the steps in the flow was investigated in detail and the required enhancements were outlined which need to be applied. For this purpose a new strategy was proposed which

helps to make the flow more systematic and automated in order to reduce the time and efforts necessary for modeling FinFET-specific faults and synthesizing test algorithms for their detection.

The results of experiments done for several real-life 16nm and 14nm FinFET-based memory instances proved the use fulness of the flow and revealed some interesting characteristics of FinFET-based memory devices. In particular, the experiments showed that FinFET-based memory devices compared with planar-based devices are more prone to dynamic faults and are more stable to process variation faults.

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Built-In Test Flow for FinFET-based Memory Devices

Rapidly developing FinFET technology, alternative to the conventional planar technology, plays an important role in routing modern silicon industry. Due to their unique structure, the defect types and corresponding fault models for FinFET transistors are different compared to planar ones. As a result the established flow used for synthesizing the embedded test solutions for MOSFET-based memory devices does not enable a smooth transition to FinFET-based devices. Thus, there is a need to tune the existing solution to support FinFETs. In this paper the upgraded and automated test development flow is introduced for FinFET-based memory devices, which was validated on several 16nm and 14nm memory instances. Eventually new faults were identified that are specific to FinFETs and their behavior was studied in detail.

Գ. Ա. Ճաղարյան

ՖինՖԵՏ հիշող սարքերի ներդրված թեստավորման ընթացք

Արագորեն զարգացող ՖինՖԵՏ տեխնոլոգիան՝ ավանդական պլանար տեխնոլոգիայի այլընտրանքը, շատ կարևոր դեր է խաղում ժամանակակից սիլիկոնային արդյունաբերության ուղղորդման գործում: Շնորհիվ իրենց յուրահատուկ կառուցվածքի՝ ՖինՖԵՏ տրանզիստորների դեֆեկտների տիպերը և համապատասխան անսարքությունների մոդելները տարբերվում են պլանար տրանզիստորներից: Արդյունքում ներդրված հիշող սարքերի թեստավորում անլուծումների սինթեզման համար օգտագործվող ամրագրված ընթացակարգը չի կարող սահուն կիրառվել ՖինՖԵՏ հիշող սարքերի համար: Ուստի կարիք կա ձևափոխելու գոյություն ունեցող լուծումը ՖինՖԵՏ-ների համար: Այս հոդվածում ՖինՖԵՏ հիշող սարքերի համար թեստի մշակման բարելավված և ավտոմատացված ընթացակարգն է ներկայացված, որը վավերացված է մի քանի 16 և 14 նանոմետրանոց հիշող սարքերի նմուշների վրա: Արդյունքում նոր անսարքություններ են հայտնաբերվել բնորոշ միայն ՖինՖԵՏ-ներին, որոնց վարքը խորությամբ ուսումնասիրվել է:

Г. А. Джагарян

Последовательность встроенного тестирования для устройств памяти, основанных на технологии ФинФЕТ

Быстро развивающаяся технология ФинФЕТ, альтернатива существующей планарной технологии, играет важную роль в развитии современной силиконовой промышленности. Благодаря их уникальной структуре типы дефектов и соответствующие модели неисправностей для ФинФЕТов отличаются по сравнению с планарными транзисторами. В результате уже существующая процедура, используемая для синтеза встроенных решений по тестированию устройств памяти, основанных на технологии МОСФЕТ, не позволяет плавно перейти к устройствам памяти, основанным на технологии ФинФЕТ. Таким образом, возникает необходимость усовершенствовать существующее решение для технологии ФинФЕТ. В этой статье представлена модернизированная и автоматизированная процедура для разработки тестовой методологии для устройств памяти, основанных на технологии ФинФЕТ, который был проверен на нескольких 16 и 14 нанометрических экземплярах устройств памяти. В результате экспериментов были обнаружены новые неисправности, которые свойственны только таким устройствам. Поведение этих неисправностей было изучено в деталях.

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