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Overvoltage Elimination of Dual-Branch Series–Parallel Charge Pumps with Thin Oxide Transistors

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Abstract
Integrated circuits increasingly rely on on-chip generation of voltage levels beyond the nominal supply. Charge pumps provide this functionality using capacitors and switches, but their boosted internal nodes raise reliability concerns in scaled CMOS technologies, especially in processes offering only thin-oxide devices. Prior studies have shown that aging mechanisms such as bias temperature instability can noticeably alter the output voltage and startup behavior of conventional series-parallel charge pumps. This paper presents an aging-aware series–parallel voltage doubler that mitigates overstress at critical output nodes while preserving the intended voltage-boost operation. The circuit is sized to match the fresh-state characteristics of the reference design, enabling a fair comparison. Simulation results under long-term BTI stress confirm improved stability of the charge-pump behavior with reduced aging-induced drift.

Keywords: Charge pump, Voltage doubler, Bias Temperature Instability (BTI), Overstress mitigation, Series–parallel topology, Overvoltage elimination

1. Introduction

Integrated circuits (ICs) constitute the backbone of modern electronic and information technologies, enabling computation, sensing, and communication across domains ranging from consumer electronics to biomedical instrumentation, autonomous transportation, and defense systems. In everyday use, ICs power computers, smartphones, and televisions by providing processing, storage, and reliable transfer of digital information.[1] At the infrastructure level, they are equally indispensable in fiber-optic networks, satellite links, and wireless connectivity, where performance and robustness directly determine system-level quality of service. As emerging workloads in artificial intelligence, machine learning, and the Internet of Things continue to expand, ICs are increasingly expected to deliver higher functionality together with stringent energy-efficiency and long-term reliability requirements.[2]

Within modern ICs, on-chip generation of auxiliary voltage domains is often mandatory to satisfy block-level requirements that cannot be met by the nominal supply alone.[3] Charge pumps (CPs) represent one of the most widely adopted solutions for this purpose, since they provide voltage multiplication using only capacitors and switches and can be fully integrated with a compact form

factor and a straightforward pumping mechanism.[4] Conceptually, charge pumps operate as voltage multipliers driven by two non-overlapping clock phases, typically supplied by an oscillator that produces out-of-phase control signals.[5] Historically, CPs span a broad range of applications: classical Cockcroft–Walton structures were originally intended for high-voltage generation and remain associated with use cases such as particle acceleration and X-ray tubes, while monolithically integrated Dickson-type pumps have been broadly adopted in IC practice, including as on-chip high-voltage generators for non-volatile memories.[6] In addition, modern CPs serve as embedded DC–DC building blocks in low-power and energy-harvesting systems, and they are routinely employed whenever a compact "voltage booster" is needed without inductors or off-chip magnetics.[7]

Despite these advantages, long-term reliability has become a limiting factor in aggressively scaled CMOS technologies. A fundamental issue is that supply-voltage scaling has not always kept pace with device-geometry scaling, producing non-ideal voltage distributions across transistor terminals and increasing susceptibility to electrical overstress.[8] Transistor aging, in turn, gradually degrades key parameters such as threshold voltage and drain current over product lifetime. This degradation arises from multiple concurrent mechanisms, including bias temperature instability (BTI), hot-carrier injection (HCI), and gate-oxide breakdown – often modeled as time-dependent dielectric breakdown (TDDB) – each driven by combinations of terminal voltages, switching activity, and temperature.[9] In scaled technologies, reduced oxide thickness and tighter reliability margins imply that even moderate excursions beyond recommended terminal-voltage limits can accelerate these mechanisms, leading to measurable performance loss and diminished lifetime robustness.[10]

Aging concerns become particularly acute in charge pumps because CP operation inherently creates elevated internal node voltages (and, by design, a boosted output), which can place thin-oxide devices under excessive electric-field stress if not carefully managed. More broadly in nanoscale design, undesirable voltage differences between transistor terminals – especially in thin-oxide devices – which accelerates degradation such as threshold-voltage shift and drain-current reduction.[11] This challenge is amplified in technology nodes where high-voltage (thick-oxide) options are unavailable, making design-level mitigation necessary to prevent overstress while still achieving the required boosted voltage.

Charge-pump design involves a central tradeoff: achieving sufficient voltage gain and load drivability. This has led to the development of a very large number of CP architectures and control techniques – reviewed across over twenty topologies – each introducing structural changes to improve charge transfer, reduce losses, or extend feasible operating conditions.[12] This work considers the series–parallel topology (Fig. 1) as a practical and scalable baseline for a voltage-doubler-oriented implementation.

The series-parallel CP employs series charging and parallel discharge controlled by anti-phase clocks, enabling voltage multiplication through structured reconfiguration of the pumping network.[13] It has been used as an auxiliary step-up switched-capacitor stage for voltage multiplication, and more recent literature has revisited it with improved gate-control strategies that reduce VTH-related losses. Nevertheless, the topology also exhibits reliability-relevant drawbacks, including parasitic capacitance overhead due to additional switches per stage and an output voltage that can decrease strongly with increasing stage number – both of which motivate careful architecture and device-stress-aware refinement.[14] Building on these observations, the remainder of this paper develops an aging-aware series-parallel (voltage-doubler) charge-pump architecture that explicitly targets overvoltage elimination at critical nodes, thereby improving long-term reliability in thin-oxide-only processes while preserving the intended voltage-boost functionality.

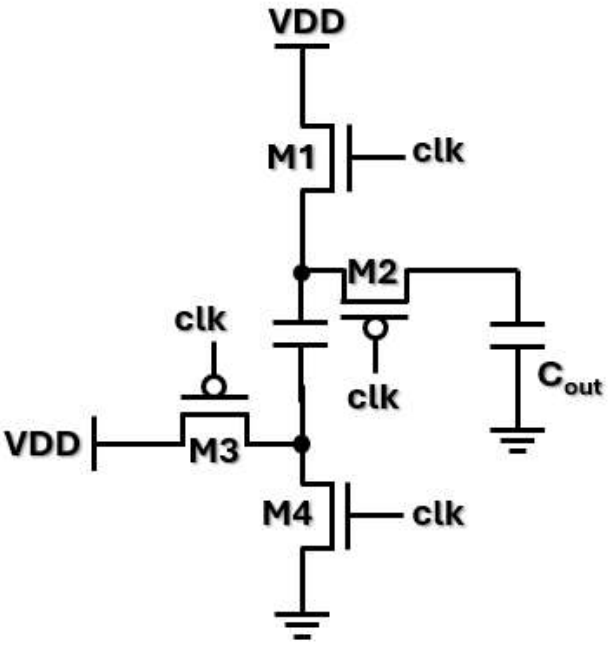

Figure 1. Series-parallel charge pump topology.

2. Previous studies

Beyond efficiency, prior work has directly shown that aging mechanisms can materially alter CP behavior, especially because CPs inherently generate elevated internal node voltages. A representative example is [15], which investigates BTI-related aging across five CP topologies (including series-parallel Fig. 2) and reports aging-aware simulation comparisons.[15] The study CMOS process with nominal VDD=1V, uses V_{in}=1V, and evaluates performance via the maximum output voltage V_{OUT} and the ramp-up time t_{ru} (time to reach 90% of V_{OUT}). Importantly, the authors observe that some transistors in the series-parallel (as well as latch-based and exponential-gain) structures experience V_{GS}>1V, indicating increased bias stress and therefore stronger susceptibility to BTI-induced degradation.

Quantitatively, the reported results show that the series-parallel CP exhibits notable aging-driven shifts after 8 years of BTI stress. At 27 °C, V_{OUT} changes from 1,406 V (fresh) to 1,43 V (aged), while t_{ru} increases from 3,53 μs to 3,87 μs (≈9,63%). At 85 °C, the degradation is more severe: V_{OUT} shifts from 1,427 V to 1,469 V and t_{ru} increases from 4,06 μs to 5,04 μs (≈24,1%). The paper also highlights a practical reliability perspective: either an increase or a decrease of V_{OUT} should be treated as a specification violation, since regulated or tightly bounded voltage targets are often required in CP-powered subsystems.

These findings collectively motivate aging-aware CP design, not only to prevent loss of efficiency but also to avoid long-term drift in generated voltage levels and startup dynamics. A key limitation for many emerging applications is that advanced nodes may offer only thin-oxide transistors, while thick-oxide/HV options become impractical, increasing the burden on circuit-level mitigation.[16] In such environments, reliability is constrained by maximum tolerable terminal voltages, and exceeding these limits increases the risk of destructive failure modes such as gate-oxide breakdown.[17] If an output-connected thin-oxide switch (e.g., the final-stage device M2) encounters a condition where its gate is held at logic 0 while its drain/source is driven near ∼2VDD, the resulting large V_{GD} or V_{GS} constitutes overstress.

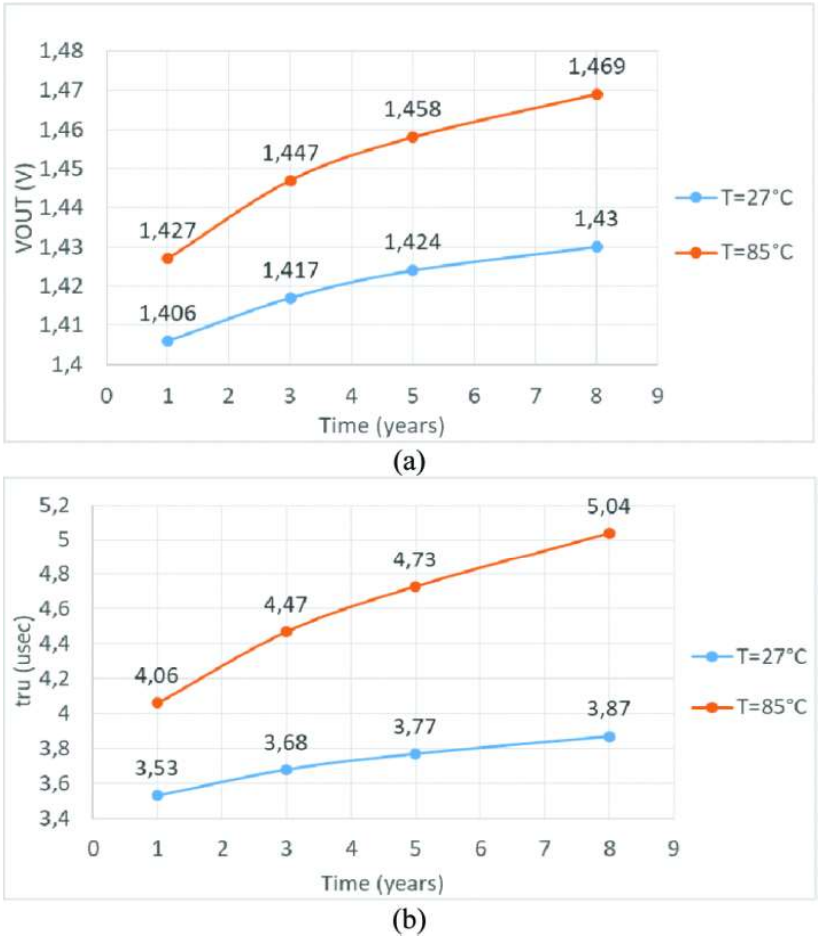

Figure 2. Series-Parallel Charge Pump: a) V_{OUT} and b) t_{ru} as a function of time.[15]

3. Recent achievements

Taken together, prior studies suggest that while the series-parallel CP is attractive for voltage boosting and has been widely analyzed from a topology perspective, its aging sensitivity under elevated internal voltages becomes a decisive challenge – especially in thin-oxide-only processes where overvoltage cannot be "outsourced" to high voltage devices. This motivates the need for architectural refinements that explicitly eliminate overstress at critical nodes while preserving the intended voltage-doubler functionality. To address this challenge, the architecture shown in Fig. 3 is proposed, which incorporates overstress-aware switching and node-voltage management to prevent excessive terminal voltage differences across thin-oxide devices during boosted operation. The next section details how the critical output transistors $M4$ and $M4'$ are protected while still delivering an output of approximately $\sim 2VDD$ and maintaining efficient charge transfer.

As shown in the schematic, the proposed design employs a dual-branch series–parallel charge pump. Compared with the single-branch implementation (Fig. 1), the dual-branch configuration charges the output capacitor $Cout$ up to $\sim 2VDD$ during both clock phases, thereby improving charging continuity and minimizing idle intervals. In addition, the component sizes were chosen such that, under fresh-device conditions, the key output characteristics – namely the steady-state output voltage and the ramp-up time – match those of the reference design, enabling a fair and direct comparison in subsequent aging and reliability evaluations.

The main difference from the conventional architecture is that the gate-control node of the output-stage transistor in one branch is driven by the output of the other branch. As a result, this control signal transitions from VDD up to $\sim 2VDD$ and never falls below VDD, which prevents the critical output

device from entering the worst-case overstress condition associated with a low gate level and a boosted drain/source voltage.

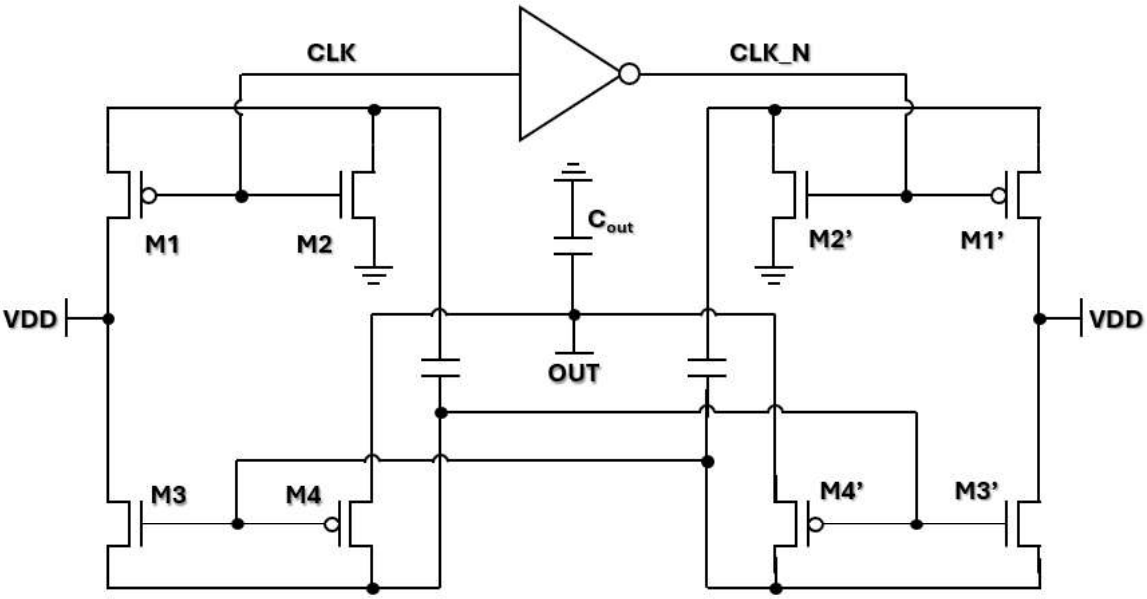

Figure 3. Proposed Series-Parallel charge pump circuit.

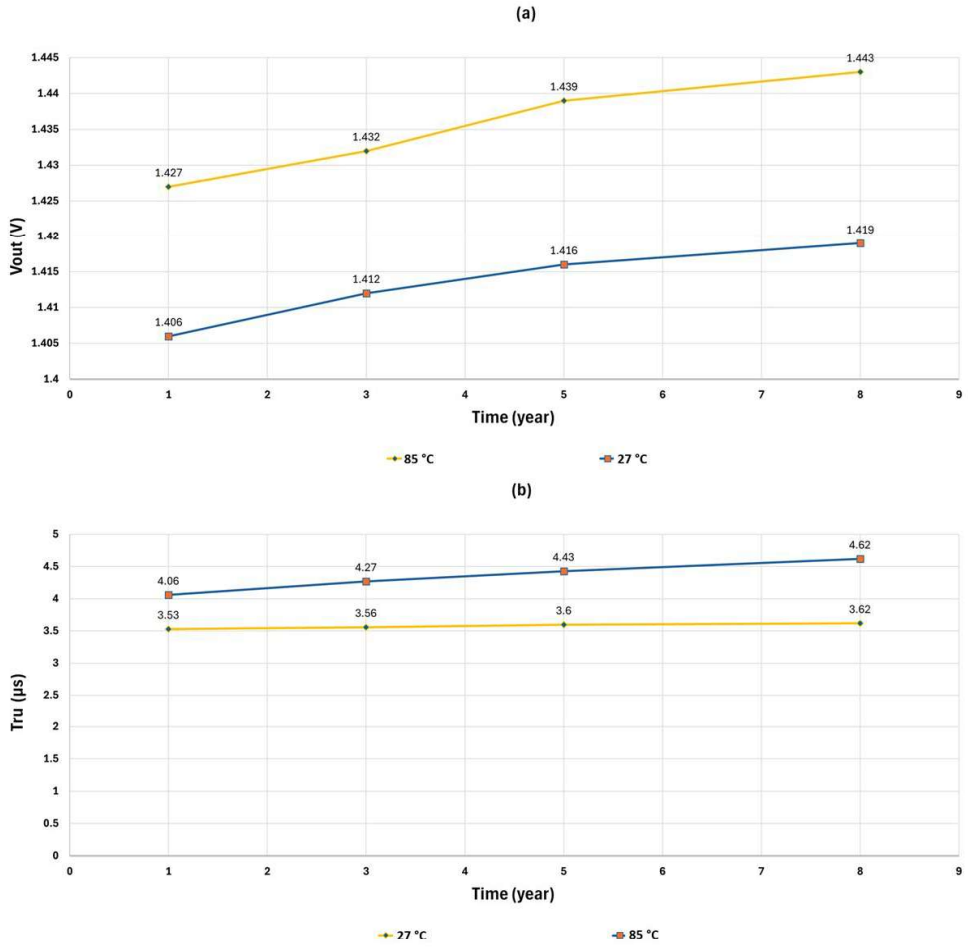

Figure 4. Proposed Series-Parallel Charge Pump: a) V_{OUT} and b) t_{ru} as a function of time.

Quantitatively, the results in Fig. 4. indicate measurable BTI-induced drift in the series-parallel CP over an 8-year stress period. At 27 °C, V_{OUT} increases from 1,406 V (fresh) to 1,419 V (aged), while tru rises from 3,53 µs to 3,62 µs (≈2,55%). At 85 °C, the impact becomes more pronounced: V_{OUT} shifts from 1,427 V to 1,443 V, and t_{ru} increases from 4,06 µs to 4,62 µs (≈13,8%).

4. Discussion

Two main reliability limitations characterize the conventional series–parallel charge pump when it is used as a voltage doubler in scaled CMOS. First, the boosted output and elevated internal nodes can place thin-oxide switches under unfavorable terminal-voltage differences during certain clock states – most critically when an output-connected device sees a low gate level while its drain/source is near $\sim 2VDD$. Such conditions increase electric-field stress, accelerate aging, and, in thin-oxide-only processes, raise the likelihood of severe oxide-reliability issues. Second, long-term BTI stress has been shown to distort the charge-pump behavior over time, affecting not only the start-up dynamics (ramp-up time) but also the steady-state output level, both of which are specification-relevant in many on-chip power domains.

To address these limitations, an aging-aware dual-branch series–parallel voltage doubler is introduced, incorporating overstress-aware node control at the output stage. The key architectural change is the cross-driven gate strategy: the gate-control node of the output transistor in one branch is driven by the boosted output of the opposite branch. This forces the gate signal to swing from VDD up to $\sim 2VDD$ and prevents it from dropping below VDD, thereby eliminating the worst-case low-gate/high-drain overstress scenario without sacrificing the intended $\sim 2VDD$ voltage-boost functionality. For a fair evaluation, the proposed design was sized such that its fresh-state output voltage and ramp-up behavior match the conventional reference.

Under an 8-year BTI stress evaluation, the proposed architecture demonstrates a clear improvement in aging robustness. In terms of ramp-up-time degradation, the increase is reduced from 9,63% to 2,55% at 27 °C (a 73,5% reduction in degradation) and from 24,1% to 13,8% at 85 °C (a 42,7% reduction). The long-term drift of the output level is also reduced: the $\Delta VOUT$ shift decreases by 45,8% at 27 °C and by 61,9% at 85 °C compared with the reference implementation. The netlists needed for simulation were exported by Galaxy Custom Designer tool.[18]

Future challenges include extending the proposed overstress-aware concept beyond the series–parallel voltage doubler to a wider set of charge-pump architectures. It is important to investigate how the same node-voltage management philosophy can be integrated into commonly used topologies such as the Dickson pump, cross-coupled charge pumps, and multi-phase switched-capacitor structures, where the location and severity of overstress-prone devices may differ. In addition, adapting the approach to higher conversion ratios (multi-stage pumps) and to topologies with different clocking schemes will require identifying the corresponding “critical” output and transfer switches and redefining their safe gate-drive generation. Such a topology-level generalization would clarify the applicability limits of the method and help establish a unified design guideline for overstress-free voltage boosting in thin-oxide-only processes.

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ԱՄՓՈՓԱԳԻՐ

Բարակ օքսիդով տրանզիստորներով երկճյուղ զուգահեռ-հաջորդական լիցքի պոմպերի գերլարումների վերացումը

Վազգեն Մելիքյան[1,*], Ռոման Իվանյան[1]

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Ինտեգրալ սխեմաներում ավելի ու ավելի հաճախ է պահանջվում սնուցման լարմանը գերազանցող մակարդակների առկայության ապահովումը: Այդ նպատակով կիրառվում են կոնդենսատորներ և փոխանջատիչներ պարունակող լիցքի պոմպեր: Սակայն վերջիններիս ներքին հանգույցներում առաջացող գերլարումները նվազեցնում են սխեմայի աշխատանքի հուսալիությունը: Նշվածը հատկապես տեղի ունի մասշտաբավորվող կոմպլեմենտար մետաղ-օքսիդ-կիսահաղորդիչ տեխնոլոգիաներով և միայն բարակ օքսիդով տրանզիստորներ պարունակող գործընթացներով պատրաստվող լիցքի պոմպերի դեպքում: Նախորդ աշխատանքներում ցույց է տրվել, որ ծերացման այնպիսի մեխանիզմները, ինչպիսիք են, օրինակ, ջերմաստիճանային շեղման անկայունությունը (ՋՇԱ), կարող են զգալիորեն փոխել ավանդական զուգահեռ-հաջորդական լիցքի պոմպերի ելքային լարումը և դրանց գործարկման բնութագրերը: Հոդվածում առաջարկվում է ծերացման նկատմամբ կայուն զուգահեռ-հաջորդական լարման կրկնապատկիչ, որում նվազեցվում է գերլարման ազդեցությունը կարևոր ելքային հանգույցների վրա՝ միաժամանակ պահպանելով նախատեսված լարման բարձրացման գործառույթը: Սխեման նախագծված է այնպես, որ թարմ (չծերացած) պայմաններում համադրելիության ապահովման նպատակով համապատասխանի նախորդ աշխատանքներում մշակված սխեմաների բնութագրերին: Սակայն միաժամանակ, ըստ երկարաժամկետ ՋՇԱ մոդելավորմամբ ստացված արդյունքների, առաջարկվող լիցքի պոմպը ծերացման հետևանքով առաջացող շեղումների նվազեցման շնորհիվ նախորդների համեմատ օժտված է աշխատանքի ավելի բարձր կայունությամբ

Բանալի բառեր՝ լիցքի պոմպ, լարման կրկնապատկիչ, ջերմաստիճանային շեղման անկայունություն (ՋՇԱ), գերլարման ազդեցության նվազեցում, զուգահեռ հաջորդական տոպոլոգիա, գերլարումների վերացում