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**THE CLOCK DUTY-CYCLE CORRECTION CALBRATION METHOD
FOR HIGH-SPEED TRANSMITTERS**

In modern high-speed SerDes systems, maintaining optimal clock quality is critical for ensuring data integrity and system reliability. This paper presents the TX delay-loop line (DLL) clock duty-cycle correction calibration method intended to respond to challenges coming from increased data rates and high-frequency clocks. The proposed method calibrates the duty cycle of the transmitted clock, minimizing jitter and skew that can lead to duty-cycle distortion (DCD), inter-symbol interference (ISI) and greater bit error rates (BER). Through several simulation tests and validations, it is shown that the method effectively improves the clock quality, particularly the duty-cycle, thereby enhancing the signal integrity and system performance in demanding high-speed communication environments. This work underscores the importance of precise clock duty-cycle correction in achieving robust and efficient SerDes operation at gigabit and beyond data rates. The proposed method covers roughly $\pm 6.5\%$ of the duty-cycle correction range. Through simulation results we encounter horizontal eye-opening improvement at transmitter differential output by $\sim 5ps$ for the 64 Gb/s data rate. The proposed method leads to 3.8% area increase.

Keywords: duty-cycle, calibration, eye opening, comparator, ISI, BER.

Introduction. There's continual push for higher data rates for the current high-speed serial links to support modern applications like 5G, cloud computing and data centers. As data rates increase, various challenges occur, such as power efficiency, noise immunity and signal integrity. To keep up with the pace and have the higher data rates within the same bandwidth range, the current trends use Pulse Amplitude Modulation (PAM4) over the Non-Return to Zero (NRZ) signaling. Since PAM4 can transmit more data over existing channels without requiring additional bandwidth, it maximizes the utilization of available channels, which is critical in environments where bandwidth is limited. It also provides higher efficiency, less loss at high frequencies, and enables to use slower clock rates than regular binary communication. Despite these advantages, it's worth noting that PAM4 also brings to table some challenges, such as increased sensitivity to noise and reduced signal-to-noise ratio (SNR) due to limited distance between levels. Additionally, the design of the transmitters and receivers' circuitries are significantly more complex for the PAM4 than for binary signals. Fig.1 illustrates

the block diagram of the high-speed SerDes systems [1]. Transmitters must generate multiple voltage levels and maintain signal integrity to avoid introducing distortion. On the other hand, receivers side need more advanced circuitry to accurately detect and differentiate between closely spaced amplitude levels. Advanced equalization techniques are to have to fight against inter-symbol interference (ISI). In the receiver side the most common blocks for this purpose are the continuous-time linear equalizer (CTLE) and decision feedback equalizer (DFE). CTLE is useful in canceling both pre-cursor and long-tail inter-symbol interference (ISI), but CTLE amplifiers must be designed with sufficient bandwidth and linearity to support PAM4 modulation [2]. DFE is highly effective against ISI and effectively cancels it out by using previous decisions about transmitted symbols to predict and subtract their effects on the current symbol. By mitigating ISI, DFE can improve the effective SNR which leads to reduced bit error rates (BER).

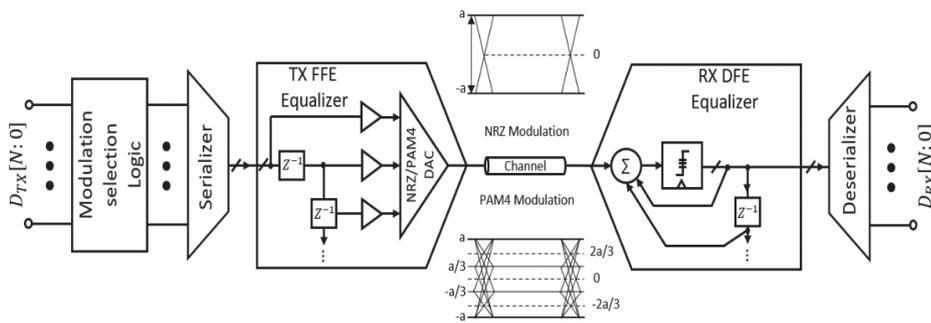


Fig.1. The block diagram of the high speed SerDes system

The TX architecture can be generally categorized by a voltage mode driver (SST) or a current mode driver (CML). Although SST driver's power consumption is substantially smaller than CML driver's power, the data path and clocking power may not show meaningful difference between the two architectures, especially for a high data rate systems such as 112 Gb/s. The SST architecture is more preferred under a limited supply level $\leq 1V$, since the data path can be fully CMOS [3]. The quarter-rate 4:1 multiplexer (MUX) is popular for the last serialization stage due to its relaxation on the timing constraint and low-power consumption in the clock path than the half-rate structure [4].

For that purpose, input clocks for the 4:1 MUX should be accurately skewed by 1UI from each other. To generate the required phases, delay a line loop (DLL) is used which receives differential clocks from the phase-locked loop (PLL) and generates the required phases for the driver and serializer. In advanced modulation schemes like PAM4, where signal levels are closely spaced, any timing error can

lead to significant data errors. A precise clock path is essential for ensuring the correct sampling of the digital signal levels. For that purpose, in this article we are going to introduce a calibration method of the duty-cycle correction for the DLL clocks, which can significantly improve the transmitters ISI and BER consequently.

Problem description. As discussed previously, a good clock path quality is an essential attribute for the high-speed data transfer in the modern serial link's transmitter (Fig.2). As the clocks are being generated from the PLL and being transferred to the TX through the routes and multiple logic circuitry, the degradation of its quality is unavoidable. Additionally, PVT (process-voltage-temperature) variations make it harder to maintain the desired merit consistent.

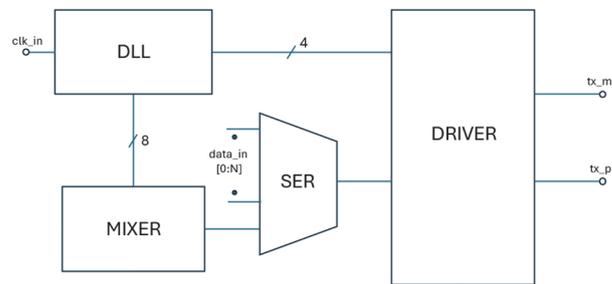


Fig.2. The transmitter's simplified block diagram

Such imperfections coming from circuitry and PVT variations lead to duty-cycle-distortion of the clocks (DCD). Its impact even more crucial for the high-speed clocks (7/8/10 GHz, depends on the data rate). Moreover, as the frequency of the clock increases so does the jitter coming from the different noise sources, such as: thermal, shot and especially switching noise.

A distorted clock at the driver stage can potentially lead to the data/bit errors. The impact of the stated can be measured in a different way, but the most straightforward and applicable way is to look at the eye opening in the two most critical points of the data path. The first one is the output of the 4:1 sterilizer in the driver, and the second one is the output of the driver itself. The impact would be instantly noticeable at the 4:1 MUX output where the data sent can be disrupted to the point of no return. It is because the data alignment is being done inside the MUX at the highest clock frequency (and the output data after this stage is in the Nyquist frequency). The second point of the measure, the driver's output, gives more general understanding of the system performance, where not only clock path delivers its enormous impact, but also part of the quality is being determined by the transmission channel, output impedance termination, and applied equalization. Thus, the impact of the proposed improvements will be measured in the two points discussed.

The proposed architecture. PLL and DLL are the two major blocks delivering the required clocks with the needed phases and frequencies. On the DLL-to-driver path an additional buffer tree is inserted to ensure proper drivability and CMOS level clocks at the input of the 4:1 MUX's.

The basic DLL loop consists of a controlled delay line, a phase detector (PD) and a low-pass filter. To control the duty-cycle of the clocks at the output of the delay line, the analog inverters are being inserted into the loop (Fig.3).

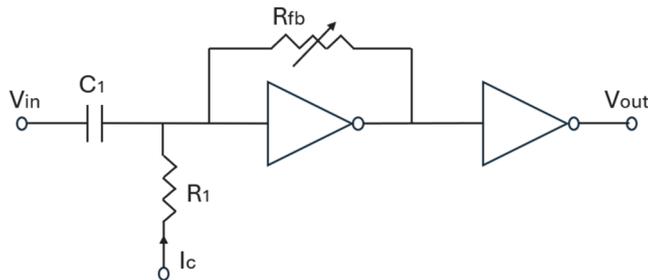


Fig. 3. Duty-cycle correction circuit based on analog inverter

The I_c current is inserted into the inverters input feedback node, in order to control its transition time, hence affecting duty cycle at the output. The required currents are generated through the current DACs. The proposed method helps choose the required codes for the DACs.

The proposed method. So far, we have the DCC correction block (analog feedback inverter) and the current DACs to control the required insertion input currents for the inverters. To have a detection/decision making loop, we need a feedback loop which will adjust the DAC codes. The block-diagram of the loop is shown below (Fig. 4).

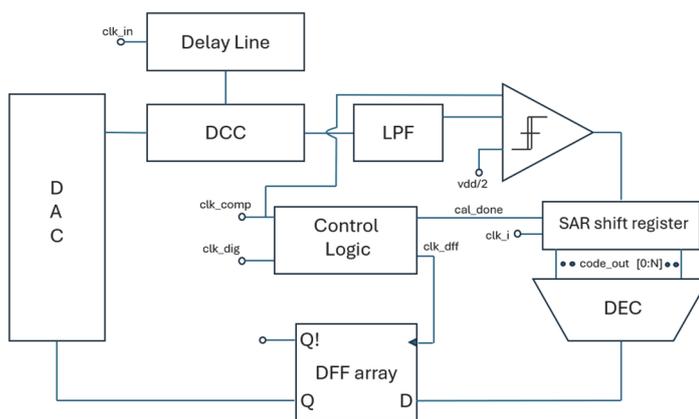


Fig. 4. The block diagram of the duty-cycle correction calibration method

At the output of the DCC inverters, a low-pass filter is placed. It integrates the clocks and sends the obtained voltage levels ($V_{DD}/2$) to the comparator. The comparator's reference node is being connected to the $V_{DD}/2$, which is being generated through a precise DAC, serving as a reference for the system's various calibration and adaptation algorithms. A 10-bit current DAC is used for the calibration.

After the comparison is done, the results are saved in the 10-bit SAR shift register. We start the calibration from the DAC's middle code, thus, the register's starting position should be 512. It is the most convenient starting point for calibration in order to keep the number of repetitions to a minimum. The output of the register will be decoded and returned to the DAC. The output of the register will be decoded and sent back to the DAC. We also need to close the loop once the calibration is complete. For this purpose, each clock cycle of the comparator is counted, and once the required cycle step is completed, the "cal_done" signal is sent to the digital control block, which controls all the PHY's calibration and adaptation processes. The calibration process ends when the "cal_done" signal equals "1".

Results. To verify the impact of the proposed method, three different tests were performed. The first and most straightforward test measures the DLL output clock duty-cycle before and after the calibration process. Fig. 5 shows the duty-cycle before the calibration process, and it is equal to 54.7%.

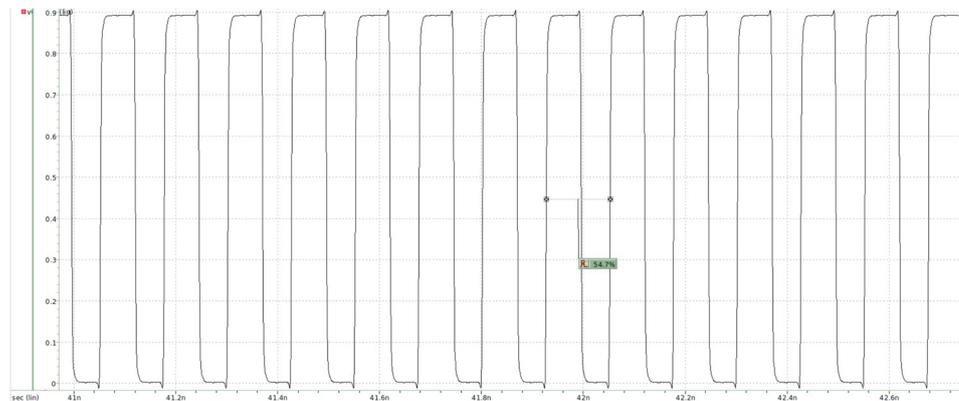


Fig. 5. The clock's duty-cycle before calibration

After implying calibration, the duty-cycle is being improved by 4.8%, resulting in 49.9% (Fig. 6).

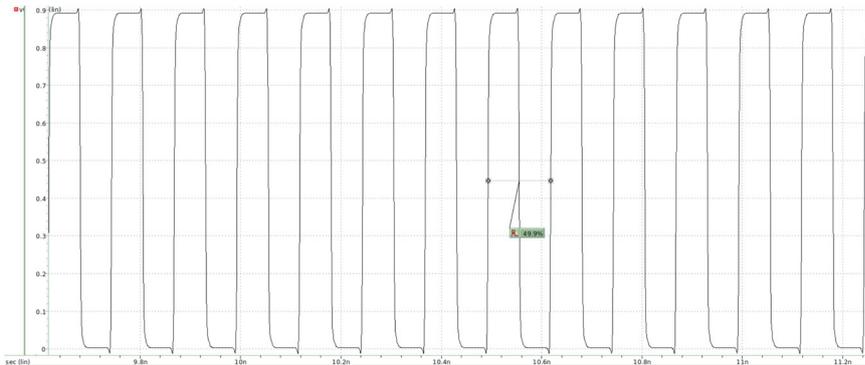


Fig. 6. The clock's duty-cycle after calibration

Overall, DACs (calibration) cover roughly $\pm 6.5\%$ duty-cycle correction range.

As stated, the clock quality will greatly impact on the final 4:1 serialization. Thus, the next verification is a transient simulation where we can see the data eye diagram after 4:1 MUX serialization (Fig. 7).

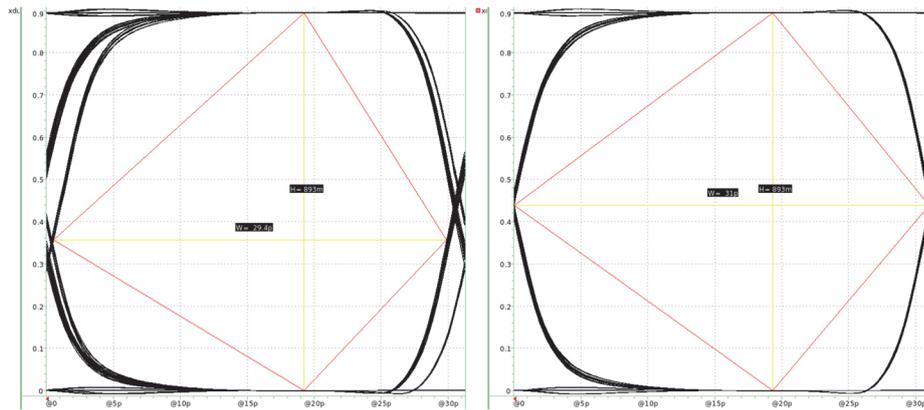


Fig. 7. 4:1 MUX output eye diagrams before and after calibration

The left diagram is the eye before the calibration and the right one, after. Before the calibration, due to distorted duty-cycle of the clock, the eye diagram is “jittery”, resulting in double crossing points and relatively closed horizontal opening (29.4ps). After the calibration, the eye quality improves in terms of jitter and horizontal opening (31ps).

Finally, TX differential output eye openings were obtained to understand the impact in the final stage (Fig. 8).

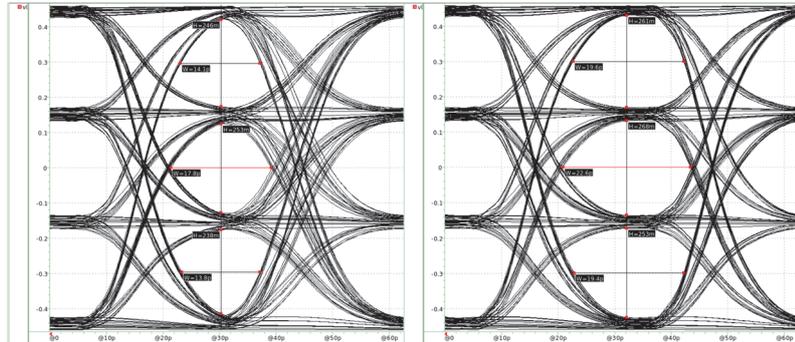


Fig. 8. TX output eye diagrams before and after calibration

We can see that the “jittery” eye diagram shown in Fig. 7 results in the poor quality of the eyes in the TX output. The horizontal eye openings are smaller by almost $5ps$ for all three eye openings compared to the obtained diagrams after calibration.

The added circuitry increases area by 3.8%. However, the comparator and DACs are regarded as general-purpose devices in the PHY. They are used for a variety of calibrations and PHY adaptation.

Conclusion. The TX DLL duty-cycle correction calibration method has been described. The method improves the duty-cycle of the clocks and allows calibration/correction in a $\pm 6.5\%$ range. The simulation results show that after the calibration, for the typical test case scenario, the duty-cycle is improved by 4.8%. This results in significant improvements in both the 4:1 MUX output stage and the TX output stage. MUX output horizontal eye is improved by $1.6 ps$. TX differential output has been tested for the PAM4 modulation at $64 Gb/s$ data rate. Horizontal openings are improved by approximately $5 ps$ for all three eyes. Schematic updates result in a 3.8% area increase. The proposed method can be used in modern high speed TX designs.

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ՏԱԿՏԱՎՈՐՄԱՆ ԱԶԴԱՆՇԱՆԻ ՑԻԿԼԻ ՀԱՄԱՄԱՍՆՈՒԹՅԱՆ ԿԱՐԳԱՎՈՐՄԱՆ ԿԱԼԻԲՐԱՑՄԱՆ ՄԵԹՈԴ ԱՐԱԳԱԳՈՐԾ ՀԱՂՈՐԴԻՉ ՀԱՆԳՈՒՅՑՆԵՐԻ ՀԱՄԱՐ

Ժամանակակից արագագործ SerDes համակարգերում տակտային ազդանշանի որակի պահպանումը կարևոր նշանակություն ունի տվյալների ամբողջականության և համակարգի հուսալիության ապահովման համար: Ներկայացված է հաղորդիչ հանգույցի հապաղման գծի տակտային ազդանշանի կարգավորման կալիբրացման մեթոդ, որը նախատեսված է՝ արձագանքելու մշտապես աճող տվյալների փոխանցման արագության և բարձրահաճախական տակտային ազդանշանին առնչվող խնդիրներին: Առաջարկվող մեթոդը կատարում է տակտային ազդանշանի ցիկլի համամասնության կալիբրացում՝ նվազեցնելով ազդանշանի թրթռոցը և շեղումը, որոնք կարող են հանգեցնել ցիկլի համամասնության խեղաթյուրման, միջնիշային միջամտության (ՄՆՄ) և բիթային սխալանքի: Միմուլյացիոն թեստերի և փորձարարական հետազոտությունների արդյունքում երևում է, որ մեթոդն էականորեն բարձրաձայնվում է տակտային ազդանշանի որակը, մասնավորապես՝ ցիկլի համամասնությունը, դրանով իսկ բարելավելով ազդանշանի ամբողջականությունն ու համակարգի կատարողականությունը բարձր արագագործությամբ հաղորդակցման հանգույցներում: Աշխատանքում ընդգծվում է տակտային ազդանշանի ցիկլի համամասնության ճշգրիտ կարգավորման դերը՝ զիգաբիթ և ավելի բարձր տվյալների փոխանցման արագությունների դեպքում հուսալի և արդյունավետ հաղորդիչ-ընդունիչ հանգույցի աշխատանքի համար: Մեթոդն ապահովում է մոտավորապես $\pm 6.5\%$ ցիկլի համամասնության կարգավորման տիրույթ: Փորձերի արդյունքների համաձայն՝ հաղորդիչ հանգույցի ելքային դիֆերենցիալ աչքի հորիզոնական բացվածքը բարելավվել է 5պվ-ով՝ 64 Գբ/վ տվյալների փոխանցման արագության դեպքում: Առաջարկվող մեթոդը հանգեցնում է մակերեսի 3.8% մեծացման:

Առանցքային բառեր. ցիկլի համամասնություն, կալիբրացում, աչքի բացվածք, համեմատիչ, ՄՆՄ, բիթային սխալանք:

Л.Д. АКОПЯН

**МЕТОД КАЛИБРОВКИ КОРРЕКЦИИ ДИСБАЛАНСА ПО
ДЛИТЕЛЬНОСТИ ТАКТОВОГО СИГНАЛА ДЛЯ
ВЫСОКОСКОРОСТНЫХ ПЕРЕДАТЧИКОВ**

В современных системах высокоскоростных SerDes (Serializer/Deserializer) поддержание оптимального качества тактирования является критически важным для обеспечения целостности данных и надежности системы. В данной работе представлен метод калибровки с использованием задержки по линии (DLL) для коррекции формы сигнала тактового сигнала с учетом дисбаланса по длительности импульсов, предназначенный для реагирования на вызовы, связанные с ростом скоростей передачи данных и высокочастотными тактовыми сигналами. Предложенный метод нацелен на коррекцию коэффициента заполнения тактового сигнала, минимизацию джиттера и смещения, которые могут привести к искажению формы сигнала (DCD), межсимвольным помехам (ISI) и увеличению ошибок передачи (BER). На основе нескольких тестов и проверок с помощью моделирования показано, что данный метод эффективно улучшает качество тактирования, особенно коэффициент заполнения, тем самым повышая целостность сигнала и производительность системы в условиях высокоскоростной передачи данных. Подчеркивается важность точной коррекции дисбаланса по длительности импульсов для достижения надежной и эффективной работы SerDes на скоростях в гигабитах и выше. Предложенный метод охватывает примерно диапазон коррекции $\pm 6,5\%$ от полного диапазона. В результате моделирования зафиксировано улучшение горизонтального раскрытия глаза (eye-opening) примерно на 5 ns при передаче данных со скоростью 64 Гбит/с . Реализация данного метода приводит к увеличению площади на $3,8\%$.

Ключевые слова: длительность импульса, калибровка, раскрытие глаза, компаратор, ISI, BER.