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THE LINEARITY IMPROVEMENT METHOD IN CONTINUOUS TIME LINEAR EQUALIZERS

Nowadays, the usage of high-speed SERDES systems has increased, and the requirements for specific components have also risen. Data rates and clock frequencies have escalated to 224 *Gbps* and 16 *GHz*, respectively, leading to stringent requirements and greater challenges in their implementation.

One of the significant challenges is the system linearity. The SERDES system data path consists of a Serializer and Driver from the transceiver side, along with channels that connect the transceiver to the receiver. In the receiver, there is an Analog Front End (AFE) that includes a Continuous Time Linear Equalizer (CTLE) and an Analog-to-Digital Converter (ADC) for the final conversion to digital signals. Along this path, signal degradation occurs, depending on the signal frequency and channel losses. To address these issues, AFEs are employed, which typically consist of an attenuator, Continuous Time Linear Equalizers, and, in some cases, variable gain amplifiers.

It is important to address the linearity problems encountered within the AFE and ADC blocks. Linearity degradation, or poor linearity, can result in significant issues within the system, including incorrect data conversion and an decreasing Bit Error Rate (BER).

This paper addresses linearity issues within the Analog Front End (AFE), with a particular focus on the Continuous Time Linear Equalizer (CTLE). The primary nonlinear behavior stems from the CTLE, largely due to the utilization of various reactive components.

Keywords: continuous time linear equalizer, linearity, Serdes system, Analog Front End, Transmitter, Receiver, Transceiver.

Introduction. In modern high-speed SerDes systems, it is crucial to employ an Analog Front End (AFE) that equalizes the signal and mitigates losses incurred from the channel. AFEs typically comprise both passive and active components [1]. Passive components are utilized for signal attenuation, whereas active components, which often include a Continuous Time Linear Equalizer (CTLE), are employed for signal equalization [2]. The CTLE plays a pivotal role in compensating for signal degradation and enhancing overall system performance. The basic architecture of an AFE is illustrated in Fig. 1.

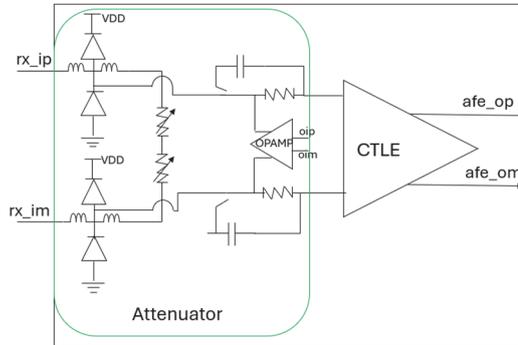


Fig. 1. Analog front end architecture

Continuous Time Linear Equalizers (CTLEs) are differential circuits that consist of a degeneration resistor, a degeneration capacitor, and output load resistors. The degeneration resistor and capacitor play crucial roles in the performance of the CTLE. The degeneration resistor helps to linearize the transconductance of the differential pair, thereby improving the linearity of the circuit. The degeneration capacitor, on the other hand, introduces a zero in the transfer function, which helps to boost high-frequency components of the signal, thereby compensating for high-frequency losses in the channel.

Modern CTLEs also incorporate inductors, which enhance bandwidth and gain [3]. The inclusion of inductors introduces additional poles and zeros in the transfer function, which can be strategically placed to further improve the equalization performance. The poles and zeros in the transfer function of the CTLE are critical in shaping the frequency response of the equalizer. Proper placement of these poles and zeros allows the CTLE to effectively compensate for the frequency-dependent losses and distortions introduced by the transmission channel, ensuring that the signal integrity is maintained [4]. The transfer function $H(s)$ of a CTLE typically includes terms for the degeneration resistor R_d , degeneration capacitor C_d , and inductors L . The general form can be expressed as (1):

$$H(s) = \frac{A(s)}{B(s)}, \quad (1)$$

where $A(s)$ and $B(s)$ are polynomials in s , the complex frequency variable. For a CTLE with inductors, the transfer function looks like this (2):

$$H(s) = \frac{s^2 + \omega_z s + \omega^2}{s^2 + \omega_p s + \omega p^2}, \quad (2)$$

where ω_z represents the frequency of the zero introduced by the degeneration capacitor and ω_p represents the frequency of the pole introduced by the inductors and other reactive components.

The basic architecture of a Continuous Time Linear Equalizer (CTLE) is illustrated in Fig. 2 [5].

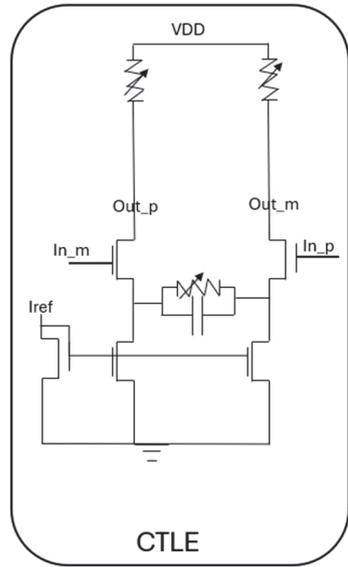


Fig. 2. Basic continuous time liner equalizer architecture

Problem description. Continuous Time Linear Equalizer with nmos input transistors (Fig.3) has been designed by SAED14 nm FinFet technology [6], and HSPICE simulations have been performed.

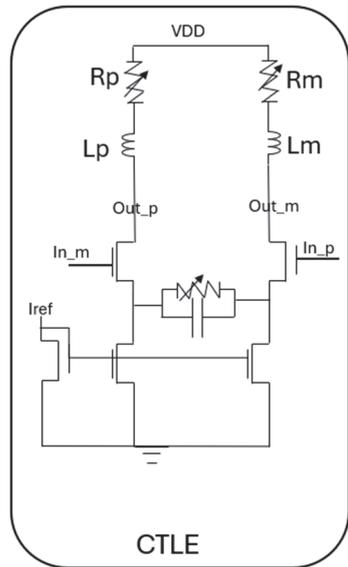


Fig. 3. The designed continuous time liner equalizer architecture

AC analyses were performed to determine the gain and bandwidth characteristics of the Continuous Time Linear Equalizer (CTLE), and the results are presented in Fig. 4.

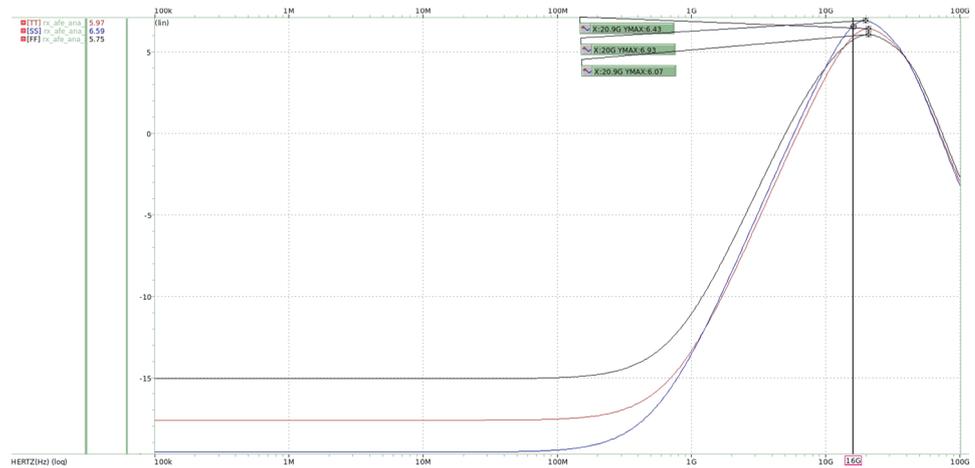


Fig. 4. CTLE AC analyses curves

Transient analyses were conducted to evaluate the linearity of the Continuous Time Linear Equalizer (CTLE). The applied signal frequency was set to be three times lower than the Nyquist frequency. Initially, the target design frequency for the circuit was established at 16 GHz, which is in accordance with PCIe 6 standards [7]. These analyses are crucial for understanding the dynamic behavior of the CTLE and ensuring that it performs effectively under varying signal conditions. By setting the target frequency at 16 GHz, the design aims to meet the stringent requirements of high-speed data transmission standards, thereby ensuring robust and reliable communication. The results of the transient analysis are depicted in Fig. 5, which illustrates the small-signal gain and linearity characteristics when the gain is 1 dB lower than its maximum value. This method is a common approach for measuring circuit linearity in SerDes systems. By analyzing the small-signal gain and linearity at this specific point, we can gain valuable insights into the performance and reliability of the CTLE under real-world operating conditions. Ensuring that the gain remains consistent and linear is essential for maintaining signal integrity and minimizing errors in high-speed data transmission.

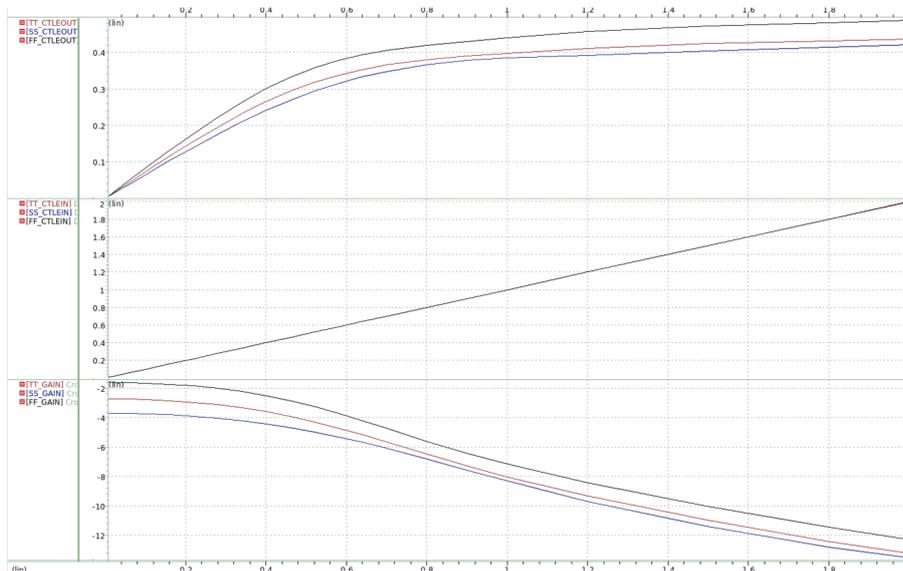


Fig. 5. CTLE Linearity curves, transient analysis results

It is essential to mention that both AC and transient analyses were conducted for the typical (TT), fast (FF), and slow (SS) corners. These analyses were performed with supply voltages of 1.2 V, 1.32 V, and 1.08 V, and at temperatures of 25°C, 125°C, and -40°C, respectively. This comprehensive approach ensures that the CTLE's performance is evaluated under various process, voltage, and temperature (PVT) conditions, providing a thorough understanding of its behavior across different scenarios. A summary of the AC and transient analyses for these three PVT conditions is provided in Table 1.

Table 1

The main parameters of CTLE

| Measurement | SS | TT | FF |
|----------------------------|-------|-------|-------|
| Peak frequency (GHz) | 20 | 20.9 | 20.9 |
| Gain_at_Nyquist (dB) | 6.59 | 5.97 | 5.75 |
| Peak_Gain (dB) | 6.93 | 6.43 | 6.07 |
| Gain at low frequency (dB) | -19.6 | -17.6 | -15.1 |
| Output Linearity (mV) | 269 | 276 | 311 |

Degeneration resistors are commonly employed to enhance linearity, which is a standard approach for amplifiers and equalizers [8]. However, based on the linearity numbers presented in Table 1, it is evident that linearity varies across corners by up to 10%, which is unacceptable for modern systems. Even with a supply voltage of 1.2 V, maintaining good linearity across all PVT corners is

challenging due to the small saturation margin of the input devices. This issue is more pronounced in the slow (SS) corners and other slow conditions. Ensuring consistent linearity across different process, voltage, and temperature conditions is crucial for the reliable performance of high-speed SerDes systems. Addressing these variations is essential to meet the stringent requirements of modern communication standards.

The proposed solution. One of the solutions proposed at the Irish Signals and Systems Conference involves replacing current source transistors with polyresistors. Additionally, a replica path was added to control the current through the CTLE, along with a 4-bit R2R digital-to-analog converter (DAC). The proposed solution has improved the linearity problem. However, it is not applicable to contemporary chips, as it increases the area of the CTLE by using resistors and adding the replica path with the R2R DAC [9].

The proposed solution do not include as many changes and additions to the CTLE. The proposed changes and solution are as follows. An additional transistor is incorporated into the main signal path m1 and m2, with its gates connected to the common mode voltage of the main data path signal, typically originating from the attenuator. The source of this transistors is connected to a current source, while the drain is connected to the outputs of the Continuous Time Linear Equalizer (CTLE). Furthermore, a new circuit has been added, consisting of controllable current mirrors and current sources [10]. This component can be any circuit that is independent or exhibits low variation across PVT conditions, such as a constant current source circuit. The basic circuit diagram of the updated scheme is shown in Fig. 6.

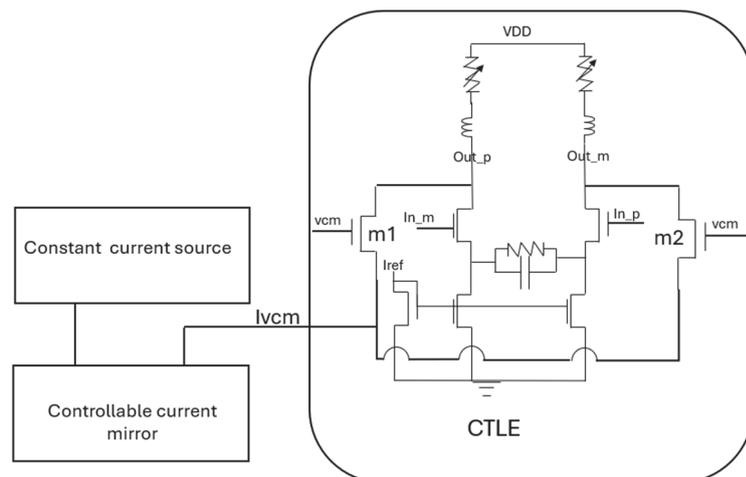


Fig. 6. The proposed circuit diagram

The newly added transistors in the differential paths, along with the programmable current mirrors, offer the capability of adjusting the current value through the main CTLE path. This adjustment results in a change in the drain voltage of the input devices, thereby increasing the saturation margin and enhancing the linearity values. This technique can also be employed to mitigate the linearity issues in cases of excessively high values, ensuring optimal CTLE performance without the noise associated with high-amplitude signals. By fine-tuning the current through the CTLE path, the design achieves improved signal integrity and reliability, which is crucial for high-speed data transmission systems. A controllable current mirror designed for three thermometric bits is utilized to cover a wide current range. This design allows for precise control over the current flowing through the CTLE path, enhancing the flexibility and performance of the equalizer. Additionally, the transistors connected to the CTLE outputs are chosen to be 20 times smaller to prevent any bandwidth degradation caused by device capacitance and metal connections. Figure 7 presents the implementation of the controllable current mirror at the transistor level.

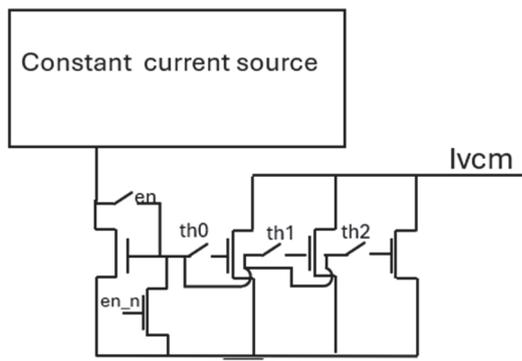


Fig. 7. Controllable current mirror

Results. In the initial step of the method verification, HSPICE simulations were conducted, and AC analysis was performed to assess the impact of the newly added transistors on the frequency response, particularly concerning bandwidth. Based on the results shown in Fig. 8, the impact of the newly added device is negligible, with the bandwidth degradation due to the device capacitance being less than 1%.

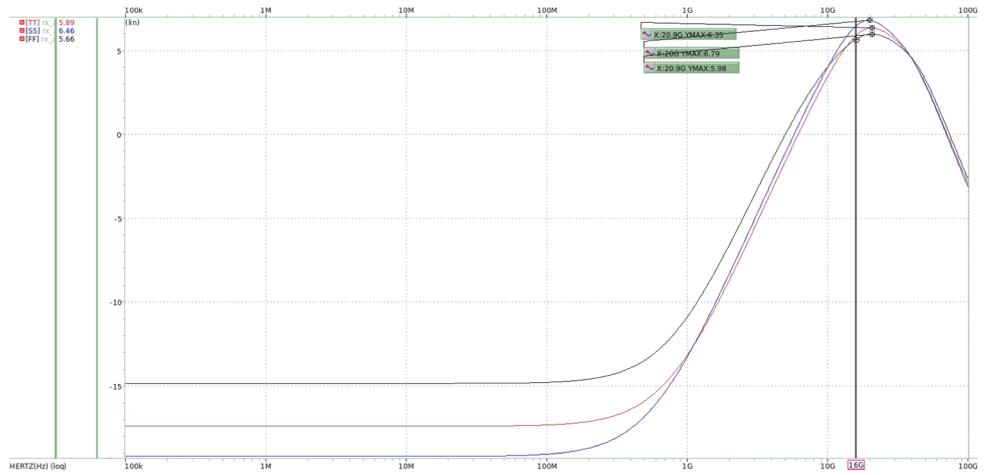


Fig. 8. CTLE AC response with the proposed method

In the next step, transient simulations were performed to identify the impact of linearity values with minimum and maximum current levels, which were controlled through three thermometric bits in the current mirror. Figure 9 shows the linearity curves for the SS corner, while the linearity values for the other two corners are presented in Table 2, along with other important parameters measured during the AC simulation.

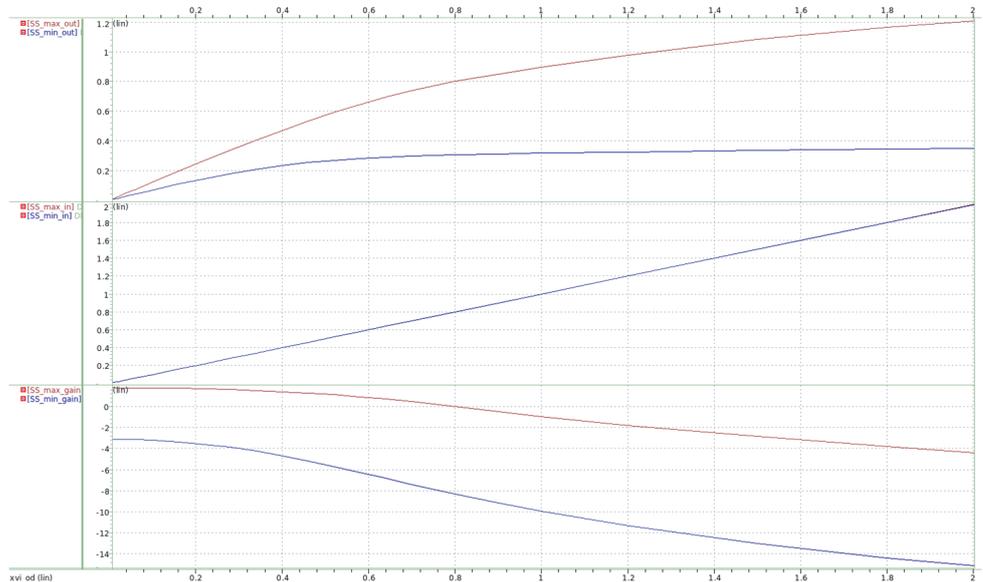


Fig. 9. Linearity curves for SS corner with minimum and maximum codes

Table 2.

The main parameters of CTLE with the proposed design

| Measurement | SS | TT | FF |
|---|-------|-------|-------|
| Peak frequency (GHz) | 20 | 20.9 | 20.9 |
| Gain_at_Nyquist (dB) | 6.46 | 5.89 | 5.66 |
| Peak_Gain (dB) | 6.79 | 6.35 | 5.98 |
| Gain at low frequency (dB) | -19.5 | -17.4 | -15.2 |
| Output Linearity with minimum code (mV) | 269 | 276 | 311 |
| Output Linearity with Maximum code (mV) | 680 | 698 | 731 |

Based on the results shown in Fig. 9 and Table 2, it is evident that the proposed solution addresses the linearity problems and increases the linearity values for the SS corner by up to 680 mV.

Conclusion. Continuous Time Linear Equalizer has been designed with the SAED 14nm FinFet technology. Poor linearity numbers are observed.

An architectural update has been proposed to enhance the linearity of the Continuous Time Linear Equalizer (CTLE). The results indicate that the linearity values for the worst corner are improved by up to 680 mV. Compared to other solutions, the proposed solution shows a 23% higher improvement. Although there is a slight increase in the circuit area and power consumption due to addition of transistors in the differential path and the implementation of a programmable current mirror, this increase is considered acceptable given the significant improvements achieved in linearity performance.

The SAED14 nm FinFet technology libraries have been used during the HSPICE simulations, and outputs have been exported by Galaxy Custom Designer tool.

REFERENCES

1. **Jang S., Lee J., Choi Y., Kim D.** Recent Advances in Ultrahigh-Speed Wireline Receivers With ADC-DSP-Based Equalizers // In IEEE Open Journal of the Solid-State Circuits Society.-2024.- Vol. 4.-P 290-304, doi: 10.1109/OJSSCS.2024.3506692 <https://ieeexplore.ieee.org/document/10767763>
2. A 16Gbps Programmable CTLE Design with Adjustable Gain / **J. Zheng, T. Shi, J. Wang, et al** // 2023 3rd International Conference on Electronic Information Engineering and Computer Science (EIECS).- Changchun, China, 2023.- P. 220–225, doi: 10.1109/EIECS59936.2023.10435457
3. **Zhang C., Wang Y., Xie M., Zhang D.** A 20Gbps CTLE with Active Inductor// 2022 7th International Conference on Integrated Circuits and Microsystems (ICICM).- Xi'an, China, 2.- P. 485–489, doi: 10.1109/ICICM56102.2022.10011348

4. **Zhang C., Xu Y., Zhang X., Wang H.** 50Gb/s High-Speed Serial Interface Receiver CTLE Equalization Circuit Design // 2023 8th International Conference on Integrated Circuits and Microsystems (ICICM).- Nanjing, China, 2023.- P. 417–421, doi: 10.1109/ICICM59499.2023.10365997
5. **Razavi B.** Design Techniques for CMOS Wireline NRZ Receivers Up To 56 Gb/s // IEEE Open Journal of the Solid-State Circuits Society.-2023.- Vol. 3.- P. 118–133, doi: 10.1109/OJSSCS.2023.3290551
6. **Melikyan V., Martirosyan M., Piliposyan G.** 14 nm Educational Design Kit: Capabilities, Deployment and Future // Small Systems Simulation Symposium.- Yerevan State University, 2018.- P. 37–41.
7. **López-Araiza K.G., Rangel-Patiño F.E., Ascencio-Blancarte J.E., Vega-Ochoa E.** A Multi-Stage CTLE Design and Optimization for PCI Express Gen6.0 Link Equalization // 2023 IEEE Latin American Electron Devices Conference (LAEDC).- Puebla, Mexico, 2023.- P. 1–4, doi: 10.1109/LAEDC58183.2023.10209113
8. **Han F., Yan J.** A Low-Power Receiver Equalization Circuit Based on Source Degeneration Structure // 2024 4th International Conference on Electronic Information Engineering and Computer Communication (EIECC).- Wuhan, China, 24.- P. 142–145, doi: 10.1109/EIECC64539.2024.10929589
9. **Singh P., Walia R., Nagulapalli R., Sakare M.** A Linearity Improved Equalizers for Short-Channel Communication Links, // 2024 35th Irish Signals and Systems Conference (ISSC).- Belfast, United Kingdom, 2024.- P. 1–5, doi: 10.1109/ISSC61953.2024.10603313
10. A Current DAC Based Current Generator with Fourth-Order Current-Mode Filter for Electrical Impedance Tomography / **J. Li, Y. Wu, D. Jiang et al** // 2024 IEEE International Symposium on Circuits and Systems (ISCAS).-Singapore, 2024.- P. 1–4, doi: 10.1109/ISCAS58744.2024.10558679

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Մ.Ա. ԽԱՉԱՏՐՅԱՆ

ԱՆԸՆԴՀԱՏ ԳԾԱՅԻՆ ՀԱՄԱՀԱՐԹԵՑՄԱՆ ՀԱՆԳՈՒՅՑՈՒՄ ԳԾԱՅՆՈՒԹՅԱՆ ԼԱՎԱՑՄԱՆ ՄԵԹՈՂ

Ներկայումս բարձր արագությամբ SERDES համակարգերը լայնորեն օգտագործվում են, և դրանց բաղադրիչներին առաջադրվող պահանջները խստացել են: Տվյալների փոխանցման արագությունները և տակտային ազդանշանների հաճախությունները հասել են 224 *Գբիթ/վրկ* և 16 *ԳՀց*-ի համապատասխանաբար, որը հանգեցնում է սահմանափակումների խստացման և մեծ մարտահրավերների առաջացման դրանց իրականացման գործընթացում: Կարևոր մարտահրավերներից մեկը համակարգի գծայնությունն է: SERDES համակարգի տվյալների ուղին բաղկացած է հաջորդականացնող հանգույցից, ելքային տանող հանգույցից և հաղորդիչ հանգույցից, ինչպես նաև հոսքուղիներից, որոնք կապում են հաղորդիչ համակարգը ընդունիչ համակարգի հետ: Ընդունիչում տվյալներն անցում են ընդունիչ հանգույցով (AFE), որը կազմված է անընդհատ գծային համահարթեցնող հանգույցից (CTLE) և

անալոգաթվային կերպափոխիչից (ADC)՝ վերջնական թվային ազդանշանների փոխակերպման համար: Այս ուղու ընթացքում ազդանշանի վատթարացում է տեղի ունենում՝ կախված ազդանշանի հաճախությունից և հոսքուղու պատճառով առաջացած կորուստներից: Այդ խնդիրները լուծելու համար օգտագործվում են ընդունիչ հանգույցները, որոնք սովորաբար բաղկացած են ճնշիչ հանգույցից, անընդհատ գծային համահարթեցնող հանգույցից և, որոշ դեպքերում, փոփոխական ուժեղացման գործակցով ուժեղարարներից: Կարևոր է անդրադառնալ ընդունիչ հանգույցում և անալոգաթվային կերպափոխիչում հանդիպող գծայնության խնդիրներին: Գծայնության վատթարացումը կամ վատ գծայնությունը կարող են հանգեցնել համակարգում նշանակալի խնդիրների, ներառյալ տվյալների սխալ փոխակերպման և բիթի սխալի տեմպի (BER) նվազման: Անդրադարձ է կատարվել ընդունիչ հանգույցի գծայնության խնդիրներին, հատկապես առաջացող անընդհատ գծային համահարթեցնող հանգույցի պատճառով: Հիմնական ոչ գծային վարքագիծն առաջանում է անընդհատ գծային համահարթեցնող հանգույցում, հիմնականում տարբեր ռեակտիվ բաղադրիչների օգտագործման պատճառով:

Առանցքային բաներ. Անընդհատ գծային համահարթեցնող հանգույց, գծայնություն, Serdes համակարգ, ընդունիչ հանգույց, Հաղորդիչ համակարգ, ընդունիչ համակարգ, հաղորդիչ-ընդունիչ:

С.А. ХАЧАТРЯН

МЕТОД УЛУЧШЕНИЯ ЛИНЕЙНОСТИ В ЛИНЕЙНЫХ УСИЛИТЕЛЯХ НЕПРЕРЫВНОГО ВРЕМЕНИ

В настоящее время наряду с широким использованием высокоскоростных систем SERDES увеличились также требования к конкретным компонентам. Скорости передачи данных и частоты тактового сигнала достигли 224 Гбит/с и 16 ГГц соответственно, что привело к большим вызовам при их реализации. Одной из значительных проблем является линейность системы. Путь данных системы SERDES состоит из сериализатора и драйвера со стороны передатчика, а также каналов, которые соединяют передатчик с приемником. В приемнике находится аналоговый фронт-энд (AFE), который включает в себя линейный эквалайзер непрерывного времени (CTLE) и аналого-цифровой преобразователь (ADC) для окончательного преобразования в цифровые сигналы. На этом пути происходит деградация сигнала, зависящая от частоты сигнала и потерь в канале. Для решения этих проблем используются AFE, которые обычно состоят из аттенюатора, линейных эквалайзеров непрерывного времени и, в некоторых случаях, усилителей с переменным коэффициентом усиления. Важно решить проблемы линейности, возникающие в блоках AFE и ADC. Деградация линейности, или плохая линейность, может привести к значительным проблемам в системе, включая неправильное преобразование данных и снижение коэффициента ошибок битов (BER). В данной статье рассматриваются проблемы линейности в аналоговом фронт-энде (AFE) с особым акцентом на линейный эквалайзер непрерывного времени (CTLE). Основное нелинейное поведение возникает из-за CTLE, главным образом из-за использования различных реактивных компонентов.

Ключевые слова: линейный эквалайзер непрерывного времени, линейность, система Serdes, аналоговая входная часть, передатчик, приемник, трансивер.