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A HIGH PRECISION CMOS CURRENT SOURCE WITH EXTERNAL COMPONENTS

This paper presents a novel design technique aimed at improving the accuracy of on-chip reference current sources. The proposed approach leverages innovative circuit design methodologies to achieve enhanced precision and reliability in reference current generation. The proposed design technique offers a significant advancement in the field of on-chip reference current sources, providing a robust and accurate solution for various applications. The novel design technique has far-reaching implications for various applications, including analog-to-digital converters, digital-to-analog converters, and other mixed-signal systems. The improved accuracy and precision of on-chip reference current sources enabled by this approach can significantly enhance the overall performance and reliability of these systems. The proposed technique has been implemented in the design of on-chip reference current source circuit in 14 nm FinFet technology. Spice simulations performed for the developed circuit show less than 7% variation of the reference current in the -40...125^{0}C temperature range considering the process variations in ±3 sigma range.

***Keywords**:* on-chip current source, current generators, calibration, initial current.

Introduction. In contemporary electronic systems, the need for high-precision and thermally stable current sources has become paramount, particularly in applications such as sensor signal conditioning, analog signal processing, and high-accuracy measurement systems [1]. High-precision current sources are indispensable components that deliver a constant current output with minimal deviation, thereby ensuring reliable performance in sensitive electronic circuits [2-4]. A crucial technical specification for modern complementary metal-oxide-semiconductor (CMOS) integrated circuits (ICs) is to guarantee high stability of the primary parameters, independent of ambient temperature, supply voltage, and technology-related deviations [5-7]. The main parameters of the elements can deviate from their typical characteristics by values ranging from tens of percent to multiples [1]. To mitigate these variations, high-precision current sources are designed to maintain a consistent output despite fluctuations in load resistance or supply voltage, thereby enhancing the overall accuracy of the system[8,9]. High-precision current sources are distinguished by their low noise, high stability, and excellent temperature

coefficients, rendering them suitable for applications in instrumentation, telecommunications, and industrial automation. The proliferation of portable devices has led to stringent requirements for energy consumption and IC surface area, thereby limiting the use of circuits with large surface areas and high energy consumption [2,3]. The design of high-precision current sources can be accomplished through various methods, including the utilization of operational amplifiers, transistor-based configurations, and integrated circuit solutions. Each approach presents distinct advantages and challenges, contingent upon the specific requirements of the application [4,5]. The availability of precision voltage sources does not guarantee the design of stable current sources. This is because the combination of resistance and a reference voltage source in the MOS structure is susceptible to resistance variation [6,7]. As technology advances, the integration of high precision current sources into compact and efficient designs continues to evolve, enabling new possibilities in the fields of electronics and instrumentation.

Statement of the problem. In the realm of electronic circuit design, achieving high precision in current sourcing remains a significant challenge. To mitigate the effects of temperature variations on the reference current, a mathematical model is proposed. This model enables to make accurate prediction and compensation of temperature-induced deviations, ensuring a stable and reliable reference current. The mathematical model takes into account the temperature-dependent behavior of the current, allowing for accurate prediction of current variations across different temperatures (Fig. 1). The model's ability to compensate for temperature variations ensures that the reference current remains accurate across a wide range of temperatures. The accurate and stable reference current provided by the mathematical model allows optimal system performance, even in the presence of temperature variations.

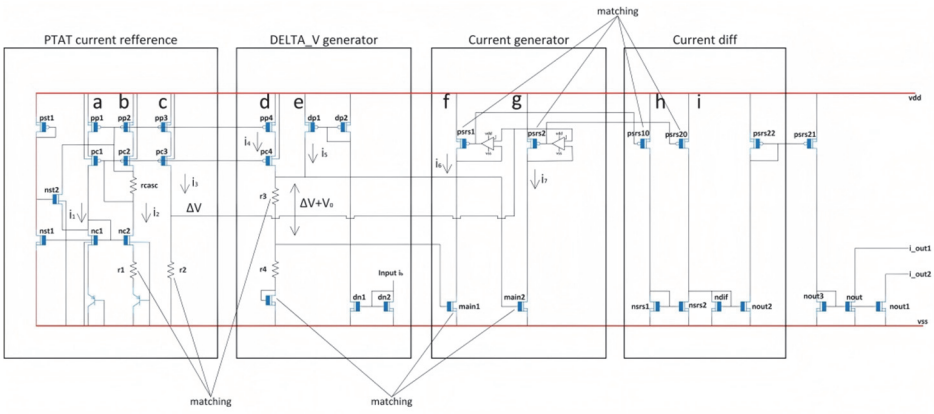

Fig. 1. The block diagram of a high-precision DC current source

Furthermore, the main two N-MOS transistors are deliberately sized to be larger than nominal to ensure robustness against fabrication-related deviations. In general, the implementation of two N-MOS transistors with increased dimensions can be an effective strategy to mitigate the effects of process variations encountered during semiconductor fabrication. This approach aims to enhance the robustness and reliability of the circuit by ensuring that the transistors can maintain their performance characteristics despite fluctuations in manufacturing parameters. However, while this method may provide a degree of improvement in performance consistency, it is not considered an optimal solution. The enlargement of transistor dimensions can lead to several trade-offs, including increased power consumption, larger die area, and potentially slower switching speeds due to increased capacitance. Therefore, while utilizing larger NMOS transistors can serve as a practical measure to address the process variations, it is essential to explore alternative design methodologies and optimization techniques that can achieve a more balanced performance profile. These may include the use of adaptive biasing, advanced layout techniques, or the incorporation of process compensation circuits, which can provide enhanced performance without the drawbacks associated with simply increasing the transistor size.

The proposed solution. The proposed method works by utilizing a simple current source and capacitor and a quartz or PLL generated stable frequency clock to provide a precise timing reference.

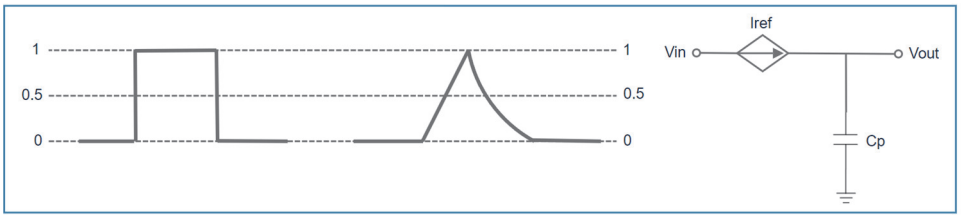

Fig. 2. A simple current source and capacitor in series

The equation for the output voltage in the proposed method for improving the accuracy of on-chip reference current sources is a crucial aspect of the design. The output voltage, Vout(t), is given by the following equation (Fig. 2):

$$Vout = \frac{Iref \times t}{C}.$$

The time required to charge the capacitor to a voltage of 0.5 V is expressed as:

$$t = \frac{C \times Vref}{Iref},$$

where Iref represents the reference current that requires calibration.

Consider a scenario in which the capacitance (C) is specified as 57 *pF*, and the reference voltage Vref is set to 0.5 *V*. In this case, the capacitor will be charged utilizing a current source. Given that the clock period (T) is constant, the reference voltage Vref serves as the output voltage of a bandgap reference circuit, which is characterized by its high accuracy and stability. The capacitor in question exhibits high performance with respect to variations in temperature, supply voltage, and manufacturing process discrepancies. This stability is crucial for ensuring that the charging process remains consistent and reliable under varying operational conditions. The charging of the capacitor can be mathematically described by the relationship between the current supplied by the current source and the voltage across the capacitor. The precise calibration of the current source is essential to achieve the desired voltage level of 0.5 *V* across the capacitor within the specified time frame, thereby ensuring optimal performance of the overall system. This choice should however be adjusted based on two factors. The comparator must have high gain and low offset at the chosen reference level, and the bigger the capacitor area, the smaller its mismatch variation.

The block diagram of the current source consists of the following blocks:

Reference current generator which generates a stable reference current that is insensitive to temperature and supply voltage variations, digital controller which generates control signals to regulate the output current, current mirrors and capacitor with high accuracy (Fig. 3).

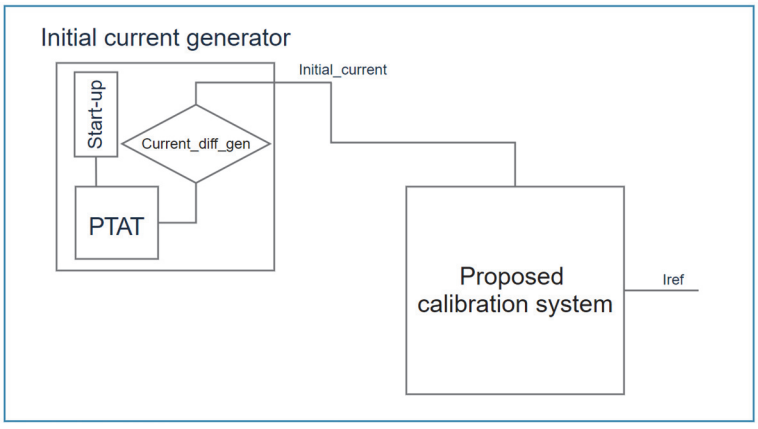

Fig. 3. The block diagram of the proposed high-precision current source

The proposed system incorporates a digitally programmable current source circuit, an 8-bit digital controller, a high-speed comparator, and an integrated capacitor. The current source transistors, highlighted in red, comprise eight binary-weighted parallel cascade current sources, with each branch controlled by a distinct

digital bit, thereby providing a programmable current value with high accuracy and resolution. The digital controller is a Mealy finite state machine (FSM) (Fig. 4).

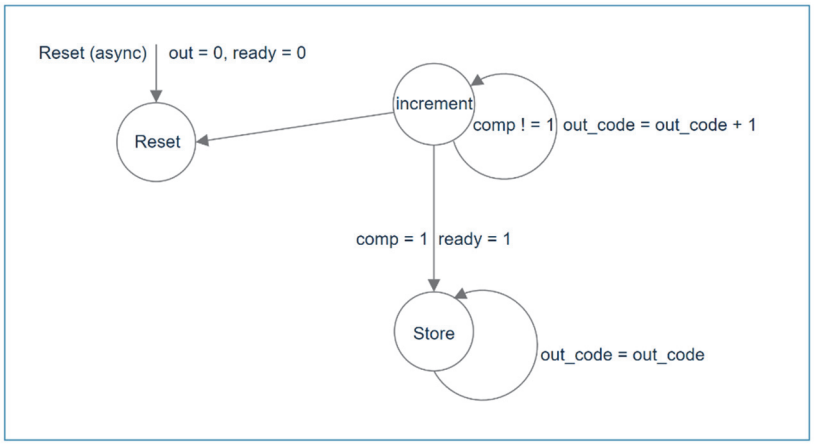

Fig. 4. The Mealy machine base for the digital controller

The controller clk, reset and comp as inputs and code_up[7:0], code_dn[7:0] and ready as outputs. It starts with a default code of zero, meaning that all the parallel current sources are disabled and the cap is charged with the current coming from internal current generator block. If the cap voltage reaches the desired value sooner than 128 input clock cycles, which is assumed to be a 128 *MHz* clock, then the current is larger than needed, dn_code is increased, cap voltage is reset and it starts charging with a smaller current. If the cap voltage reaches the desired value later than 128 input clock cycles then the current is smaller than needed, up_code is increased and the cap is charged with a larger current. This goes on until it takes exactly 128 clock cycles to charge the cap. After that the calibration process is stopped and the digital controller outputs 1 at its ready output and the code is held constant. Full implementation of the proposed method (Fig. 5).

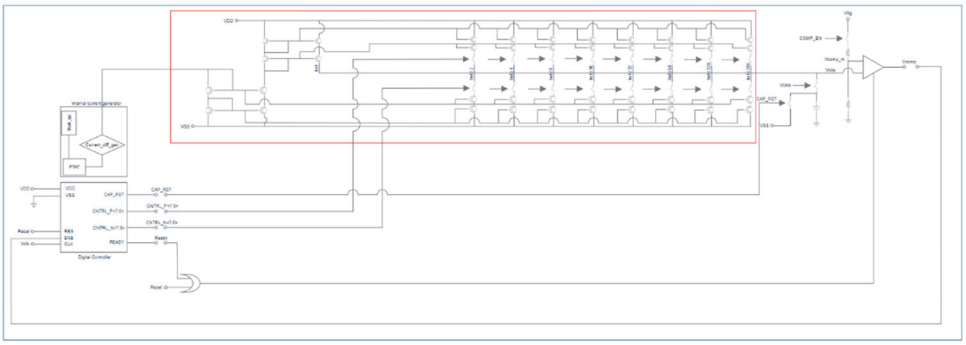

Fig. 5. The proposed current source and calibration system

The current source transistors are connected to the capacitor with switches facing the clock so that the parasitic capacitances don't add up and skew the calibration. To avoid wasting power during the idle period of operation, the comparator and the resistive divider that provides reference are disabled with COMP_EN signal. This signal is derived from ¬(Ready ∨ Reset) and the comparator will only be enabled when both inputs are passive. The designed circuit requires 128 *Mhz* input clock. The capacitance value with these frequency and resistance in mind will be 57 *pF*, which is roughly 10200 um^2 in this process:

$$C = \frac{28.5 \times 10^{-6} \times 10^{-6}}{0.5} = 5.7 \times 10^{-11}\ F.$$

The digital controller is implemented in Verilog and synthesized and verified using Design Compiler and VCS respectively [6,7]. Physical design is implemented using IC Compiler 2 tool [8]. The rest of the proposed system consists of analog blocks and is implemented in Custom Compiler using schematic and layout editors. The capacitance is chosen to be significantly larger than the rest of the circuitry so that the parasitic capacitances will not have significant contribution to the total capacitance. The layout is designed according to all recommended design rules in order to minimize the variation and offset. The switches in the resistance bank are connected to the clock signal, while the other end is connected to the capacitor so as to minimize the added parasitic capacitance on the Vcap node.

Simulation results. To substantiate the findings derived from the theoretical analysis, a series of SPICE simulations have been conducted specifically for the 14 *nm* FinFET technology node. The dependence of the reference current of initial current generator on various stabilization factors has been thoroughly analyzed and evaluated. This investigation encompasses a comprehensive examination of the key parameters that influence the stability and accuracy of the reference current within the circuit design. The results show that the reference current variation for the -40...125^{0}C temperature range considering the process variations in ±3 sigma range and supply voltage variation in ±10% range is less than 12% (Fig. 6).

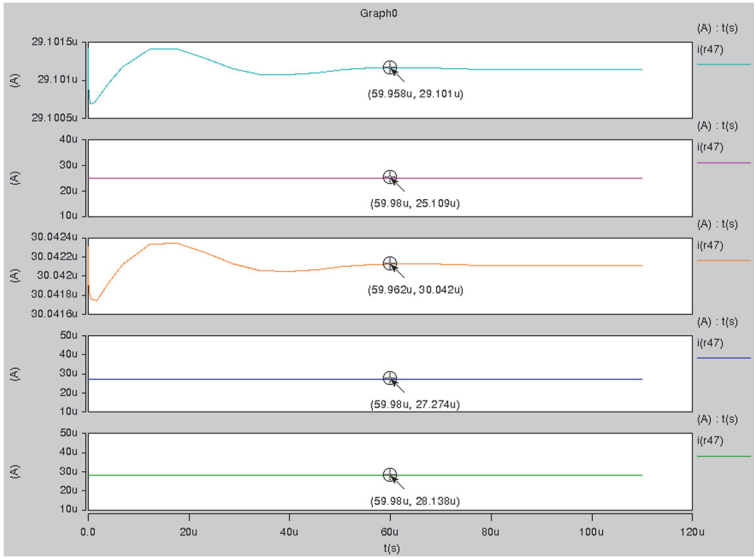

Fig. 6. The dependence of the output current on temperature, as well as supply voltage and technological changes

The simulation of the proposed circuit, utilizing a digital controller, is conducted under typical operating conditions. In this specific scenario, it is observed that the initial current output is measured at 15 μA (Fig. 7).

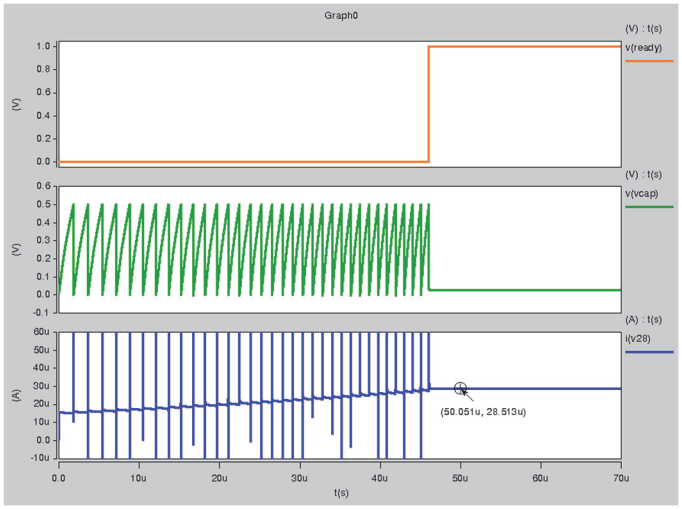

Fig. 7. The dependence of the reference current on the ambient temperature variation

The results show that the reference current variation for the -40...125^{0}C temperature range considering the process variations in ±3 sigma range and supply voltage variation in ±10% range is less than 7% (Fig. 8).

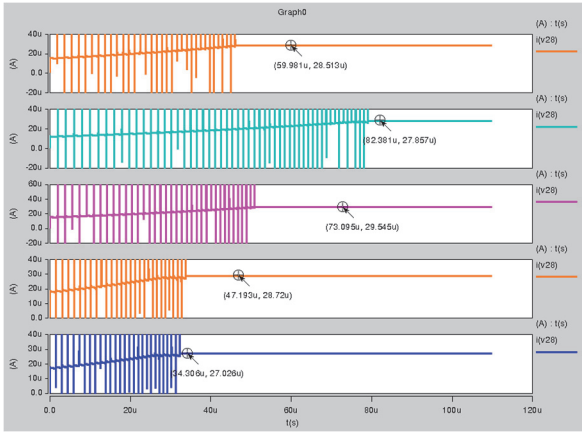

Fig. 8. The dependence of the output current on temperature, as well as supply voltage and technological changes

In summary, the findings confirm that the reference current variation remains below 7% across the specified temperature range, considering both process and supply voltage variations. This performance underscores the circuit's reliability and suitability for integration into a wide range of electronic applications, where maintaining accurate current levels is essential for optimal functionality.

Conclusion

In this paper, we present a novel design technique for on-chip current sources that has been proposed meticulously designed, and subjected to comprehensive simulation analysis. The results of these simulations indicate that the newly developed circuit is capable of delivering precise reference currents while maintaining operational stability across a wide temperature range of -40...125^{0}C and accommodating supply voltage variations of ±10%. The innovative design approach focuses on enhancing the accuracy and reliability of the current source, addressing common challenges associated with temperature-induced drift and supply fluctuations. The simulations demonstrate that the proposed circuit can effectively limit the variation in output current to approximately ±6%, thereby ensuring that the reference currents remain stable and within acceptable limits under varying environmental and operational conditions. The primary limitation of the proposed technique lies in the reliance on a digital controller, which introduces certain complexities and potential drawbacks in the overall circuit design. The integration of a digital controller necessitates additional components and circuitry, which can complicate the design process and may require careful consideration of timing and synchronization issues. Both requirements are deemed acceptable, particularly when considering the more relaxed specifications typically associated with certain segments of integrated circuits ICs.

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1-National Polytechnic University of Armenia, Institute of Radio Phisics and Electronics. “Synopsys Armenia” CJSC.

2-National Polytechnic University of Armenia. “Synopsys Armenia” CJSC.

3-Europen University of Armenia, “Synopsys Armenia” CJSC. 4- Disgo Armenia CJSC. 5-RA Defence Ministry Academy named after V. Sargsyan. The material is received on 14.01.2025.

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ԱՐՏԱՔԻՆ ԲԱՂԱԴՐԻՉՆԵՐԻ ԿԻՐԱՌՄԱՄԲ ԲԱՐՁՐ ՃՇԳՐՏՈՒԹՅԱՆԲ ԿՄՕԿ ՀՈՍԱՆՔԻ ԱՂԲՅՈՒՐ

Առաջարկվել է ներբյուրեղային հոսանքի աղբյուրների ճշգրտության բարձրացման նոր եղանակ։ Առաջարկվող եղանակով կիրառվում են սխեմաների նախագծման նորարարական մեթոդներ՝ ներբյուրեղային հոսանքի աղբյուրների ճշգրտության և հուսալիության

բարձրացման նպատակով: Առաջարկվող եղանակը զգալի առաջընթաց է ապահովում ներբյուրեղային հոսանքի աղբյուրների ոլորտում՝ ապահովելով կայուն և ճշգրիտ լուծում տարբեր համակարգերի համար: Բարձր ճշգրտությամբ ներբյուրեղային հոսանքի աղբյուրները զգալի ազդեցություն ունեն տարբեր համակարգերում, ինչպիսիք են անալոգաթվային և թվանալոգային ձևափոխիչները և այլ խառը ազդանշանային համակարգեր: Առաջարկվող եղանակով նախագծված ներբյուրեղային հոսանքի աղբյուրը կարող է զգալիորեն բարձրացնել թվարկված համակարգերի ֆունկցիոնալությունը և հուսալիությունը: Առաջարկված եղանակն իրականացվել է 14նմ FinFet տեխնոլոգիական գործընթացով՝ ներբյուրեղային հենակային հոսանքի աղբյուրի մշակման համար: Կատարված spice նմանակման արդյունքում, ջերմաստիճանի -40. . .125°C միջակայքում, տեխնոլոգիական գործընթացի ±3 սիգմա շեղումների դեպքում, մշակված սխեման ապահովել է հենակային հոսանքի 7%-ից պակաս շեղումներ:

Առանցքային բառեր. ներբյուրեղային հոսանքի աղբյուր, հոսանքի գեներատոր, հենակային հոսանք:

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ИСТОЧНИК КМОП ТОКА ВЫСОКОЙ ТОЧНОСТИ С ИСПОЛЬЗОВАНИЕМ ВНЕШНИХ КОМПОНЕНТОВ

Представлена новая технология проектирования, направленная на повышение точности интегрированных источников опорного тока. Предлагаемый подход использует инновационные методы проектирования схем для достижения повышенной точности и надежности при генерации опорного тока. Предложенный метод проектирования обеспечивает значительный прогресс в области внутрикристальных источников опорного тока, предоставляя надежное и точное решение для различных приложений. Новая технология проектирования имеет далеко идущие последствия для различных приложений, включая аналого-цифровые преобразователи, цифроаналоговые преобразователи и другие системы со смешанными сигналами. Повышенные точность и достоверность встроенных в кристалл источников опорного тока, обеспечиваемые этим подходом, могут значительно повысить общую производительность и надежность этих систем. Предложенный метод был реализован при проектировании схемы опорного источника тока на кристалле, выполненном по технологии FinFet 14 *нм*. Моделирование Spice, выполненное для разработанной схемы, показало менее 7% отклонения опорного тока в диапазоне температур -40...125^{0}C с учетом отклонений процесса в диапазоне ±3 сигма.

Ключевые слова: внутрикристальный источник тока, генераторы тока, калибровка, начальный ток**.**