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A NOVEL PVT-TRACKING POWER SUPPLY DETECTION CIRCUIT FOR RELIABLE LEVEL SHIFTER OPERATION IN MULTI-VOLTAGE ICs

In modern integrated circuits (ICs) operating across multiple supply voltage domains, precise power sequencing is essential to ensure reliable system initialization and prevent undefined behavior during power-up and transient conditions. Power-On Reset (POR) and Power-Good (PG) circuits are commonly employed to monitor supply voltages and signal when power levels are stable and within operational ranges. These signals gate critical functions such as level shifter enabling, state machine initialization, and downstream circuit activation. However, the conventional design of POR and PG circuits often involves significant overdesign to guarantee robust performance across the wide range of Process, Voltage, and Temperature (PVT) variations present in advanced semiconductor manu-facturing nodes. A novel power detection approach is proposed with simplified design and PVT resilient behavior that ensures the reliable operation of the level shifting circuits with defined failure states. The proposed methodology is implemented and verified using the SAED 14*nm* FinFET technology.

Keywords: power detection, reliability, level shifter, multi-voltage IC.

Introduction. In mixed-signal and analog integrated circuits, level shifters play a crucial role in converting low-voltage digital control signals into high-voltage signals required for driving key analog functions [1-3]. These level shifters interface between distinct voltage domains, ensuring that digital control logic can effectively interact with high-voltage analog circuitry (Fig. 1) [4-6].

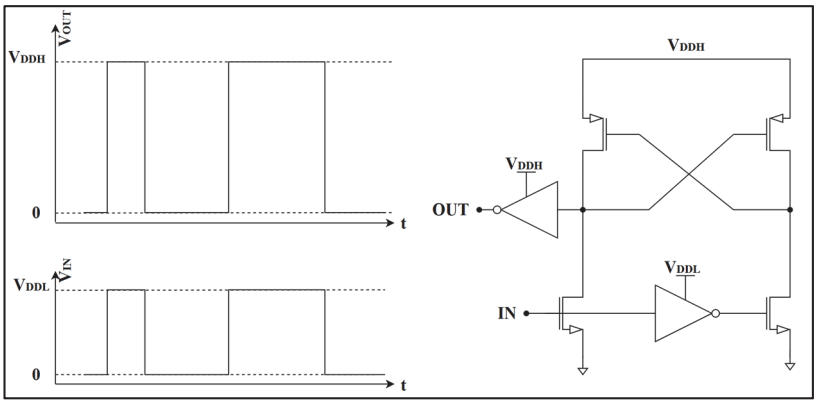

Fig. 1. The classical level shifter topology (right) and its normal operation (left)

However, for level shifters to operate correctly, both the high-voltage supply (VDDH) and low-voltage supply (VDDL) must remain within a specific operational range [7]. If either voltage deviates too far from its intended level, the level shifter can enter an undefined state, where the output does not reliably correspond to the input. This can lead to scenarios where a logic '0' at the input results in a logic '1' at the output, inadvertently enabling sensitive analog blocks and causing unpredictable circuit behavior.

Traditional level shifters are highly sensitive to PVT variations due to their simple design; hence the failure conditions can vary significantly (Fig. 2). Adjusting the Power-Good level for the worst failure case is generally a necessary compromise of design efficiency in favor of reliability.

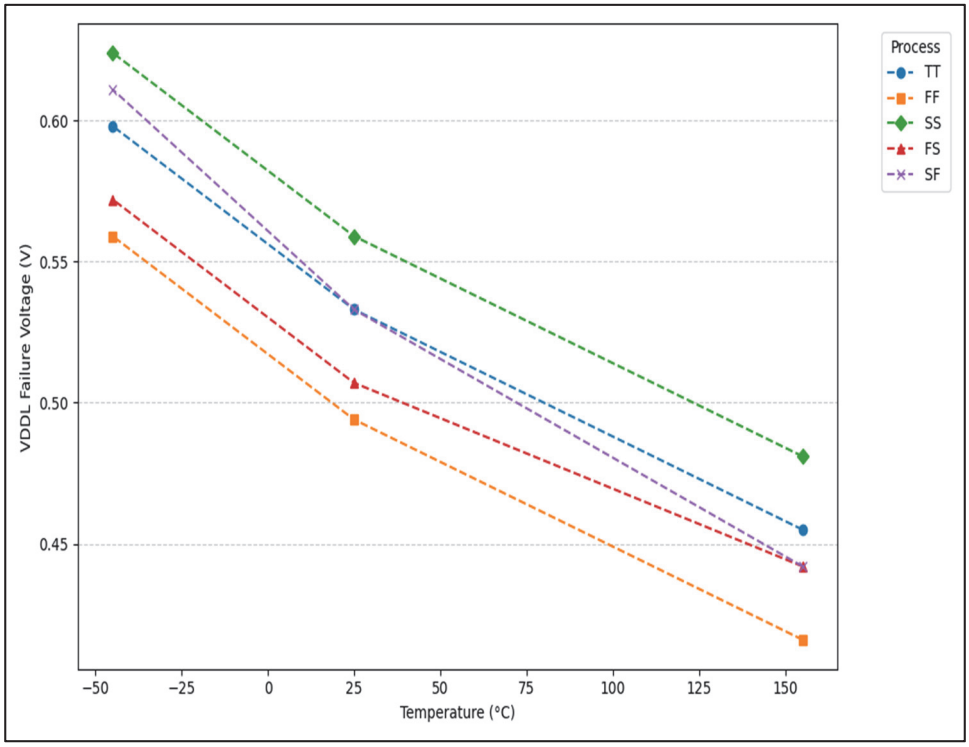

Fig. 2. VDDL failure voltage of the level shifter for VDDH=1.8V

To mitigate these risks, it is necessary to establish a well-defined operating range for both VDDH and VDDL that guarantees the correct functionality of level shifters under all conditions. A robust power detection system must be designed to monitor these supply voltages and ensure that level shifters are only enabled when both VDDH and VDDL are within their reliable operational range [8,9]. When the supply conditions fall outside this range - whether due to power-up sequencing

variations, brownout events, or transient power glitches - the power detection circuit must disable the level shifters, preventing them from outputting erroneous signals. This ensures that, regardless of power sequencing order or supply fluctuations, the level shifters will either function correctly or remain safely disabled, thereby enhancing the reliability of the entire analog subsystem and preventing unintended activation of sensitive analog circuits.

The proposed approach. To minimize the overhead, the power detection system can utilize a detection level with a negative temperature slope. This will offer less overcompensating detection at higher temperatures, while still maintaining large overhead at fast process corners (Fig. 3) [10,11].

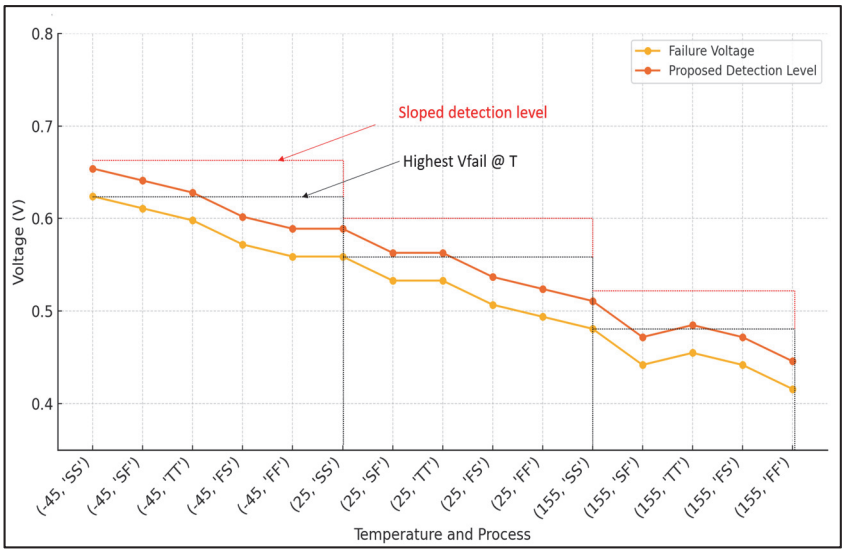

Fig. 3. Failure voltage and the proposed PVT tracking detection level

Following not only temperature but also process variations is necessary in order to minimize the voltage overhead completely. The proposed circuit does this by introducing minimal modifications in the existing level shifter circuit (Fig. 4). The modifications should ensure the predictable failure state of the circuit, whilst maintaining the PVT response of the level shifter.

The addition of N3 adds slight asymmetry in the DC characteristics of the circuit and ensures that it will fail at marginally higher voltages than the symmetric level shifter structure. N4 and N5 thick gate oxide transistors ensure that the N1, N2 and N3 core devices are not subjected to overvoltage stress. The P<100:7> chain of p-channel transistors in series acts as a weak pull-up path for the pre-buffered output. The gates of these devices are controlled by VDDL, so that as the difference between high and low supply voltages grow – the pull up path

conductance increases and accelerates the PG release. The input signal can either be tied high to VDDL or controlled by an enable signal. The design is implemented in SAED 14nm FinFET technology but the proposed approach is not unique to this process and can be used universally [12].

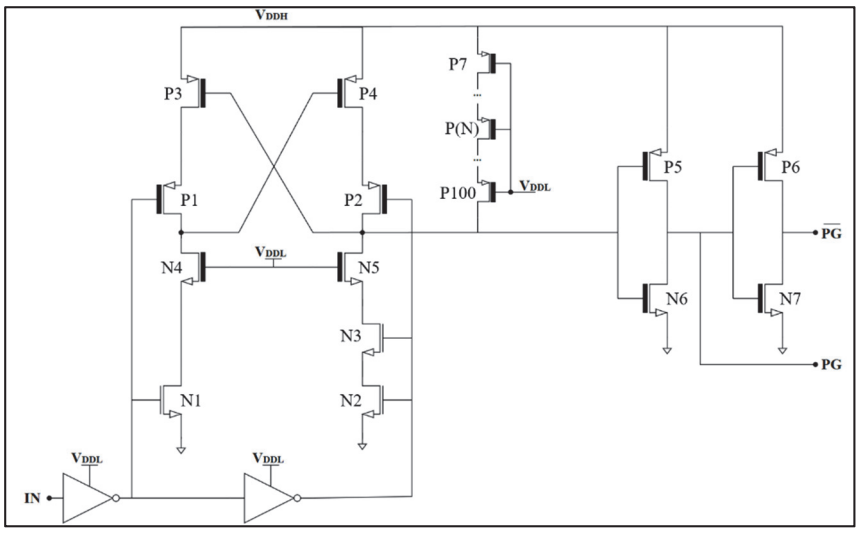

Fig. 4. The proposed power detection circuit

Analyzing the DC response of two identical level shifters—one standalone, without power detector gating, and the other with PG enable—shows drastic differences in current consumption in near-failure states (Fig. 5).

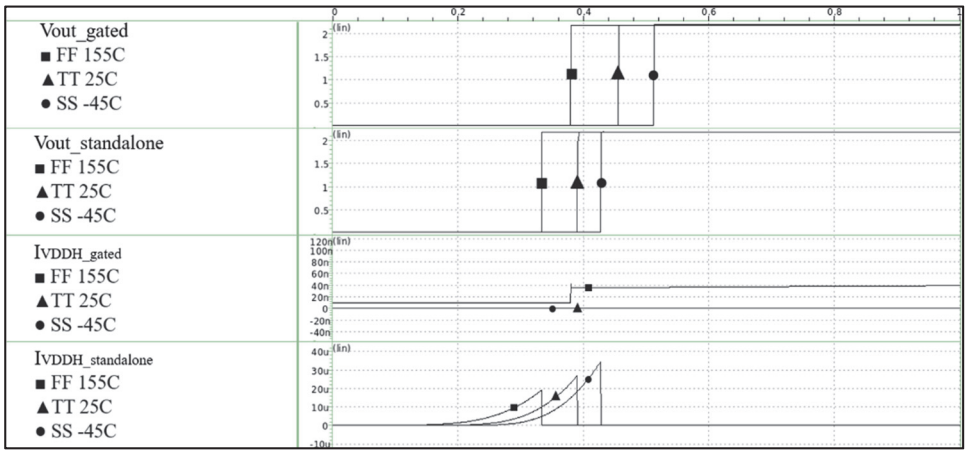

Fig. 5. DC response of standalone and gated level shifters

Simulations are performed across PVT conditions to ensure that the actual detection levels match with the proposed behavior from Figure 3. The results show

the desired PVT tracking behavior and enough headroom to account for mismatch variations (Fig. 6).

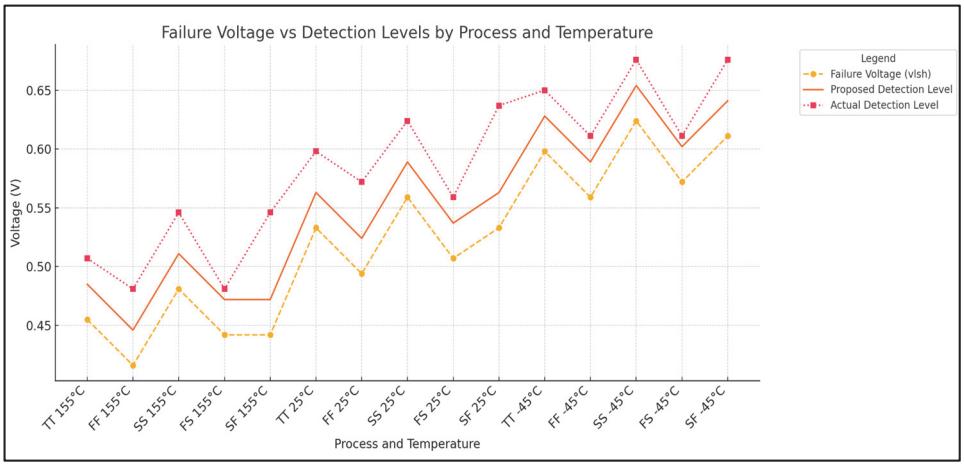

Fig. 6. Failure voltage, the proposed and simulated detection levels

Monte Carlo statistical mismatch simulations are performed using sigma amplification targeting 5σ coverage. This ensures over 99.9999% yield or less than 1 defective part per million. The difference between failure detection voltage and level shifter failure voltage are positive in all iterations (Fig. 7).

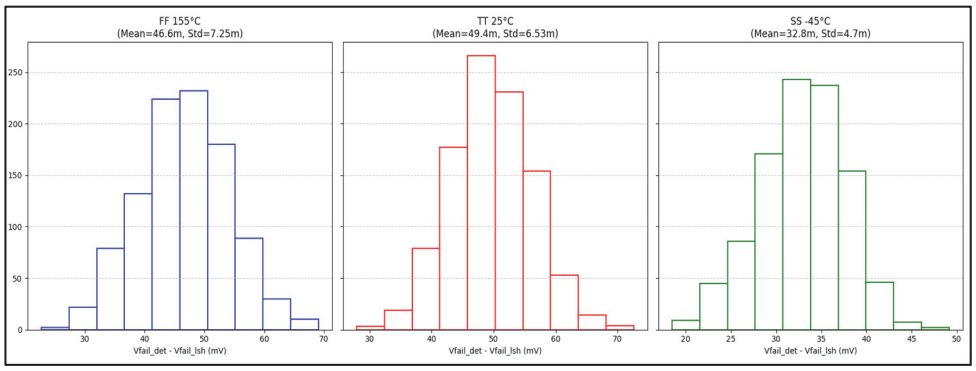

Fig. 7. 5σ mismatch simulation results

Results. The implemented design achieves the desired PVT tracking behavior, accurately detecting failure conditions and gating the level shifters before they get the chance to form an erroneous output. This is achieved by occupying an area roughly the size of three level shifters. Considering the commonality of level shifters in mixed-signal IPs, the addition of the detection circuit will not be a noticeable footprint increase next to the dozens if not hundreds of level shifters.

The main downside of the proposed approach is that it consumes static current during normal operation, meaning that the power supplies are within the operational range and PG=1 (Table).

Table

Power Timing and Area of the proposed power detection circuit

Process Corner	Area (μm^2)	Delay (ps)	Power (μW)
Fast	180	18.2	12.4
Nominal		30.1	7.2
Slow		74.8	3.8

Conclusions. A novel PVT tracking power supply detection circuit is proposed and implemented in the SAED 14*nm* FinFET technological process. The proposed circuit consumes moderate static power in order to maintain simple topology while offering robust power detection. The detector tracks the PVT behavior of level shifters and unlike traditional systems which offer robust performance by overdesigning the circuit for the worst corner performance. This is achieved by introducing slight asymmetries in the level shifter design via weak pull up paths and mismatched input transistors. The design is verified against PVT and also industry grade 5σ mismatch variation. Compared to traditional power detection circuits it's also smaller in size as it does not employ reference voltage generators or differential amplifiers.

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Հ.Հ. ՍԱՀԱԿՅԱՆ

ԼԱՐՄԱՆ ՄԱԿԱՐԴԱԿԻ ՓՈԽԱՐԿԻՉՆԵՐԻ ՀՈՒՍԱԼԻ ԱՇԽԱՏԱՆՔԸ ԲԱԶՄԱԼԱՐՈՒՄԱՅԻՆ ԻՆՏԵԳՐԱԼ ՍԽԵՄԱՆԵՐՈՒՄ ԱՊԱՀՈՎՈՂ, ԳԼՋ ՇԵՂՈՒՄՆԵՐԻՆ ՀԵՏԵՎՈՂ ՍՆՈՒՑՄԱՆ ԼԱՐՄԱՆ ՀԱՅՏՆԱԲԵՐՄԱՆ ՇՂԹԱ

Ժամանակակից ինտեգրալ սխեմաներում (ԻՍ), որոնք աշխատում են բազմաթիվ սնուցման լարումների միջոցով, հստակ սնուցման լարման հաջորդականությունը կարևոր է համակարգի հուսալի մեկնարկի, սնուցման և անցումային պայմանների դեպքում անորոշ վարքագծի կանխարգելման համար: Սովորաբար կիրառվում են սխեմաներ, որոնք վերահսկում են սնուցման լարումները և ազդանշան տալիս, երբ լարման մակարդակները կայուն են և գտնվում են գործառության սահմաններում: Այս ազդանշանները կառավարում են կարևոր գործառույթներ, ինչպիսիք են լարման մակարդակի փոխարկիչների ակտիվացումը և ներքին շղթաների միացումը: Սակայն այս գործառույթներն ապահովող ավանդական սխեմաների նախագծումը հաճախ պահանջում է նախագծման զգալի կրկնակներ՝ ապահովելու հուսալի աշխատանքը արտադրական գործընթացի, լարումային և ջերմաստիճանային (ԳԼՋ) փոփոխությունների լայն տիրույթում, որոնք առկա են առաջավոր կիսահաղորդչային արտադրական հանգույցներում: Առաջարկվում է նորարարական սնուցման լարման հայտնաբերման մեթոդ, որն ունի պարզեցված կառուցվածք և ԳԼՋ շեղումներին հետևող վարքագիծ, ապահովելով լարման մակարդակի փոխարկիչների հուսալի աշխատանքը: Առաջարկվող շղթան նախագծվել և մոդելավորվել է ՍԱՌԻԴ 14*nm* FinFET տեխնոլոգիայի կիրառմամբ:

Առանցքային բառեր. սնուցման լարման հայտնաբերում, հուսալիություն, լարման մակարդակի փոխարկիչ, բազմալարումային ԻՍ:

Г. Г. СААКЯН

ПНТ-ОТСЛЕЖИВАЮЩАЯ СХЕМА ДЕТЕКТИРОВАНИЯ НАПРЯЖЕНИЯ ПИТАНИЯ ДЛЯ НАДЕЖНОЙ РАБОТЫ ПРЕОБРАЗОВАТЕЛЕЙ УРОВНЯ НАПРЯЖЕНИЯ

В современных интегральных схемах (ИС), работающих в условиях нескольких доменов напряжения питания, точное управление последовательностью подачи питания имеет решающее значение для надежной инициализации системы и предотвращения неопределенного поведения во время включения и переходных процессов. Схемы Power-On Reset (POR) и Power-Good (PG) обычно используются для мониторинга напряжений питания и формирования сигнала, когда уровни напряжения стабильны и находятся в рабочих диапазонах. Эти сигналы управляют важными функциями, такими как включение уровневых преобразователей, инициализация конечных автоматов и активация последующих схем. Однако традиционное проектирование схем POR и PG часто требует значительного запаса по проектированию для обеспечения надежной работы в широком диапазоне изменений технологического процесса, напряжения и температуры (ПНТ), характерных для современных полупроводниковых производств. В данной работе предлагается новый подход к детектированию напряжения питания с упрощенной конструкцией и устойчивостью к ПНТ-изменениям, который обеспечивает надежную работу уровневых преобразователей с предсказуемым поведением в условиях отказа. Предложенная методология была реализована и проверена с использованием САУД 14*nm* FinFET технологии.

Ключевые слова: детектирование напряжения питания, надежность, преобразователь уровня напряжения, многовольтовая ИС.