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THE RELIABILITY IMPROVEMENT METHOD FOR THE BANDGAP REFERENCE WITH THIN OXIDE TRANSISTORS

Nowadays the sizes of CMOS (complementary metal-oxide-semiconductor) technology elements are shrinking to critical dimensions. As a result, previously negligible physical phenomena begin to manifest, whose effects are insignificant at higher technology levels. Supply voltage does not scale proportionally, and the gate dielectric thickness decreases, subjecting devices to stronger electric fields, thus causing stress on transistors and decreasing reliability.

A method is proposed for designing of bandgap reference with usage of only thin oxide devices, which are improved reliability of circuit and protected from stress conditions.

Keywords: CMOS, stress, reliability, aging, thin oxide device, bandgap reference.

Introduction. Continued scaling in modern submicron technologies makes ensuring the reliable and uninterrupted operation of integrated circuits (ICs) more challenging. The reliability of system operation is influenced by both internal and external factors. To anticipate such effects, it is necessary to model systems correctly during the design process [1].

One phenomenon that leads to a deterioration in the reliability of blocks is aging. Therefore, ignoring the impact of aging effects will lead to a decrease in the production of reliable ICs.

The deterioration of circuit characteristics over time is known as aging. This is primarily due to the degradation of the gate oxide layer and the interface between the gate dielectric and silicon over time [2]. The two main aging effects are Hot Carrier Injection (HCI) and Bias Temperature Instability (BTI). This work presents methods to reduce the circuit degradation and proposes alternatives to the existing solutions.

In technological processes below 5nm, semiconductor manufacturers face difficulties in fabricating transistors with thick gate oxide layers. This necessitates replacing all transistors with devices featuring thin gate oxide layers, complicating the IC design stages.

Analog components, which play a significant role in modern ICs, are responsible for receiving, processing, and transmitting signals (information) from one system to another. These are also the most sensitive parts of ICs. A significant portion of such systems consists of operational amplifiers that use high supply

voltages to ensure a high DC gain and a wide input signal frequency range. Analog circuits include voltage and current systems. In some analog circuits, such as voltage regulators, digital-to-analog and analog-to-digital converters, it is necessary to have bandgap reference with high precision. In other words, the accuracy of such circuits depends on the precision of the bandgap reference. Ideally, Bandgap reference should be independent of the technological process, supply voltage, and temperature changes. However, it is impossible to isolate the system from environmental influences. From this perspective, it is necessary to have temperature-independent bandgap reference.

The proposed solution and simulation results. The concept behind a traditional bandgap reference voltage source involves combining two voltages: one with a positive temperature coefficient (the voltage difference between the base and emitter of two bipolar transistors) and the other with a negative temperature coefficient (the base-emitter voltage, VBE). This combination produces a stable reference voltage. Its expression is:

$$V_{ref} = V_{BE} + \mathrm{K}V_T.$$

Among them, VBE represents the forward bias voltage from the base to the emitter of the bipolar transistor, K is a constant, and the V_T thermal voltage.

The traditional bandgap reference power supply structure is shown in Fig.1.

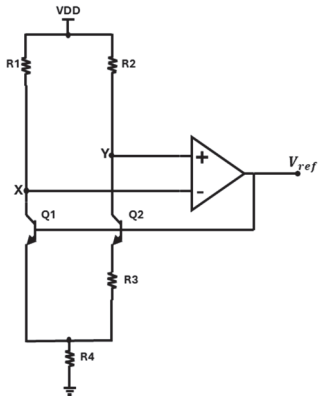

Fig. 1. A traditional bandgap reference voltage source

As shown in Fig. 1, this design employs an operational amplifier to equalize the voltages at points X and Y. The amplifier's output reference voltage is then fed back to the bases of transistors Q1 and Q2 [3].

For the development and analysis of the bandgap reference and to test the methods for reducing the effects of aging on transistor parameters, Synopsys' Galaxy Custom Designer [4] schematic editor is used.

Operational amplifier. In the first stage, an operational amplifier with an embedded cascode is designed. Folded-cascode operational amplifiers are widely used inside bandgap reference to provide high DC gain. In addition to the main constituent transistors, the circuit also includes transistors that enable power the operation down. These transistors are marked with dashed lines: M41, M42, M43, M44, and M54.

The schematic view (Fig. 2) and the HSPICE simulation results (Fig. 3) of the folded-cascode operational amplifier designed by SAED14nm FinFET technology are presented below [5-7].

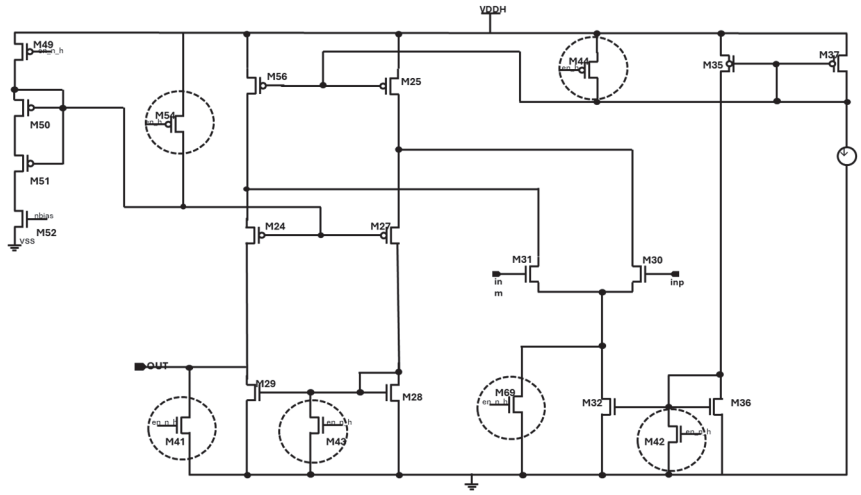

Fig. 2. Schematic view of the folded-cascode op-amp

Fig. 3. The AC characteristic of the designed folded-cascode op-amp

• Transistor M41 in power down mode sets the output of the operational amplifier to 0 (VSS) while also setting the same value on the drains of transistors M29 and M24.

• Transistor M43 sets a value of 0 on the gate of transistor M29, on the gate and drain of transistor M29, and on the drain of transistor M27.

• Transistor M42 sets a value of 0 on the gate of transistor M32, on the gate and drain of transistor M36, and on the drain of M35.

• Transistor M44 sets the VDD value on the gates of transistors M56, M25, and M35, as well as on the gate and drain of M37.

• Transistor M54 sets the VDD value on the gates of M24, M27, and M51, on the drain of transistor M49, and on the source and gate of transistor M50.

When the circuit is switched to the power down mode, overvoltages occur on the following transistors: M41, M42, M43, M44, M54.

To prevent overvoltages in the circuit, an operational amplifier circuit is developed with added transmission gates and transistors (Fig. 4), setting 0 and VDD values on all terminals of the n-channel and p-channel transistors, respectively.

The effect of the added transistors preventing overvoltages is implemented as follows:

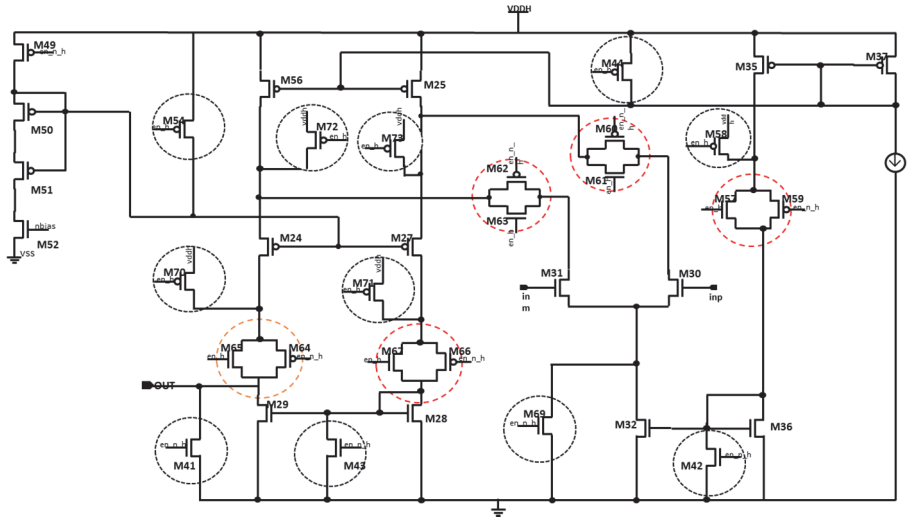

Fig. 4. The schematic view of the folded-cascode op-amp after modifications

• Transistor M35 before the modifications, in the power down mode, the drain value of transistor M35 was 0. Now, transistor M58 sets the drain value to VDD. A transmission gate, consisting of transistors M57 and M59, acts as a switch

that disconnects the connection between the drains of M35 and M36 during power down mode. Without the transmission gate, this connection would cause a short between VDD and VSS.

- Transistors M71 and M73 set the drain and source values of transistor M27 to VDD in the power down mode. Consequently, the voltage between the terminals of M27 equals zero, as transistor M54 sets the gate value to VDD. To avoid a short, a transmission gate consisting of transistors M66 and M67 disconnects the connection between the drains of M27 and M28 during the power down mode.
- Transistors M70 and M72 set the drain and source values of transistor M24 to VDD in power down mode, preventing overvoltages between the transistor's terminals. Transistors M64 and M65 serve as transmission gates to disconnect the connection between the drains of M24 and M29, avoiding a short between VDD and VSS.
- Transistors M72 and M73 set the drain values of M56 and M25 transistors to VDD, while transmission gates, consisting of transistor pairs M62-M63 and M60-M61, disconnect the drains from transistors M31 and M30, respectively.
- Modifications to the M30 and M31 input differential pair transistors are made at a higher level.
- Transistor M69 sets the drain value of M32 to VSS in the power down mode.
- In this way we also protect transistors M27 M24, M56, M25, M32, M30 and M31.
- After those changes, aging simulations are performed, and it is found that problems are solved and there is no significant degradation in the power down mode (Table 1).

Table 1

V_{th} and I_c values of devices for folded-cascode operational amplifier before and after modifications

Transistors Name	Power down mode before modifications		Power down mode after modification	
	ΔV_{th} (mV)	ΔI_c (%)	ΔV_{th} (mV)	ΔI_c (%)
M35	197	19,9	0,9	1,4
M31, M30	200	20,7	1,1	1,9
M25, M56	243	23,7	25	3,5
M27, M24	245	23,9	27	3,9

Bandgap reference. Some of the critical components of the bandgap reference (Fig. 5) are the transistors serving as current sources. It is essential to reduce the aging effects on transistors M6, M7, and M8. The pair of transistors M6 and M7 equalizes the input voltages of the operational amplifier, thereby creating a voltage independent of absolute temperature. Transistor M8 copies the current flowing through M6 and M7 and, using a voltage divider, provides different reference voltage values. Aging in bipolar transistors often occurs due to bias temperature instability. However, in this case, the base of the bipolar transistors is connected to the collector, preventing reverse bias. Even so, possible degradation should not be ruled out. If resistors degrade, the parameter shifts will be identical, so resistor degradation will not affect the reference voltage value. Nevertheless, to fully protect against aging phenomena, the likelihood of resistor degradation must also be reduced.

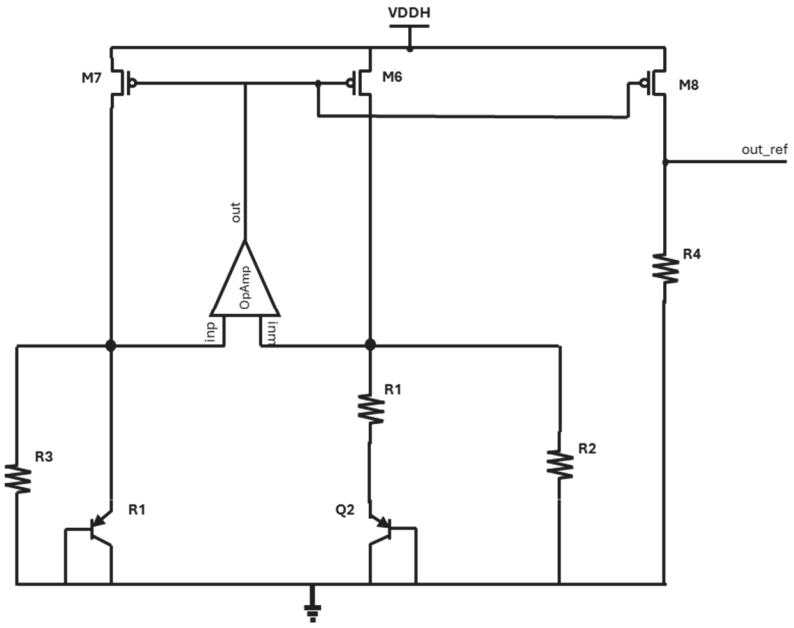

Fig. 5. The scheme of the bandgap reference

• The sources of M6, M7 and M8 transistors are connected to the high-voltage source VDD. The drain voltage varies during operation, but in the power down mode, the drains are set to 0. The output of the operational amplifier, which is set to 0 in the power down mode, is connected to the gates of the transistors. In the power down mode, this causes an overvoltage between the source and the gate. Additionally, the voltage difference between the source and the gate is sufficient to keep the transistors in the ON state.

• The bases and collectors of Q1 and Q2 bipolar transistors are connected to the low-voltage source VDD, whose value is 0. The emitter of Q1 is connected to the operational amplifier input, while the emitter of Q2 is connected to a resistor whose other terminal is connected to the other operational amplifier input. The floating value at the inputs of the operational amplifier in the power the down mode occurs due to the bipolar transistors.

• One terminal of the R4 resistor (or the terminal of the last resistor in a parallel connection) is connected to VSS, which is 0, while the other terminal is connected to the drain of transistor M8, which, in the power down mode, has a floating value. This can result in leakage current, albeit small. However, for designing circuits that minimize the aging-induced degradation, it is necessary to eliminate the potential floating values on conductors.

To prevent overvoltages in the proposed bandgap reference (Fig. 6), transmission gates and transistors which are added set VDD values on all terminals of p-channel transistors and set 0 values on the operational amplifier inputs and circuit output in the power down mode.

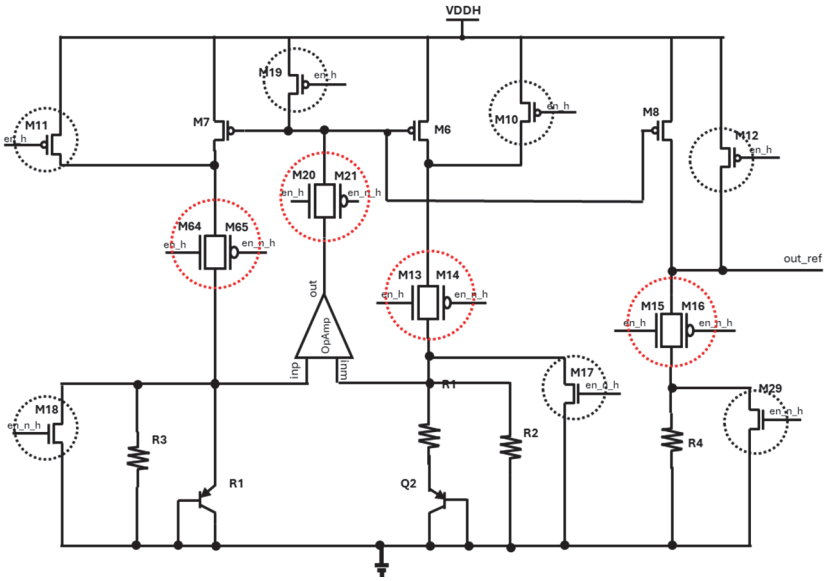

Fig. 6. The scheme of the bandgap reference after modification

The effect of the added transistors preventing overvoltages is implemented as follows:

• Transistor M19 sets the gates of M6, M7, and M8 transistors to VDD in the power down mode, disabling them. Transistors M10, M11, and M12 set the drains of M6, M7, and M8 to VDD, respectively.

• Transistor M18 sets the emitter of the Q1 bipolar transistor to 0 in the power down mode. Additionally, the transistor pair M64-M65, serving as a transmission gate, disconnects the connection between the drain of M7 and the emitter of Q1 and resistor R3, preventing a short between VDD and VSS.

• Transistor M17 sets the second terminal of resistor R1 to 0 in the power down mode, while the transmission gate, consisting of transistors M13-M14, disconnects the drain of M6 from resistors R1 and R2, preventing a short between VDD and VSS.

• With transistor M29, the voltage drops across resistor R4 in the power down mode equalling to zero. The transistor pair M15-M16 disconnects the resistor from transistor M8, preventing a short.

At the output of the operational amplifier, a value of 0 is set in the power down mode using transistor M41 (Fig. 4). Additionally, the output of the operational amplifier is connected to the gates of transistors M6, M7, and M8 which in the power down mode are set to VDD by transistor M19 (Fig. 4), leading to a short between VDD and VSS. To address this, a transistor pair M20-M21 (transmission gate) is added to disconnect the connection between the operational amplifier output and the gates of transistors M6, M7, and M8.

The gates of the input differential pair transistors M30 and M31 are set to 0 in the power down mode using transistors M17 and M18. Transmission gates, consisting of transistor pairs M13-M14 and M64-M65, disconnect the inputs of the operational amplifier from transistors M6 and M7, respectively.

Conclusion. Circuits have been developed only using thin oxide devices. The aging effects are studied on a bandgap reference, operating in the power-down mode. It is observed that, with the standard architecture, aging serious impacted the primary parameters of the amplifier, particularly in the power-down mode, due to the stress conditions affecting the thin oxide devices. New schematic solutions have been implemented to prevent the stress conditions on the devices due to aging degradation in a 10-year lifetime.

The summary table of the designed bandgap reference before and after the proposed design updates, with a 10-year aging is summarized in Table 2.

Table 2

Results of bandgap reference before and after the proposed design updates

Parametrs	Initial	Before modification	After modification
Gain (*dB*)	60.5	42.3	56.1
V_{ref} (*mV*)	800 ± 8	600 ± 40	750 ± 12
I_{ref} (*mA*)	0,25	0,19	0,24

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Yerevan state university. “Synopsys Armenia” CJSC. The material is received on 29.01.2025.

Գ.Ա. ՈՍԿԱՆՅԱՆ

ԲԱՐԱԿ ՕՔՍԻԴԻ ՇԵՐՏՈՎ ՏՐԱՆԶԻՍՏՈՐՆԵՐՈՎ ՀԵՆԱԿԱՅԻՆ ԼԱՐՄԱՆ ԱՂԲՅՈՒՐԻ ՀՈՒՍԱԼԻՈՒԹՅԱՆ ԲԱՐՁՐԱՑՄԱՆ ՄԵԹՈԴ

Ներկայումս ԿՄՕԿ (կոմպլեմենտար մետաղ-օքսիդ կիսահաղորդիչ) տեխնոլոգիայի տարրերի չափերը հասել են կրիտիկականի։ Արդյունքում սկսում են ի հայտ գալ նախկինում աննշան ֆիզիկական երևույթներ, որոնց ազդեցությունը ավելի բարձր տեխնոլոգիական մակարդակներում աննկատ էր։ Սնման լարումները համապատասխան կերպով չեն մասշտաբավորվում, փականի դիէլեկտրիկի հաստությունը փոքրանում է, ինչի արդյունքում սարքերը ենթարկվում են ուժեղ էլեկտրական դաշտի ազդեցության՝ առաջացնելով սթրես տրանզիստորներում և հուսալիության նվազում։

Առաջարկվում է նախագծման մեթոդ, որը թույլ է տալիս ստեղծել հենակային լարման աղբյուր՝ օգտագործելով միայն բարակ օքսիդի շերտով տրանզիստորներ, որոնք պաշտպանված են սթրեսային պայմաններից և ապահովում են սխեմայի բարձր հուսալիություն։

Առանցքային բառեր. ԿՄՕԿ, սթրես, հուսալիություն, ծերացում, բարակ օքսիդի շերտով տրանզիստոր, հենակային լարման աղբյուր։

Г.А. ВОСКАНЯН

МЕТОД ПОВЫШЕНИЯ НАДЕЖНОСТИ ИСТОЧНИКА ОПОРНОГО НАПРЯЖЕНИЯ С ТОНКИМИ ОКСИДНЫМИ СЛОЯМИ ТРАНЗИСТОРОВ

В настоящее время размеры элементов технологии КМОП (комплементарный металл-оксид-полупроводник) уменьшаются до критических размеров. В результате начинают проявляться ранее незначительные физические явления, влияние которых было несущественным на более высоких размерах технологий. Питающее напряжение не уменьшается пропорционально, а толщина диэлектрика затвора уменьшается, подвергая устройства более сильным электрическим полям, что вызывает напряжение на транзисторах и снижает их надежность.

Предлагается метод проектирования опорного источника напряжения с использованием только тонких оксидных приборов, которые обладают улучшенной надежностью схемы и защищены от условий напряжения.

***Ключевые слова*:** КМОП, стресс, надежность, старение, транзистор с тонким оксидом, опорный источник напряжения.