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A MINIMIZATION METHOD FOR TRANSISTOR AGING INFLUENCE IN HIGH-TO-LOW VOLTAGE LEVEL CONVERTER DESIGN

Most activities would be impossible to imagine without the integrated circuits that are produced today. Modern integrated circuits have attained extremely high levels of integration by adhering to Moore's law. The density of element placement on the wafer can be significantly increased thanks to the advancements in nanoelectronics. The decrease in operating voltages required for transistors that does not keep up with transistor scaling leads to the emergence of unwanted voltage values between the transistor's terminals. The inability of factories to manufacture transistors with a thick dielectric layer results in overvoltage issues, which accelerate the aging and compromise system functionality in the coming years. It is suggested that a level converter be designed using the proposed method in order to address the communication issue with the aging effect.

Keywords: voltage level converter, multivoltage supply, aging effect, power consumption, overvoltage.

Introduction. Numerous industries, including autonomous vehicles, medical gadgets, portable electronics, and military gear, heavily rely on integrated circuits. Computers, smartphones, and TV sets are just a few of the many electronic gadgets that use integrated circuits to process and store data, among other tasks. They aid in facilitating communication across a range of media, such as fiber optic networks, satellite linkages, and wired and wireless connections. Therefore, miniaturization, performance, cost reduction, and high productivity are the primary factors that make ICs so crucial.

The integration level of 100 billion transistors per chip has already been attained by foundries, who are making separate preparations to fit an increasing number of transistors into each square millimeter of silicon [1].

Significantly increasing the density of element placement on the wafer is made possible by the revolution in nanoelectronics. However, the decrease in operating voltages required for transistors does not match transistor scaling, resulting in the occurrence of unwanted voltage values between the transistor's terminals. As a result, engineering problems pertaining to the fabrication of microelectronic integrated circuits are challenging to be solved. Due to these

production issues, as the degree of integration has increased, semiconductor microcircuit factories are now unable to supply integrated circuit designers with transistors with a thick dielectric layer, which enables operation at relatively higher voltages without appreciably affecting the effects of aging.

The aging effect is one of the most significant variables influencing the reliability of integrated circuits (ICs) [2]. As a result, the circuit's characteristics decrease with time and may eventually cause the circuit to fail [3]. For instance, threshold voltage degradation is brought on by the NBTI effect. The transistor's operational point changes when the threshold voltage rises. When the circuit is operating at greater supply voltages or high temperatures, threshold changes fall even faster. In contemporary systems, variations in transistor properties like threshold and current become more apparent when gate length and operating voltages are scaled. Transistor performance is also reduced by the HCI effect. It harms the NMOS and PMOS gate oxides. Because of the high temperature and voltage at which the transistor functions, the carriers get enough kinetic energy from the field to get beyond the gate oxide's (SiO2) potential barrier. Since transistor sizes are scaled more aggressively than supply voltages, as previously indicated, the electric field will likewise increase in value as technologies get smaller (1)[4]:

$$Evertical = \frac{Vnom}{Tox}. \quad (1)$$

The velocity of hot carriers in some cases where the electrical field is high enough could be higher than the saturation velocity [5]:

$$\Delta V_{TH} \sim \frac{1}{\sqrt{L}} \exp(\propto_1 E_{OX}) \exp(\propto_2 V_{DS})\, t^{n_{HC}}. \quad (2)$$

The dependency of threshold voltage change on account of hot carrier effect is explained above (2)[6], where $\propto_1$ and $\propto_2$ are the voltage scaling factors, V_{DS} – the drain source voltage difference, E_{ox} – the oxide electrical field, n_{HC} – the time exponent.

Once carriers have accumulated sufficient energy, they can collide with Si atoms and remove electron-hole pairs, resulting in ionization. Consequently, the field-accelerated produced carriers may re-initiate ionization. The produced carriers have the potential to harm the interface or be injected into the oxide. At significantly higher drain-source voltages than gate-source voltages, this impact is most pronounced (Fig. 1).

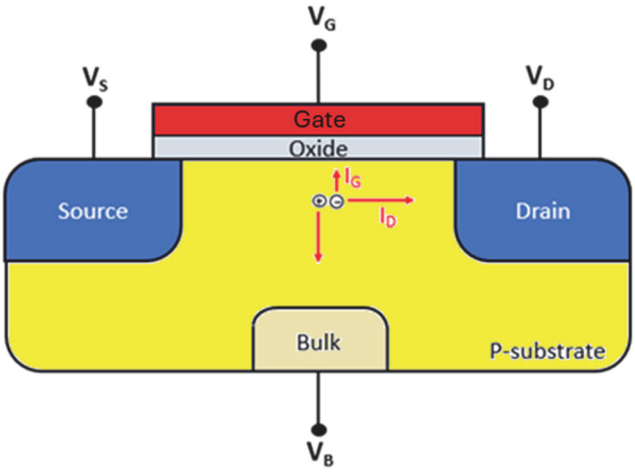

Fig. 1. Accelerated hot carriers

Injecting hot carriers into the oxide may have a second effect, since the high gate voltage may push them in the direction of the gate. Electrons can pass over the potential barrier and enter the oxide if the gate voltage is high enough (Fig. 2).

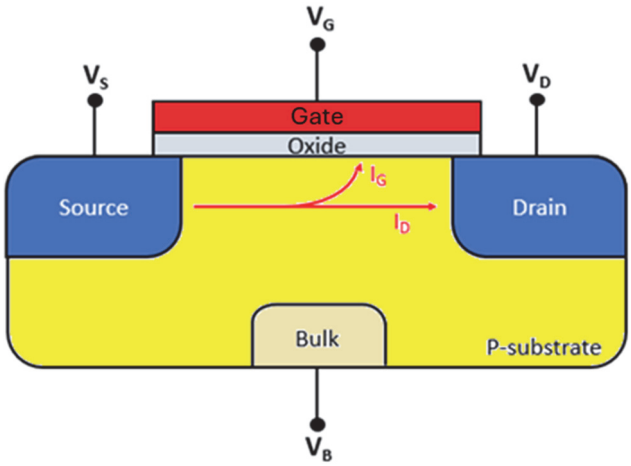

Fig. 2. A channel hot carrier

Tests are conducted on specific models provided by semiconductor factories and under well-defined working settings to account for the aging phenomena of the IC. These conditions represent a variation of +10% from the nominal value of the supply voltage and an operating temperature of +125°C [7].

Designers research and apply a variety of techniques to address the issues that have been found. The impacts of aging phenomena can be avoided in a variety of ways. By using technical and circuit solutions, the impact can be lessened or

eliminated [8]. Using regulatory protrusions found in certain contemporary IS, it is possible to document the aging phenomenon's presence and offset the detrimental effects of technological deviations [9]. However, the cost of adding each protrusion is significant. As a result, control, accounting, and compensation methods that are part of the IS must be developed [10].

Nowadays, low power systems and digital circuits are a big problem in circuit design. Short-circuit power, dynamic power, and static power are all greatly decreased by lowering the supply voltage. Low supply voltages, however, restrict the circuit's speed and have an impact on the sub-block's linearity and internal gain [11]. Utilizing the multi-voltage supply system, where each segment has its own local voltage source, is the main focus of recent and developing applications [12].

To create an interface between sub-blocks, the voltage level converter uses a variety of supply voltage approaches. Low-level voltages can be changed into higher-level voltages suitable for later stages by using voltage level converters. Voltage level converters are therefore employed as an intermediate and auxiliary block. These voltage level converters must be high-speed, low-power, and have a smaller silicon area to minimize their total performance impact. However, current architectures make it impossible to construct voltage level converters without using transistors with a high dielectric layer because stress voltage causes aging effects that reach detectable levels.

The problem description. The issues mentioned are typical for a level shifter since the high (VDDH) and low (VDD) supply levels can be somewhat distant from one another (Fig. 3). Not all technologies have thick oxide devices or are designed to withstand the high voltage differentials between transistor terminals that generate stress.

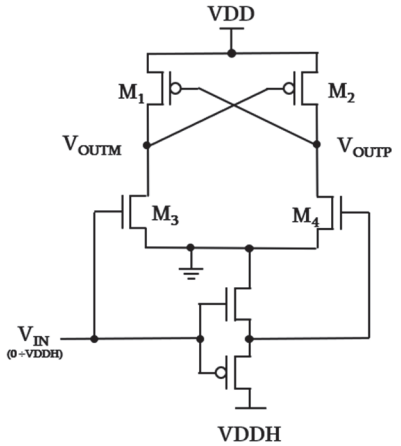

Fig. 3. Level converter modern architecture

Understanding the circuit's weak points is crucial when examining the level shifter's overall architecture. The input signal is controlled by the M3 and M4 control transistors. The VDDH level, the design's high supply level, creates the input signal, and the VDD level creates the output signal. Transistor M3 is opened by the logic 1 level at the input (VDDH), whereas transistor M4 is in the off mode. The gate of M2 opens as a result of M3 being open, bringing it to the zero level. The output (OUTP) in this instance is brought to the logic 1 level by M2, but its level is VDD. On the flip side, outm approaches level 0 and outp shuts off transistor M1[13].

Since the maximum voltage difference between the terminals of all transistors is VDD, it should be noted that when the VDDH signal reaches the circuit's input and transistor M3's source is grounded, the potential difference between the gate and source of M3 is VDDH, which is unacceptable.

The proposed solution. A circuit that converts VDDH to Vnbias without stress voltage for the transistor can be used to address the issue of transistor overvoltage and to provide suitable operating conditions for the transistor (Fig. 4). This approach ensures that the transistors will have a significantly longer service life and work under the manufacturer-specified settings (without overvoltage).

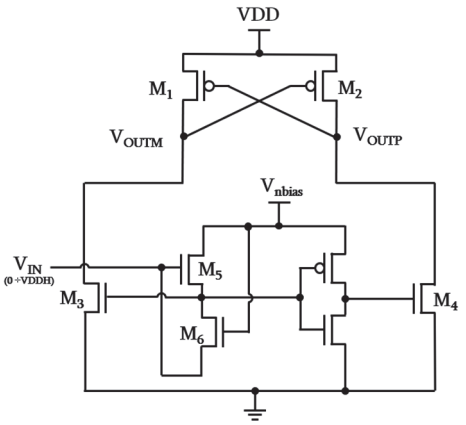

Fig. 4. Level converter proposed architecture

The principle of operation of the first stage is the same as the inverter. Since the M6 transistor's source is also linked to Vin and the gate to Vnbias, the conditions for opening the M6 transistor are satisfied. When Vin is connected to the gate of the M5 transistor, it has a low level, and the M5 transistor is closed. As a result, M4's gate is high and M3's gate is low. The output is a logical zero. When Vin is high, the transistor M6's terminal that is connected to Vin turns into a drain, and the transistor M6's terminal that is connected to the gate of M3 turns into a source. The gate of VDDH and the source of transistor M5 are both subjected to potential Vnbias at the same time. When Vgs exceeds Vth and transistor M5 opens,

M6 is consistently closed because there is no potential difference between the source and the gate, both of which have potential Vnbias. Transistor M3's gate is thus brought up to the potential Vnbias, whereas transistor M4's gate is pulled to zero by the inverter output.

Depending on the input level, the OUTN and OUTP outputs give a steady voltage. The logic 1 level for this output is VDD, or 0.8 *V*, and it is 1.2 *V* for a high input voltage level. Bandgap circuits or voltage dividers can be used to determine the Vnbias value; given the right matching techniques in the designs, the voltage shouldn't fluctuate by more than 5*%*.

Simulation results. Aging simulation is done for the VDDH level 1.2 *V* and 125 °C temperature. This is stress conditions that are applied for 10 years aging.

With the proposed approach, the maximum current degradation is less than 10% as opposed to 52% in modern architecture, and the maximum threshold voltage degradation is less than 50 *mV* as opposed to 250 *mV* in modern architecture (Fig. 5).

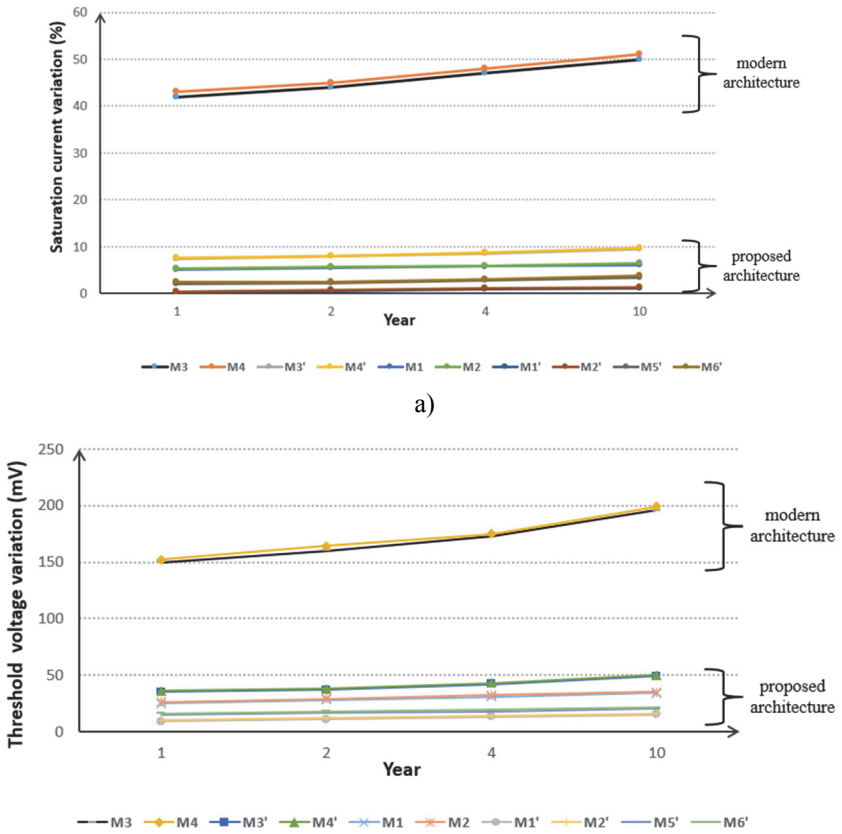

Fig. 5. The transistor saturation current (a) and the threshold voltage (b) variation in 10 years for modern and proposed architectures of a level converter

The plot for the proposed method (Fig.6) show that the voltage level is settling at VDD level for the OUTP. The rising time remains relatively constant, but the degradation of transistors M3 and M4's characteristics results in a significant increase in the switching time from high to the low logic level.

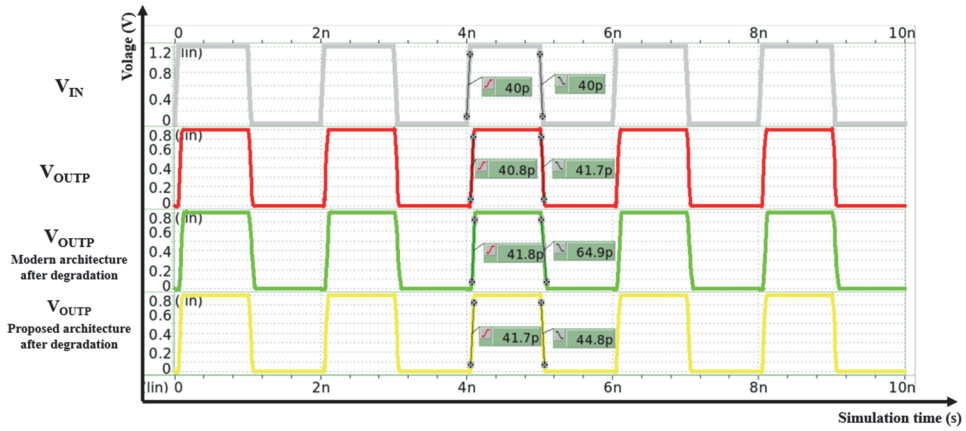

Fig. 6. Transient analysis of level converters

Conclusion. A level converter with a modern architecture has been designed with the SAED 14 *nm* FinFet technology [14]. Overvoltage is observed on transistors, resulting in excessively fast aging. To lessen the aging effect, an architecture upgrade has been proposed. The findings show that the saturation current and threshold voltage degradation are lessened, not exceeding 10 percent and 50 *mV*, respectively. This has an effect on the level converter's primary parameters, particularly rise and fall times. However, the circuit area and the number of transistors employed rose somewhat, but this increase is acceptable for the intended outcomes. The SAED 14 *nm* FinFet technology libraries have been used during the HSPICE simulations, and outputs have been exported by Galaxy Custom Designer tool [15].□

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ԲԱՐՁՐԻՑ ՑԱԾՐ ԼԱՐՄԱՆ ՄԱԿԱՐԴԱԿԻ ՓՈԽԱԿԵՐՊՉՈՒՄ ՏՐԱՆԶԻՍՏՈՐՆԵՐԻ ԾԵՐԱՑՄԱՆ ԵՐԵՎՈՒՅԹՆԵՐԻ ՆՎԱԶԵՑՄԱՆ ՄԵԹՈԴ

Տարբեր բնագավառների գործունեության մեծ մասն անհնարին կլիներ պատկերացնել՝ առանց ներկայումս արտադրվող ինտեգրալ սխեմաների: Ժամանակակից ինտեգրալ սխեմաները հասել են ինտեգրման շատ բարձր մակարդակի՝ ըստ Մուրի օրենքի: Նանոէլեկտրոնիկայի ոլորտում նվաճումների շնորհիվ՝ տարրերի տեղաբաշխման խտությունը շարունակում է աճել: Տրանզիստորների համար անհրաժեշտ աշխատանքային լարումների նվազեցումը, որն ավելի արագ է կատարվում, քան տրանզիստորների մասշտաբավորումը, հանգեցնում է դրանց ելուստների միջև կիրառվող ոչ ցանկալի լարման արժեքների: Հաստ դիէլեկտրական շերտերով տրանզիստորներ արտադրելու գործարանների անկարողությունը հանգեցնում է գերլարման խնդիրների, որոնք արագացնում են ծերացումը և վտանգում համակարգի ֆունկցիոնալությունը հետագա տարիներին: Առաջարկվում է մշակել լարման մակարդակի փոխարկիչ՝ օգտագործելով առաջարկվող մեթոդը՝ ծերացման երևույթի խնդիրը լուծելու համար:

Առանցքային բառեր. լարման մակարդակի փոխարկիչ, բազմավոլտ սնուցում, ծերացման երևույթ, էներգասպառում, գերլարում:

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МЕТОД МИНИМИЗАЦИИ ЯВЛЕНИЯ СТАРЕНИЯ ТРАНЗИСТОРОВ В КОНСТРУКЦИИ ПРЕОБРАЗОВАТЕЛЯ НАПРЯЖЕНИЯ С ВЫСОКОГО УРОВНЯ НА НИЗКИЙ

Большинство видов деятельности было бы невозможно представить без интегральных схем, которые производятся сегодня. Современные интегральные схемы достигли чрезвычайно высокого уровня интеграции, следуя закону Мура. Плотность размещения элементов на пластине может быть значительно увеличена благодаря достижениям в области наноэлектроники. Снижение рабочих напряжений, необходимых для транзисторов, не поспевает за масштабированием транзисторов, что приводит к появлению нежелательных значений напряжения между выводами транзистора. Неспособность заводов производить транзисторы с толстым диэлектрическим слоем приводит к проблемам с перенапряжением, которые ускоряют старение и ставят под угрозу функциональность системы в последующие годы. Предлагается разработать преобразователь уровней с использованием предлагаемого метода для решения проблемы связи с эффектом старения.

Ключевые слова: преобразователь уровня напряжения, мультинапряжение, эффект старения, энергопотребление, перенапряжение.