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S.A. KHACHATRYAN, A.S. GABOYAN

THE UNDERSHOOT AND OVERSHOOT MINIMIZATION METHOD IN VOLTAGE REGULATORS

As in modern data transfer circuits data rate and clock frequency continu to increase, the contribution of jitter to the overall timing error becomes increasingly significant in high-speed interfaces.

The main techniques of jitter minimization are usage of decaps and supply voltage regulation. There are two main groups of voltage regulators: linear and switching. In high-speed transceivers linear voltage regulators are often used, especially low-dropout regulators (LDOs). The main advantages of linear voltage regulators are small area and power consumption compared to switching regulators. LDO provides regulated output voltage to sensitive analog circuits for different load currents with the help of negative feedback. Another advantage of LDO is big power supply rejection compared with other regulators.

In this paper, a method of overshoot voltage reduction in LDOs during load switching is proposed.

Keywords: voltage regulator, low-dropout regulator, LDO, overshoot, negative feedback, ripple, fast loop.

Introduction. The architecture of a typical electronic microsystem consists of several on-chip voltage sources for regulation [1]. In modern circuits LDOs are used to supply noise-sensitive loads, such as voltage or current mode drivers, analog equalizers, delay-locked loops, etc. These voltage regulators should be independent of the load current and process variation. The basic architecture of a voltage regulator is shown in Fig.1.

It consists of an error amplifier (EA) which is used for controlling the pass transistor gate to provide a regulated output voltage. Error amplifiers are often based on folded cascode and active load operational amplifiers (opamp). The folded cascode structure can achieve a high open loop gain with one stage. This topology uses a differential pair at the input for rejection of common mode and power supply noise. Therefore, the folded cascode offers an auto-compensation of phase margin, great common mode range on the input and a two-stage amplifier gain. Moreover, this topology has a better Power Supply Rejection Ratio (PSRR) is compared to the two-stage amplifier and a telescopic amplifier, since there is no pole splitting [2]. Op Amp based on an active load amplifier has a simple architecture with high gain and good stability parameters.

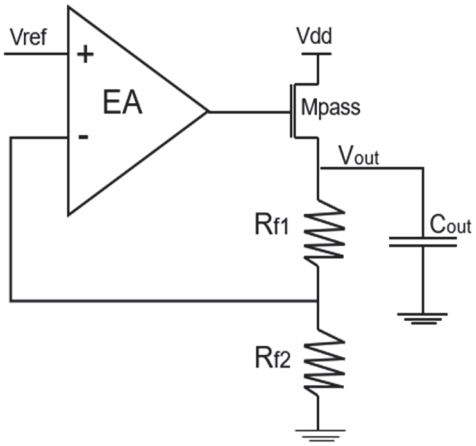

Fig.1. Voltage regulator architecture

The amplification factor for voltage regulator is defined by following equation:

$$\text{Av}=Vref\left(\frac{Rf1}{Rf2}+1\right) \text{ [3].} \quad (1)$$

As shown in the above equation the voltage regulator amplification can be controlled by changing Rf1 and Rf2 resistor values.

For improving the voltage regulator's PSRR, a technique with adding a capacitor between regulator output and AC ground is commonly used, which changes the dominant pole [3]. The output capacitor is being charged during a period when more current flows through the pass gate than required for load driving. When the pass gate cannot provide the necessary current for load driving, the capacitor starts to discharge, which minimizes the undershoot. By increasing the output capacitor value, the output ripple of the voltage regulator will decrease, but it will have an impact on response time. In addition, there is also a limiting factor for increasing the capacitor such as area.

Problem description. A voltage regulator circuit using folded cascode architecture Fig.2 [4] has been designed by SAED14 nm FinFet technology [5], and HSPICE simulations have been performed.

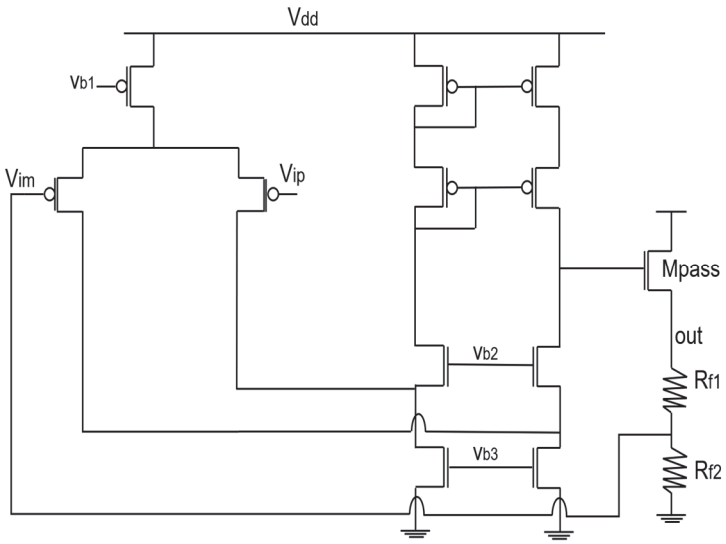

Fig.2. A voltage regulator based on folded cascode opamp

An output Mpass transistor is designed for driving up to 1 *mA* current and middle point of feedback resistors called Vfb.

In the first step of circuit verification, HSPICE simulation is performed for TT (Vdd=0.9*V*, T =25°C), FF (Vdd=0.945*V*, T=-40°C), SS (Vdd=0.838*V*, T=125°C) cases and voltage regulator stability parameters are checked. Results are shown in Fig. 3 and in Table 1.

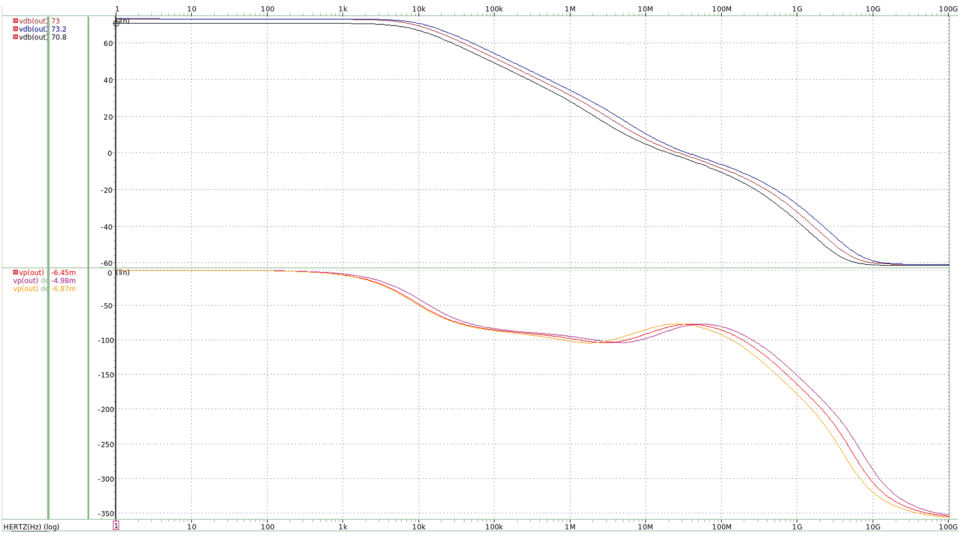

Fig.3. AC characteristics of nmos fast loop voltage regulator stability results.

Table 1.

The main voltage regulator stability parameters

Measurement	SS	TT	FF
PM *(deg)*	74	76	78
GM *(dB)*	36,2	37,1	37,7
UGB *(MHz)*	19,6	26,9	35
Gain at low frequency *(dB)*	70,8	73	73,2

During the simulations, the 3 *pF* output capacitor was used, and the output load has changed so that the output current value increased from 0 to 1 *mA* during 20 *pS* which caused a huge undershoot and 18 *nS* settling time for TT case. The output current value was decreased from 1 *mA* to 0 *mA* which caused a huge overshoot as shown in Fig. 4, Fig. 5 and on Table 2 for TT, FF, SS corners.

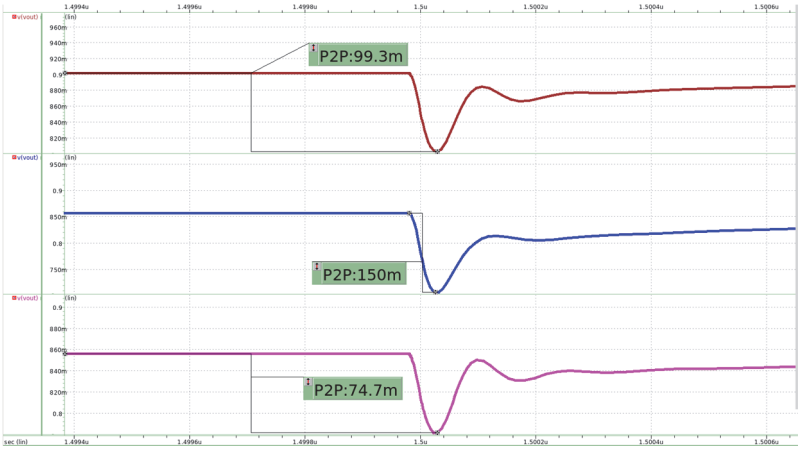

Fig.4. A voltage regulator output undershoot

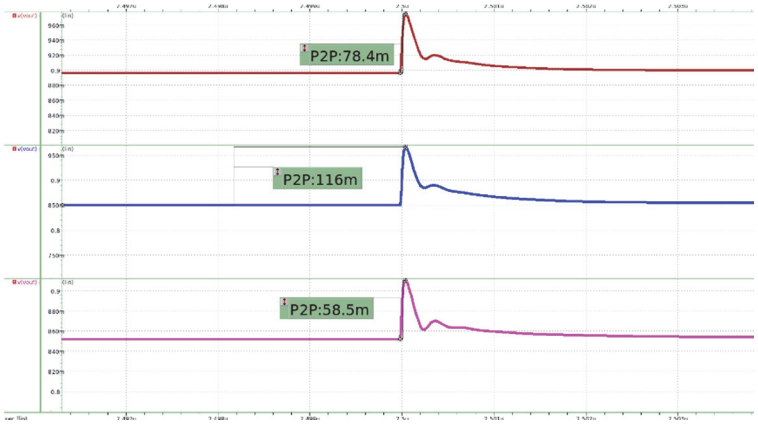

Fig.5. A voltage regulator output overshoot

Table 2

The voltage regulator output measurement results

Measurement	SS	TT	FF
P2P undershoot *(mV)*	150	99.3	74,7
Settling time undershoot *(nS)*	24	18	17
P2P overshoot *(mV)*	116	78,4	58,5
Settling time overshoot *(nS)*	19	17	14,7

As shown in Fig.4, the output voltage of the voltage regulator drops from 900 *mV* to 838 *mV* due to load changing, which is unacceptable, because it can lead to high jitter in clock path circuits or data errors in transceivers, because modern high-speed critical circuits are designed to work with +-5% range of voltage supply. In modern designs, power supply Induced Jitter (PSIJ) is one of the major contributors which limits the timing budget of high-speed systems [6].

The proposed solution. Two voltage regulators are added (Fig.6) in parallel to the main voltage regulator to provide higher bandwidth and shorter response time.

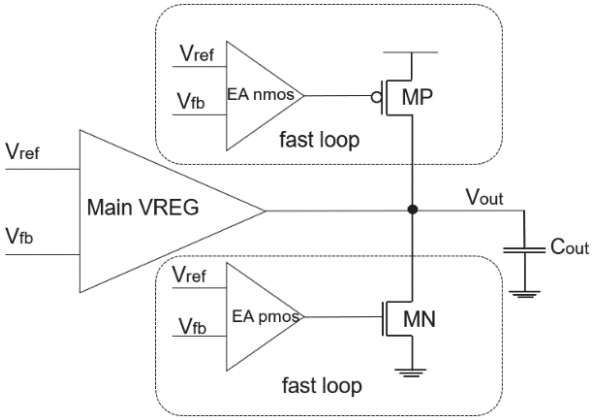

Fig.6. Main and fast loop voltage regulators

Added voltage regulators are called ‘fast loop’. Because the fast loop and main voltage regulator are connected to each other parallelly as shown in Fig. 6, PSRR requirements for the main voltage regulator are stricter, but it’s necessary to design fast loop regulators to have less than 0 *dB* PSRR.

The operating principle of the fast loop voltage regulators is as follows: when the main voltage regulator is not able to provide a necessary current for driving the load, MP transistor provides the missing part of the needed current and if the main voltage regulator gives more current than necessary for load driving, the excess current discharges through the MN transistor. Besides using fast loop

regulators as a charge and discharge paths, they also give an opportunity to reduce the settling time due to a higher bandwidth (800 *MHz*) compared to the main regulator (100 *MHz*).

Error amplifier (nmos and pmos) is opamp which can be a folded cascode as used in the main voltage regulator or another type of operational amplifier. In the proposed architecture, an opamp is used based on active load configuration (Fig.7). This circuit has good features in terms of self-bias capability, common-mode rejection, voltage gain, and the gain-bandwidth product [7].

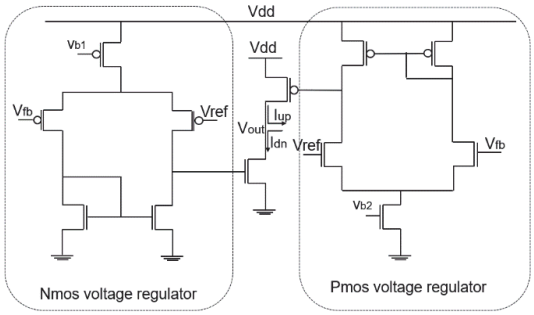

Fig.7. Fast loop voltage regulator architecture based on active load OTA

Error amplifiers used in fast loop have poor phase margin and are able to use the proposed architectures of LDOs without any kind of external compensation. It is necessary to implement an internal compensation that ensures stability under all load conditions. This may be accomplished by using pole split techniques based on the Miller effect, where the compensation network consists of a current buffer as a differentiator that sets the dominant pole at an internal node. Other Miller compensation techniques for multistage amplifiers can also be used, as proposed in Fig. 8 [8]□

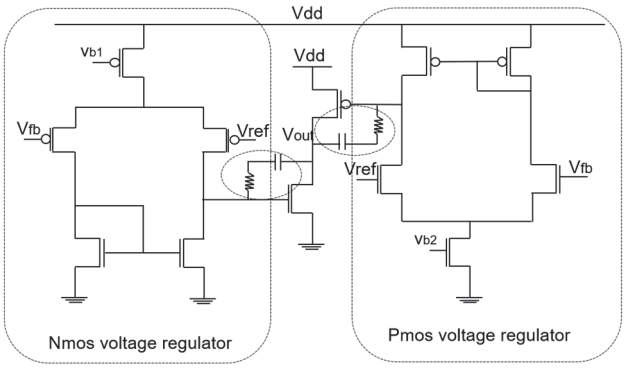

Fig.8. Fast loop voltage regulator architecture based on active load OTA with Miller compensation circuit

Internal compensation causes a higher output voltage ripple, it can be reduced by charging/discharging the current available to charge and discharge the gate capacitance of the pass transistor, thus improving the settling time of the regulator. This sets a trade-off between transient response and power consumption because, according to the results, a reduction in power consumption penalizes the capacity to handle the gate capacitance of the power transistor.

Results. In the first step of the method verification, HSPICE simulation carried out and the fast loop voltage regulator's stability parameters were checked. The results are shown in Fig. 9 and Fig. 10 and in Table 3 for TT,SS and FF corners.

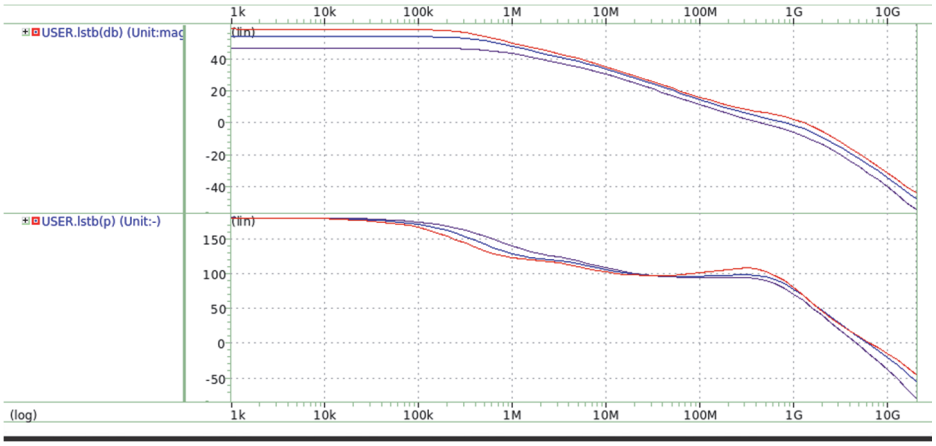

Fig.9. AC characteristics of pmos fast loop voltage regulator

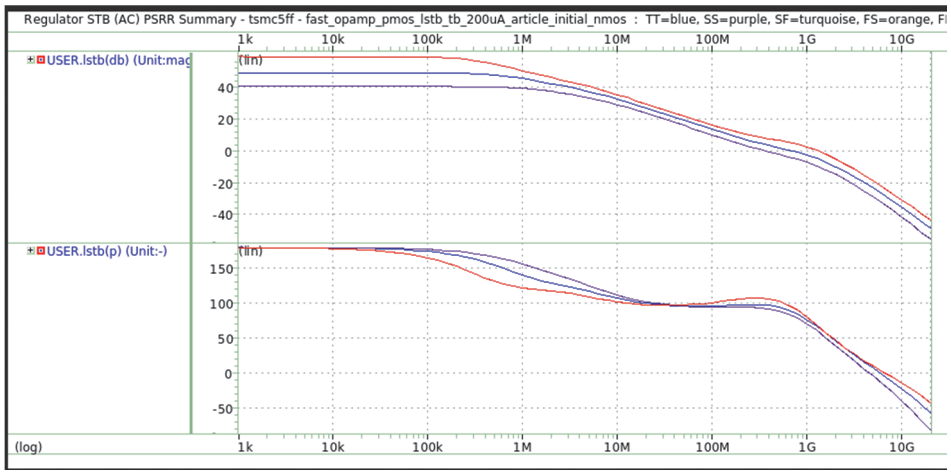

Fig.10. AC characteristics of nmos fast loop voltage regulator stability results

Table 3

The voltage regulators stability parameters

Type	Corner	PM *(deg)*	GM *(dB)*	UGB *(MHz)*	Gain at low frequency *(dB)*
PMOS voltage regulator	SS	92,4	26,06	374,6	46,8
	TT	88,9	25,3	683,8	53,9
	FF	73,8	23,4	1141,1	58,6
NMOS voltage regulator	SS	93,4	26,6	322,2	40,6
	TT	91,4	25,7	596,6	49,2
	FF	71,6	23,3	1203,4	59,5

In the second phase, HSPICE simulation was performed to check the proposed method with transient analysis. During the simulation, the output current value changes from 0 to 1mA and is measured undershoot, settling time values as shown in Fig. 11 , and changes from 1*mA* to 0 and measured overshoot, settling time values as shown in Fig.12 and in Table 4.

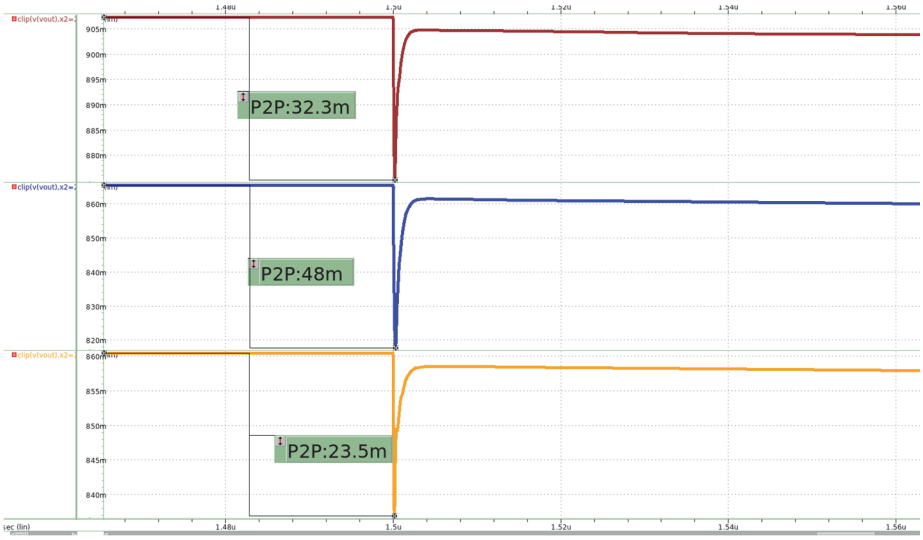

Fig.11. Voltage regulator output voltage with proposed architecture

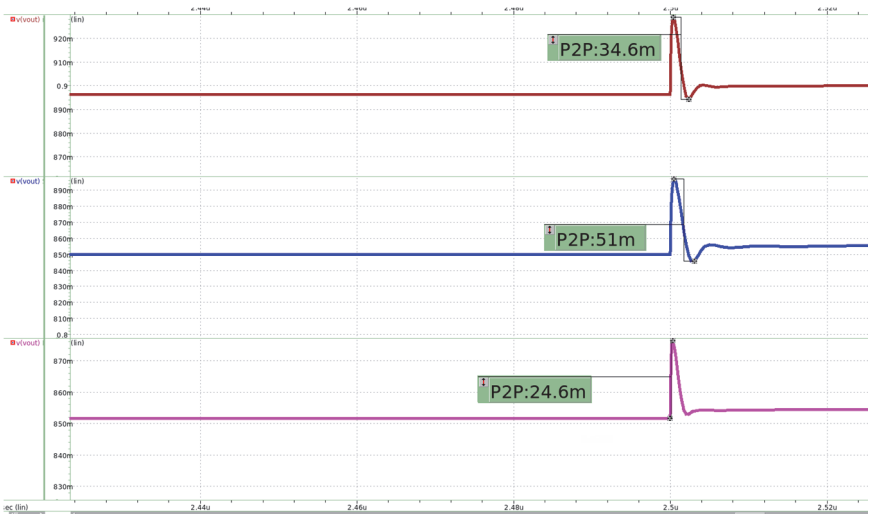

Fig.12. Voltage regulator output voltage with proposed architecture

Table 4

The voltage regulators output measurement results comparison

Measurement	SS	TT	FF
P2P undershoot *(mV)*	38	32,3	23,5
Settling time undershoot *(nS)*	2,87	2,17	1,95
P2P overshoot *(mV)*	51	34,6	24,6
Settling time overshoot *(nS)*	3,07	2,8	2,47

As shown in Table 4, with the proposed version, the drop is three and the settling time is approximately nine times less than in the voltage regulator based on folded cascode opamp.

Conclusion. A voltage regulator based on folded cascode operational amplifier has been designed with the SAED 14 *nm* FinFet technology. A huge voltage drop is observed.

An architecture update has been proposed to reduce the voltage drop. According to the results, the voltage drop is reduced 3 times. But the circuit area and power consumption increase slightly because two stabilizers are added, but this increase is acceptable for the desired results.

The SAED14 *nm* FinFet technology libraries have been used during the HSPICE simulations, and outputs have been exported by Galaxy Custom Designer tool.

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National Polytechnic University of Armenia. The material is received on 08.06.2024.

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ԼԱՐՄԱՆ ԿԱՐԳԱՎՈՐԻՉՆԵՐՈՒՄ ԹԵՐՑԱՏԿԻ ԵՎ ԳԵՐՑԱՏԿԻ ՆՎԱԶԵՑՄԱՆ ՄԵԹՈԴ

Ներկայումս տվյալների փոխանցման արագագործ հաղորդիչ-ընդունիչ հանգույցներում տվյալների և տակտային ազդանշանի հաճախության մեծացմանը զուգընթաց ազդանշանի թրթռոցի դերը ժամանակային սխալանքի մեջ դառնում է նշանակալից։

Ազդանշանի թրթռոցի նվազարկման հիմնական եղանակներից են կապազերծող ունակությունների օգտագործումը և սնուցման լարման կարգավորումը։ Գոյություն ունեն լարման կարգավորման համակարգերի երկու հիմնական խմբեր՝ գծային և փոխանջատվող։ Արագագործ փոխանցման գծերում հիմնականում կիրառվում են լարման կարգավորման գծային համակարգերը, մասնավորապես՝ ցածր անկման կարգավորիչները (Low-dropout regulators)։ Լարման կարգավորման գծային համակարգերի հիմնական առավելություններն են փոքր մակերեսը և ցածր էներգասպառումը՝ ի համեմատ լարման կարգավորման փոխանջատվող համակարգերի։ LDO-ները կարգավորված ելքային լարումը տրամադրում են զգայուն անալոգային սխեմաներին՝ տարբեր բեռի հոսանքների համար, բացասական հետադարձ կապի միջոցով։ LDO-ների մյուս առավելությունը բարձր և ցածր հաճախականային սնման աղմուկների ճնշման մեծ գործակիցն է՝ համեմատած լարման կարգավորման այլ համակարգերի։

Առաջարկված է բեռի փոփոխման պայմաններում LDO-ներում գերլարման նվազարկման մեթոդ։

Առանցքային բառեր՝ հաղորդիչ-ընդունիչ հանգույց, լարման կարգավորման համակարգ, LDO, ազդանշանի թրթռոց, կապազերծող ունակություն ։

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МЕТОД МИНИМИЗАЦИИ ПРОСАДКИ И ПЕРЕРЕГУЛИРОВКИ В РЕГУЛЯТОРАХ НАПРЯЖЕНИЯ

Поскольку в современных схемах передачи - приема данных скорость передачи данных и тактовая частота продолжают расти, дрожание сигнала в общей ошибке синхронизации становится все более значительным в высокоскоростных интерфейсах.

Основными методами минимизации джиттера являются использование декаплирующих конденсаторов и регулирование напряжения питания. Существуют две основные группы регуляторов напряжения: линейные и импульсные. В высокоскоростных приемопередатчиках часто используются линейные регуляторы напряжения, особенно регуляторы с малым падением напряжения (LDO). Основными преимуществами линейных регуляторов напряжения являются малая площадь и энергопотребление по сравнению с импульсными регуляторами. LDO обеспечивает регулируемое выходное напряжение для чувствительных аналоговых схем для различных токов нагрузки с помощью отрицательной обратной связи. Другим преимуществом LDO по сравнению с другими регуляторами является коэффициент подавления высокочастотных и низкочастотных шумов источника питания.

В статье предложен метод снижения перенапряжения в LDO при изменении нагрузки.

Ключевые слова: схема передачи-приема данных, регулятор напряжения LDO, дрожание сигнала, декаплирующий конденсатор.