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V.A. SAHAKYAN

AN ACCURACY IMPROVEMENT TECHNIQUE FOR ON-CHIP CURRENT SOURCES

A new design technique for accuracy improvement of on-chip reference current sources is proposed. A mathematical model has been developed describing the operation of the proposed technique. Based on the obtained equations, the variation of the reference current caused by the changes in operating conditions and process inaccuracies of the technological should not exceed 1…2%. The proposed technique has been implemented in the design of on-chip reference current source circuit in 14 *nm* FinFet technology. Spice simulations performed for the developed circuit show less than ± 5% variation of the reference current in the -40...125^{0}C temperature range considering the process variations in ±3 sigma range. The circuit keeps that accuracy for the supply voltage drop up to 0.66 *V*.

Keywords: on-chip current source, current generators, reference current sources.

Introduction. ICs have found wide application in various systems such as household appliances complex electronic systems, computers, military, aviation, space stations, etc. One of the technical specifications of modern complementary metal-oxide-semiconductor (CMOS) ICs is to ensure high stability of the main parameters, regardless of ambient temperature, supply voltage, and technology deviations. The main parameters of the elements in relation to the typical characteristics may deviate from values reaching tens of percent to multiple [1]. As a result, it becomes clear that the issues of maintaining the stability of various IC parameters have become crucial for chip designers. With the advent of portable devices, the energy consumption and requirements for the IC surface have also tightened, limiting the use of circuits with a large surface area and high energy consumption [2,3]. The design of stable reference voltage sources and the development of voltage stabilizers have also become an important task. The existing deviations in the latest technological processes and new developments, as well as the strict requirements imposed on the IC, have made the need for new methods and solutions urgent conditioned by reducing the deviations in the output values of these nodes and ensuring the safe operation of circuits connected to them as a load [4,5]. The availability of precision voltage sources does not ensure the design of stable current sources. The combination of resistance and a reference voltage source in the MOS structure depends on resistance variation [6,7].

However, in nodes requiring high accuracy, such indicators lead to large deviations either from standard results or the requirements of the technical specification. So, with the development of CMOS technology, a number of difficulties have arisen due to the need of stable current sources, supply voltage values in the IC, the provision of which is an essential reliability indicator.

Statement of the Problem. The modern CMOS IC design process allows the resistance to be produced in two ways: by a transistor operating in a triode mode, or by polysilicon. The resistance of a transistor operating in the triode mode depends on the ambient temperature and technology. Changing the resistance of such a device won't provide high stability of the current source, therefore, the use of such structures in the stable current source design does not make sense:

$$R = \frac{1}{\mu * C_{ox} * W/L * (V_{gs} - V_{th})}.$$

The resistances obtained on the basis of polysilicon is independent of the applied voltage values, and the temperature impact is about 1.5%. While the technology process shifts of result in ± 20% resistance change. So, it becomes clear that the design of stable on-chip current sources are relevant and require the development of new design technique.

The Proposed solution. The block diagram of the current source consists of the following main blocks: PTAT block, voltage and current generator (Fig. 1).

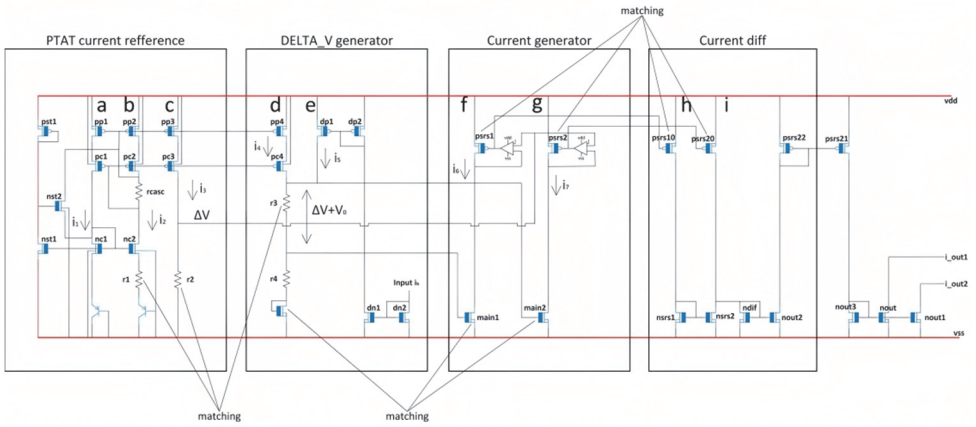

Fig. 1. The block diagram of a high-precision DC current source

It is known that the current flowing through a N-MOS transistor in a linear mode is determined by:

$$I_d = \beta\left[(V_{gs} - V_{th})V_{ds} - 0.5{V_{ds}}^2\right],$$

where

$$\beta = \frac{(W/L)\mu_n \varepsilon_{ox}}{t_{ox}}.$$

Hence, it is obvious that if the transistor dimensions are large, the changes in the remaining parameters under the above influences can be ignored. If the temperature is constant, mobility is a fixed parameter. In cases of all possible processes, the thickness of the oxide layer t_{ox} varies approximately within ± 4.5...5%. If we assume that the temperature is stable, then the change in β will be approximately within 5%. The difference of currents flowing through two N-MOS transistors operating in linear modes will be determined by the expression:

$$I_{d1} - I_{d2} = \beta\left[\left(V_{gs1} - V_{th}\right)V_{ds1} - 0.5{V_{ds1}}^2\right] - \beta\left[\left(V_{gs2} - V_{th}\right)V_{ds2} - 0.5{V_{ds2}}^2\right],$$

$$\Delta I = \beta(V_{gs1} - V_{gs2})V_{ds},$$

$$\beta = \frac{(W/L)\mu_n \varepsilon_{ox}}{t_{ox}},$$

$$\beta(T) = \frac{W}{L}\mu(T_0)\left(\frac{T_0}{T}\right)^{-1.5} = bT^{-1.5},$$

$$\Delta I = \beta\left(V_{gs1} - V_{gs2}\right)V_{ds},$$

$$V_{gs1} - V_{gs2} = \Delta V + V_0.$$

The difference of gate source voltages is designated as $\Delta V+V_0$. It is necessary to get this designation according to the circuit, and imagine that ΔV is the drain source voltage:

$$V_{ds} = \Delta V,$$

where ΔV is the output voltage of the PTAT unit. ΔV is directly proportional to temperature, and V_0 is a voltage independent of temperature,

$$\Delta I = \beta(\Delta V + V_0)\Delta V,$$

$$\Delta I(T) = baT^{-1.5}T(V_0 + aT) = abV_0T^{-0.5} + a^2bT^{0.5}.$$

To understand how the resulting expression depends on the temperature change, it is necessary to derive it in time and get the following expression:

$$\Delta I(T) = baT^{-1.5}T(V_0 + aT) = abV_0T^{-0.5} + a^2bT^{0.5},$$

$$\frac{\partial \Delta I(T)}{\partial T} = -0.5abV_0T^{-1.5} + 0.5a^2bT^{-0.5} = 0.$$

From the graphical presentation of the resulting expression, it can be seen that the current depends on the temperature variation (Fig. 2).

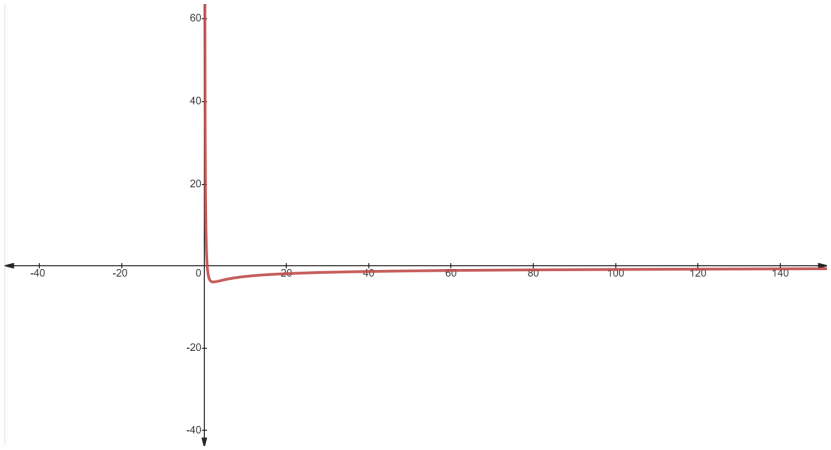

Fig.2. The graphical display of the obtained equality

Simulation Results. To justify the mean of the theoretical analysis Spice simulations for 14 *nm* FinFet technology note has been performed. The dependence of the reference current on several in stabilization factors has been considered and checked. Based on the simulation results, it is possible to reach a less than 3% current change from the temperature variation in the range - 40…125^{0}C (Fig. 3).

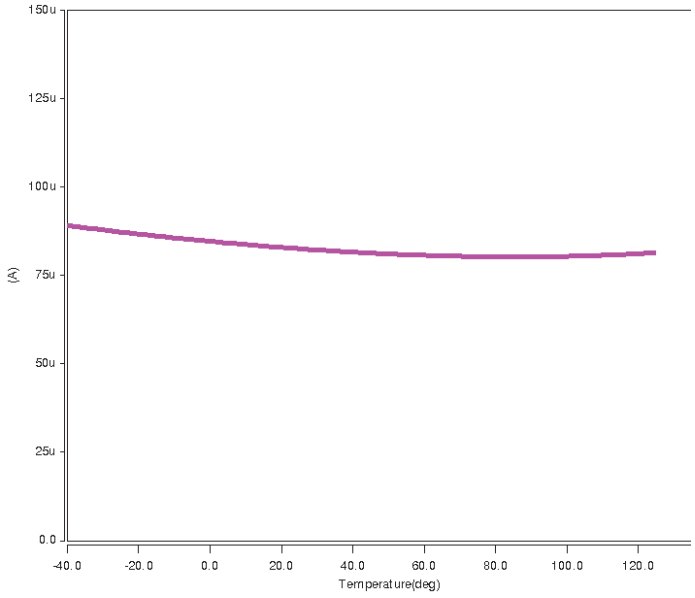

Fig. 3. The dependence of the reference current on the ambient temperature variation

Based on the simulation results, it is possible to reach less than ± 3% current change from the supply voltage and process variations (Fig. 4).

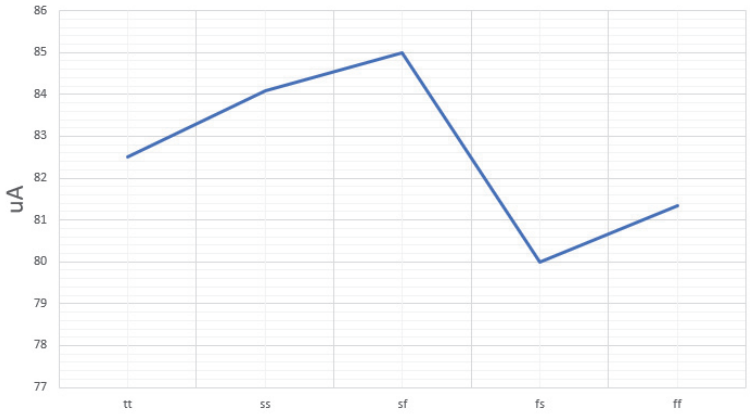

Fig. 4. The dependence of the output current on technological changes

The results show that the reference current variation for the -40…125^{0}C temperature range considering the process variations in ±3 sigma range and supply voltage variation in ±10% range is less than ± 5% (Fig. 5).

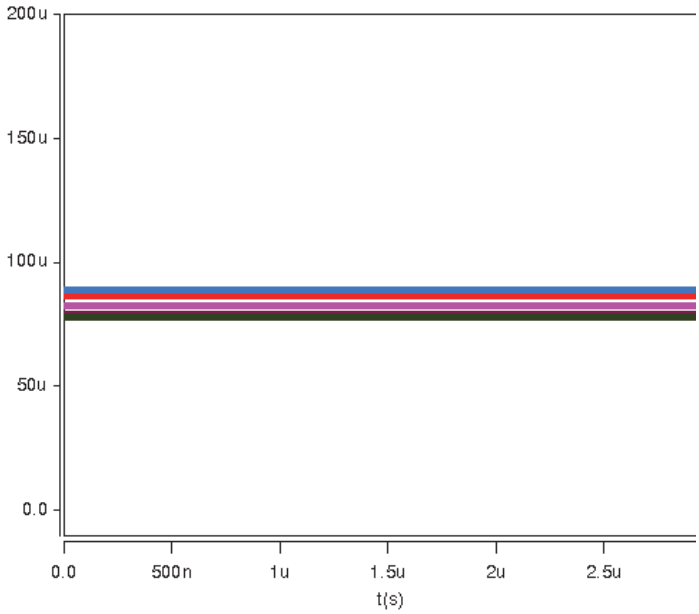

Fig. 5. The dependence of the output current on temperature, as well as supply voltage and technological changes

The next reformed analyze is the power supply noise impact on the designed circuit. The PSRR analysis performed in 100...10^{10} *Hz* ensure more than -10 *dB* noise rejection and more than -35 *dB* rejection in a low frequency range (Fig. 6).

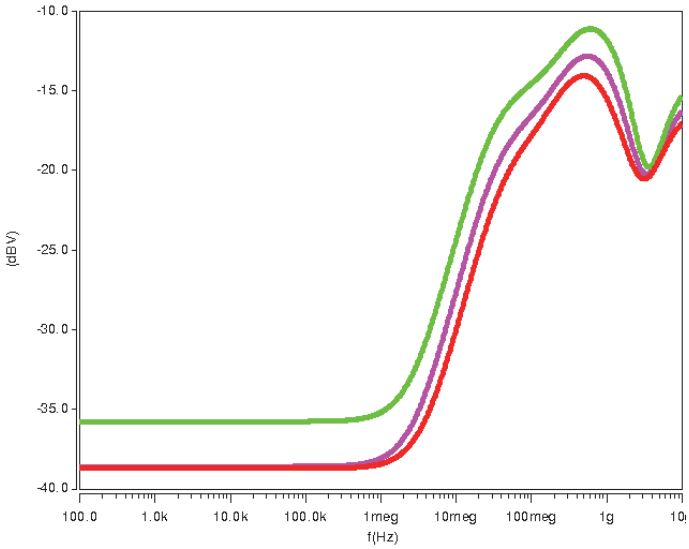

Fig. 6. The results of the frequency analysis

Conclusion. A novel design technique for on-chip current sources has been proposed, designed, and simulated. According to those simulations, the new circuit is capable of providing accurate reference currents and operate in the -40...125^{0}C temperature and ± 10% supply variation ranges by providing around ± 5% variation compared to the existing resistor-based architecture, which provides several times lower accuracy. The main limitation of technique is the usage of bipolar transistors as well as the estimated area increase by 20%. Both requirements are acceptable considering more relaxed requirements for such parts of IC.

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Վ.Ա. ՍԱՀԱԿՅԱՆ

ՆԵՐԲՅՈՒՐԵՂԱՅԻՆ ՀՈՍԱՆՔԻ ԱՂԲՅՈՒՐԻ ՃՇՏՈՒԹՅԱՆ ԲԱՐՁՐԱՑՄԱՆ ԵՂԱՆԱԿ

Առաջարկվել է ներբյուրեղային հոսանքի աղբյուրների ճշգրտության բարձրացման նոր եղանակ: Առաջարկված եղանակի հիմքում ընկած է մշակված մաթեմատիկական մոդելը: Ստացված հավասարումների արդյունքում հիմնավորվել է, որ աշխատանքային պայմանների փոփոխությունների և տեխնոլոգիական գործընթացի անճշտությունների հետևանքով առաջացող հոսանքի շեղումը չպետք է գերազանցի 1-2%: Առաջարկված եղանակն իրականացվել է 14 *նմ* FinFet տեխնոլոգիական գործընթացով՝ ներբյուրեղային հենակային հոսանքի աղբյուրի մշակման համար: Կատարված spice նմանակման արդյունքում, ջերմաստիճանային -40…125°C միջակայքում, տեխնոլոգիական գործընթացի ±3 սիգմա շեղումների դեպքում, մշակված սխեման ապահովել է հենակային հոսանքի ± 5%-ից պակաս շեղումներ: Սխեման ունակ է՝ պահպանելու նշված ճշգրտությունը սնման լարման՝ ընդհուպ մինչև 0,66 *Վ* նվազագույն արժեքի պարագայում:

Առանցքային բառեր. ներբյուրեղային հոսանքի աղբյուր, հոսանքի գեներատորներ, հենակային հոսանքի աղբյուրներ:

В.А. СААКЯН

СПОСОБ ПОВЫШЕНИЯ ТОЧНОСТИ ВНУТРИКРИСТАЛЛИЧЕСКИХ ИСТОЧНИКОВ ТОКА

Предложен метод повышения точности внутрикристаллических источников тока. Предлагаемый метод основан на разработанной математической модели. В результате полученных уравнений установлено, что отклонение тока, вызванное изменением условий работы и неточностями технологического процесса, не должно превышать 1…2%. Предлагаемый метод был реализован с использованием 14 *нм* технологического процесса FinFet для разработки внутрикристаллического эталонного источника тока. В результате экспериментального моделирования в диапазоне температур -40...125°C при отклонениях технологического процесса ±3 сигма разработанная схема обеспечивала ±5% отклонений от эталонного тока. Схема способна поддерживать указанную точность при падении напряжения питания до 0,66 *В*.

Ключевые слова: внутрикристаллический источник тока, генераторы тока, опорные источники тока.