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POWER SNIFFER PERFORMANCE DEGRADATION AND WAYS TO SUPPRESS THE DEVIATION OF THE WORKING PARAMETERS DUE TO RANDOM TECHNOLOGICAL VARIATIONS

One of the most important challenges of modern ICs is power dissipation, particularly the static power dissipation. To be able to reduce static power consumption of an IC, it is separated into different power domains so that the supply power can be turned off for certain domain when not in use. Separate power domains lead to several peculiarities, one of them is the powering up and down the power supply. To represent the supply voltage state by another domain supply, circuits like power sniffers are used. With the evolution of the technologies, the role of random technological variations in the circuits becomes substantial. The paper presents ways to reduce the performance degradation caused by random variations in the 16*nm* technological process node. HSpice tool is used for circuit simulations. Target sigma representing random variations is 5. For every PVT 300 iterations with random variations are run. The results are presented by QQ plots and measurement table. By applying the proposed modifications performance degradation is reduced by around 40% (average for all measured parameters). By implementing the proposed circuit changes the area of the circuit is increasing by around 35%, no power consumption increase is observed.

Keywords: power sniffer, static power, power domain, random technological variations.

Introduction. Power dissipation is one of the most crucial aspects of the modern integrated circuits (ICs). Power dissipation affects the self-heating of the circuits which is one of the most undesirable effects of reliability verification [1,2]. The evolution of the technological process and decrease in transistor channel lengths result in the increase of the portion of static component of the power dissipation in overall power consumption. And if for former technologies, the static power was neglectable compared with dynamic power, in modern ICs, static power consumption can reach up to the dynamic component. In the case when the dynamic power consumption is directly affecting the IC performance and operation frequencies, and in most cases its reduction can cause performance degradation, the static power reduction does not affect the above mentioned aspects. Thus, to reduce the power consumption of the modern ICs, lowering the static power consumption can be a reasonable solution.

Static power consumption is mainly produced from the leakage currents of the transistors. One of the reasons for finFET technology creation is the ability to improve controllability of the transistors (thus to have less leakage current in the cut-off region). Although it was a good solution, in deep sub-micron technologies the issue is again actual. So, the way to cut down the static power consumption is to power down the certain parts of ICs which are not in use at certain time slots. For that reason, there are different power domains in ICs to be able to turn off their power supply. Therefore, there should be some kind of circuits which should ensure safe power-up and power-down of different domains. It is natural that the state of one supply should be represented by another supply. For that reason, the circuit called power sniffer is used to notify to other circuits about the state of a certain domain power. Also, power sniffers should ensure noise immunity as its output should not switch in case of noise on the observed supply. In other words, the switching thresholds for power-up and power-down should be different (the circuit should have hysteresis).

Considering the effects of technological imperfections during the design process is one of the critical aspects. The basic approach is to test the circuit for different transistor types, voltages and temperature ranges. But more sensitive/ critical circuits should be checked for more pessimistic cases. For that reason, simulations can be run taking into account random technological variations [3,4]. In other words, when simulating the circuit for certain process, voltage and temperature (PVT), the simulator can run multiple simulations each time varying the parameters of the circuit elements in random order, in a given deviation range. So, when checking the circuit with regular simulations, it may meet the specifications, but with simulations with random variations it may fail the specifications, up to having functional fails. That is the reason that simulations with random variations must be run for sensitive circuits.

Section 1 discusses the power sniffer circuit and its operation. Section 2 represents the simulation results with the initial circuit. Section 3 proposes ways to improve performance and shows the simulation results with implemented changes. The summary of the paper is in Section 4.

1. Power sniffer circuit and operation. The power sniffer circuit is presented (Fig. 1). As discussed in the previous section, it should indicate the presence of one power supply with another one. In the circuit presented in this paper, the active power supply (the main supply of the circuit) has high voltage level, and the observed signal has low voltage level (which is given to the input of the circuit). To avoid overvoltage issues the circuit is constructed using thick oxide or high voltage threshold (HVT) transistors. The main idea of the circuit is to change the switching

threshold of the circuit depending on the direction of switching of the input. By that the circuit eliminates the cases when the output will switch because of noises on the input signal. In other words, to be able to accurately indicate the ramp-up and ramp-down of the observed power supply. Shifting the switching threshold voltage is done by changing the pull-up and pull-down driving forces of the first stage of the circuit. It is implemented by MNFB and MPFB transistors which are shorting the middle net of the pull-up/down parts to high voltage power/ground. As the input of the circuit is low-voltage and cannot fully open the MNIN1 and MNIN2 transistors, to be able to calibrate the pull-up strength (compared with pull-down), resistors are used for the pull-up part. In other words, sizes of MNIN1 and MNIN2 transistors are set in a way to be able to set the logic low level signal on net out0 (lower than switching point of the inverter MN0/MP0). The inverted logic level of out0 is given to MNFB and MPFB transistors by a feedback inverter. The circuit is also performing level shifting (the input is low and the output is high voltage level). The circuit is calibrated with a 25*fF* output load.

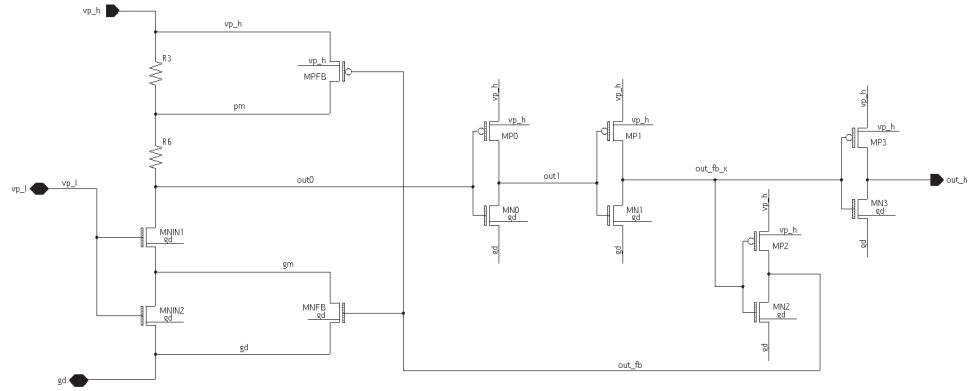

Fig. 1. Power sniffer circuit

Table 1

Simulation conditions

Parameter	**Value**
Transistor types	TT, FF, SS
NMOS capacitance type	T, F, S
Resistor type	T, F, S
Supply voltage (*V*)	1.1 +/-10%
Temperature (*C*)	-40, 25, 125
Input voltage nominal value (*V*)	0.8

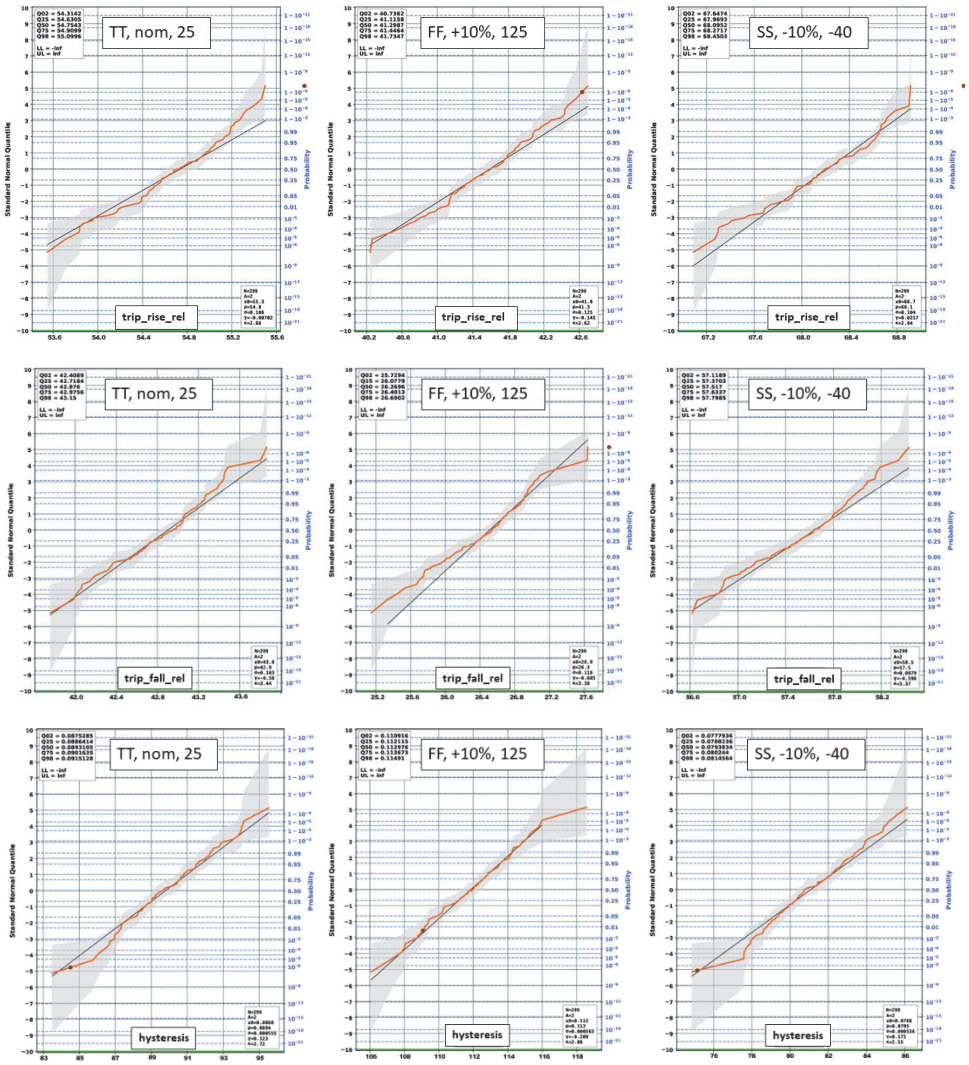

Fig. 2. QQ plots of the initial circuit

2. The simulation results of the initial circuit. The circuit is using 16 *nm* technological process HVT transistors. All simulations are done using HSpice tool [5]. Simulation conditions are presented in Table 1. Simulations performed for all combinations of PVT. To test the circuit, a triangle signal to the input is applied with a 1 millisecond rise and fall times (the typical time for power supply to turn on/off) which represents low voltage input power supply ramp-up and ramp-down. The following parameters will be observed for checking the functionality: the trip point of the input signal for output rising, the trip point of the input signal for

output falling, hysteresis of the circuit. The rising and falling trip points are calculated in percents regarding vp_l input supply voltage (as the supply voltage differs between PVTs). The target sigma for variations is 5. As the circuit has less than 100 devices, for every PVT 300 iterations with random violations are run (in that case the majority of the parameter distribution values are obtained). Simulation results with QQ plots are presented (Fig. 2).

3. The improved circuit, simulation results. The power sniffer circuit with modifications is presented (Fig. 3). Capacitors with MNCFB and MPCFB transistors are added to the feedback line, in the pull-down part the regular NMOS transistors are replaced with stack transistors connected in parallel, in the pull-up part single resistors are replaced with multiple smaller nominal resistors connected in series. MNCFB and MPCFB transistors are correspondingly in deep well and separate N-well to be able to connect the bulks to source and drain terminals to create effective device capacitances. As the power/ground should switch from its regular place to the middle point of resistors/input NMOS transistors, there is a voltage settling issue. The transition should be quick and stable to avoid false switchings due to power noise.

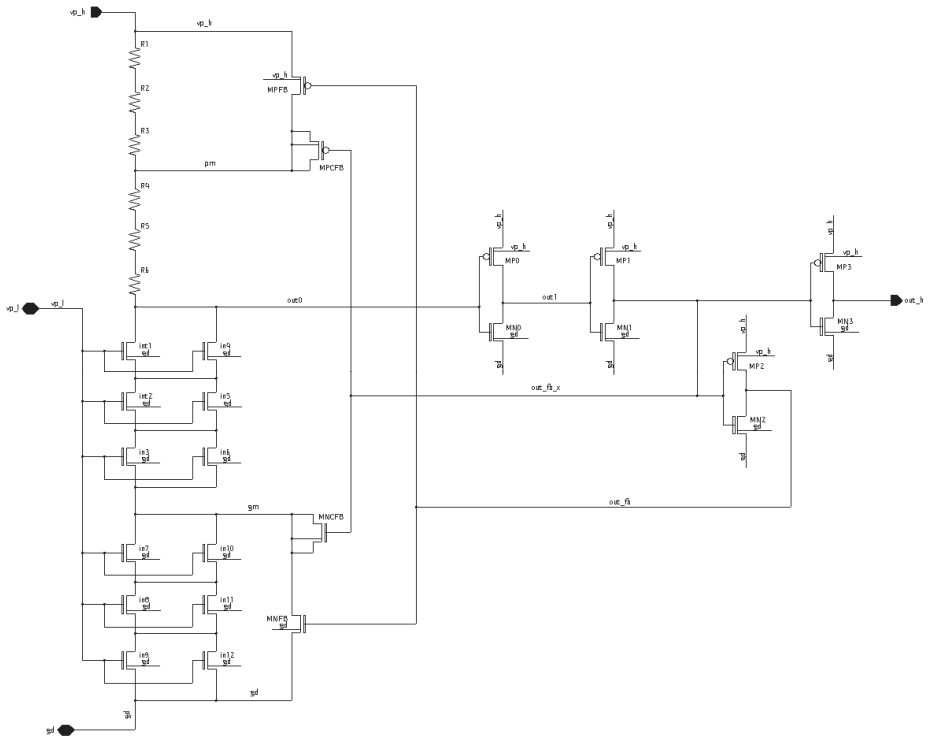

Fig. 3. A modified power sniffer circuit

Observe the pull-up part for example. When the input power is on (has nominal voltage value), the circuit power is in its regular place. That means that the gate of MPFB is logic 1 so the gate of MPCFB is logic 0 and pm net voltage is around half of the power. When the output of the circuit switches (due to input switching), prior to opening of MPFB transistor (due to MP2, MN2 inverter delay) the MPCFB capacitance pulls the pm net higher as the gate of MPCFB is switching from 0 to 1, which leads to a quicker settlement of power on pm net. By that we prevent the circuit from bouncing around switching points.

The same process is happening in the pull-down part. On the other hand, by stacking the NMOS transistors the effect of long channel length is achieved which helps to reduce the negative effects from the process variation (particularly channel length modulation). Also, when stacked, to achieve same current carrying capability, parallel legs of transistors are added. By that, the variations are kind of spread between a bigger number of transistors. In that case, the probability that the random variations would be in the same direction for more transistors is less, which leads to better simulation results. For the same reason, simulation results are better for series connection of more resistors with smaller nominals.

Simulation results' QQ plots for modified circuit and comparison table are presented (Fig. 4, Table 2).

From the QQ plots, it can be observed that the data of the updated circuit is closer to normal distribution compared with the initial circuit simulation results. The worst-case results of all PVT corners' simulations are presented in table 2. The average value, minimum and maximum values of median +/- target sigma are shown for rising and falling tripping points and hysteresis. Also, the deviation of the results is presented for initial and updated circuits. The hysteresis is calculated by subtraction of rising and falling tripping points, expressed by absolute values, so the hysteresis unit is millivolt.

The rising and falling tripping points are expressed relative to power supply in percents as the supply voltages for different simulation corners are different. From the simulation results it can be seen that the parameter degradations of the updated circuit are around 40% less compared with the initial design.

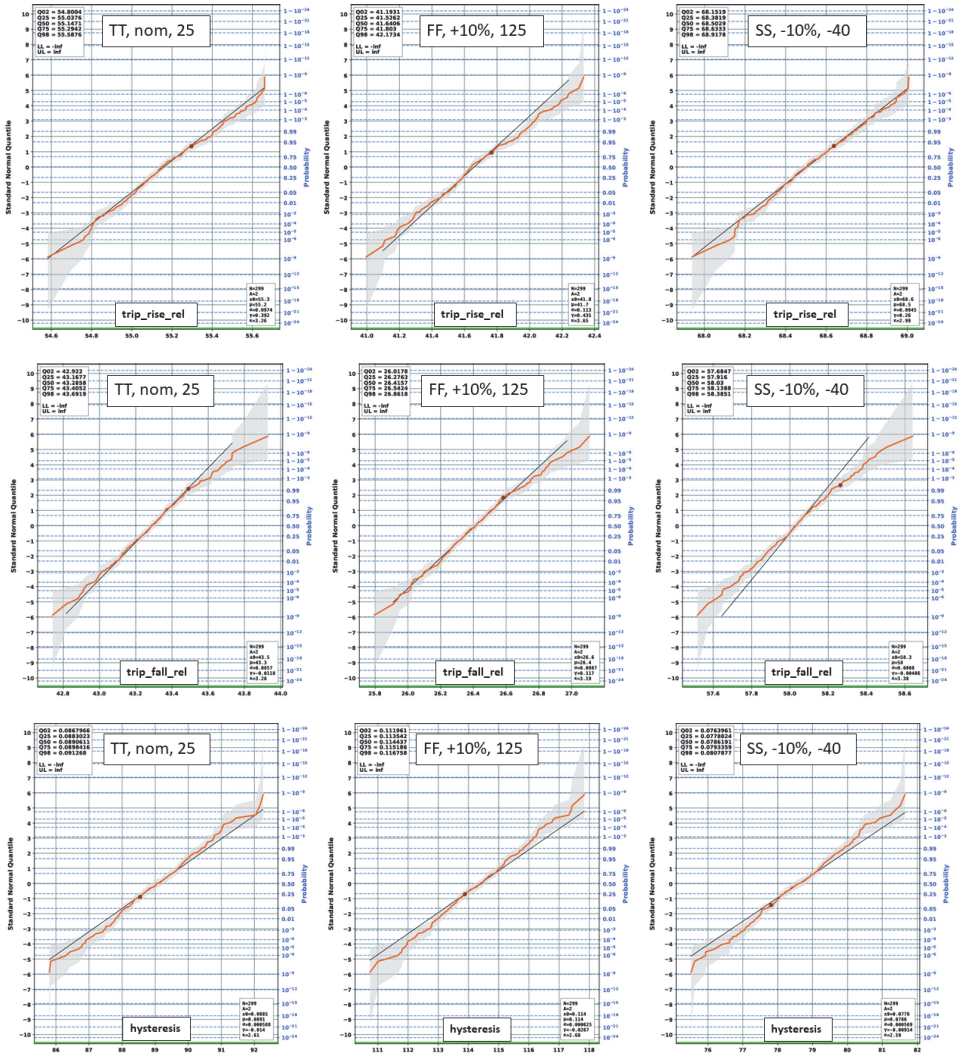

Fig. 4. The QQ plots of the modified circuit

The drawback of the proposed modifications is that by adding the capacitances, placing them in separate wells, increasing number of NMOS transistors and pull-up resistors, the area of the circuit is increasing by around 35%. Power consumption of the circuit is not a critical parameter as this circuit consumes power only when the input supply voltage is turned on or off (whose frequency is not comparable with clocking signal frequencies). But overall, after the changes, the circuit power is practically the same as the current in serial connected pull-up and pull-down part is kept the same and the energy of the added capacitance is kept within the circuit.

Table 2

Simulation results

Parameter		Initial design			Modified design			Deviation (initial/ modified)
		Median+/- target sigma (*min*)	Mean	Median+/- target sigma (*max*)	Median+/- target sigma (*min*)	Mean	Median+/- target sigma (*max*)	
Hysteresis (mV)	TT	85.4	89.8	94.9	85.8	89.1	92.2	9.5/6.4
	FF	107.6	112.9	117.7	110.8	114.3	117.6	10.1/6.8
	SS	75.8	79.5	84.6	75.5	78.6	81.5	8.8/6.0
Rise trip point relative to supply voltage (%)	TT	53.7	54.7	55.6	54.6	55.1	55.6	1.9/1
	FF	40.3	41.3	42.7	41.0	41.6	42.3	2.4/1.3
	SS	67.2	68.1	69.0	68.0	68.5	69.0	1.8/1
Fall trip point relative to supply voltage (%)	TT	41.9	42.8	43.9	42.7	43.2	43.8	2.0/1.1
	FF	25.2	26.2	27.4	25.8	26.4	27.0	2.2/1.2
	SS	56.6	57.5	58.3	57.6	58.0	58.5	1.7/0.9

Conclusion. Circuit modifications are presented to reduce the performance degradation in power sniffer circuit caused by random variations. In the paper 16nm technological process is used. For simulations HSpice tool is used. Target sigma for variations is 5. For a single PVT 300 iterations of simulations are run. By applying the proposed modifications the performance degradation is reduced by around 40%, which is average for all the measured parameters. Also, the data of the updated circuit is closer to normal distribution compared with the initial circuit. The implementation of the suggested changes in the circuit increases the area of the circuit by around 35%, no power consumption increase is observed.

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Վ.Ս. ԳԵՎՈՐԳՅԱՆ

ՊԱՏԱՀԱԿԱՆ ՏԵԽՆՈԼՈԳԻԱԿԱՆ ՇԵՂՈՒՄՆԵՐԻ ՀԵՏԵՎԱՆՔՈՎ ՍՆՄԱՆ ՎԻՃԱԿԻ ՈՐՈՇՄԱՆ ՇՂԹԱՆԵՐՈՒՄ ԱՇԽԱՏԱՆՔԱՅԻՆ ՊԱՐԱՄԵՏՐԵՐԻ ՎԱՏԹԱՐԱՑՈՒՄԸ ԵՎ ԴՐԱՆՑ ՑՐՎԱԾՈՒԹՅԱՆ ՆՎԱԶԵՑՄԱՆ ՄԻՋՈՑՆԵՐԸ

Արդի ինտեգրալ սխեմաների նախագծման մարտահրավերներից է էներգասպառումը, մասնավորապես՝ ստատիկ էներգասպառումը: Ստատիկ էներգասպառումը նվազեցնելու նպատակով ինտեգրալ սխեման բաժանվում է սնուցման տարբեր կղզյակների, որպեսզի դրանց սնման լարումները հնարավոր լինի անջատել, երբ դրանք չեն օգտագործվում: Կղզյակների բաժանումը հանգեցնում է մի շարք առանձնահատկությունների, որոնցից են սնման լարման միացումն ու անջատումը: Մի կղզյակի սնման լարման վիճակը մեկ այլ կղզյակի լարումով արտահայտելու համար օգտագործվում են սնման վիճակի որոշման շղթաներ: Տեխնոլոգիական գործընթացի զարգացմանը զուգընթաց տեխնոլոգիական պատահական շեղումների դերը մեծանում է: Հոդվածում նկարագրված են 16նմ տեխնոլոգիական գործընթացում պատահական շեղումներից առաջացած շղթայի աշխատանքային պարամետրերի շեղումները փոքրացնելու ուղիներ: Շղթաների նմանարկման համար օգտագործվել է HSpice ծրագրային միջոցը: Պատահական շեղումների թիրախային չափը 5 սիգմա է: Ամեն ԳԼՋ-ի համար կատարվել է 300 շեղումներով նմանարկում: Արդյունքները ներկայացված են QQ գրաֆիկներով և տվյալների աղյուսակով: Առաջարկվող փոփոխությունները կատարելուց հետո աշխատանքային պարամետրերի վատթարացումը նվազել է մոտավորապես 40%-ով (միջինացված բոլոր հաշվարկվող պարամետրերի համար): Արդյունքում շղթայի մակերեսը մեծանում է մոտավորապես 35%-ով, էնեգասպառման աճ չի դիտարկվում:

Առանցքային բառեր. սնման վիճակի որոշման շղթա, ստատիկ էներգասպառում, սնուցման կղզյակ, պատահական տեխնոլոգիական շեղում:

В.С. ГЕВОРГЯН

УХУДШЕНИЕ ПРОИЗВОДИТЕЛЬНОСТИ АНАЛИЗАТОРА ПИТАНИЯ ИЗ-ЗА СЛУЧАЙНЫХ ТЕХНОЛОГИЧЕСКИХ ОТКЛОНЕНИЙ И СПОСОБЫ ПОДАВЛЕНИЯ ИЗМЕНЕНИЙ ЕГО РАБОЧИХ ПАРАМЕТРОВ

Одним из наиболее важных вызовов современных интегральных схем является рассеивание мощности, особенно статическое рассеивание. Для снижения статического энергопотребления микросхемы она разделена на разные домены напряжений, чтобы можно было отключить питание для определенного домена, когда он не используется. Отдельные домены питания имеют некоторые особенности, одна из которых — включение и выключение источника питания. Чтобы представить состояние напряжения питания с помощью источника питания другого домена, используются такие схемы, как анализаторы питания. С развитием технологий роль случайных технологических отклонений в схемах становится существенной. В статье представлены способы снижения отклонений, вызванных случайными изменениями в 16*нм* технологическом процессе. Инструмент HSpice используется для моделирования схем. Целевая сигма, представляющая случайные вариации, равна 5. Для каждого процесса, напряжения и температуры выполняется 300 итераций со случайными вариациями. Результаты представлены в виде графиков QQ и таблицы. При применении предложенных модификаций деградация производительности снижается примерно на 40% (в среднем по всем измеряемым параметрам). При реализации предложенных схемных изменений площадь схемы увеличивается примерно на 35%, роста энергопотребления не наблюдается.

Ключевые слова: анализатор питания, статическое энергопотребление, домен напряжения, случайные технологические отклонения.