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IBIS MODEL ACCURACY IMPROVEMENT USING VARIABLE STEP

In all times of integrated circuits (IC) manufacturing, the speed of getting the product on the market has been the main problem for all manufacturers. The main reason for late products has always been the speed of the tools that carry out the testing. The main simulator used by every manufacturer is the SPICE simulator, but with the SPICE simulator it can take up to months to simulate the whole TXRX macro. But since the 1990s with the introduction of the I/O Buffer Information Specification (IBIS) models, the testing time has decreased dramatically.

A method is proposed to generate IBIS models with a variable step, that will help to increase the accuracy of the IBIS model during signal integrity (SI) simulations and will correlate with SPICE simulations better. The proposed method can be implemented for all types of TX drivers and IBIS models.

Keywords: transmitter, signal integrity, variable step, accuracy, IBIS.

Introduction. From the start of integrated circuit (IC) design, SPICE simulation has always been used in areas such as IC design to simulate the design because of its high level of accuracy. However, at the system level, the SPICE simulation has a few cons for the user and the device manufacturer. SPICE simulations could only model a circuit at the transistor level, so the simulator should have exact information about the circuit and PVT parameters. Many IC vendors consider this type of information unacceptable and avoid making their models available to the public. Even though SPICE simulations are very accurate, simulation speeds are very slow for transient simulation analysis, which is often used when assessing signal integrity performance. Also, not all SPICE simulators are fully compatible. Default simulator options may also differ with different SPICE simulators. Because some very essential options control accuracy, convergence, and algorithm type, any inconsistency in options may produce poor correlation in simulation results between different simulators. As SPICE variants exist, models are often incompatible between simulators so they should be extracted for a specific simulator. Another choice for SPICE simulation is I/O Buffer Information Specification (IBIS) [1]. Intel initially developed IBIS to give customers access to accurate I/O buffer models without risking their intellectual property. The core of the IBIS model consists of Vt, It, Iv,

and capacitance tables. At first, the IBIS models included only 2 types of tables: current vs. voltage (Iv) and voltage vs. time (Vt). But because IBIS models were just models for TX, they would not give the same result as the SPICE simulation. That is why the standard of the IBIS models has changed since then. During the development of the IBIS model, developers created a new type of IBIS model called IBIS-AMI [1].

The If simulations are used for calculating the capacitance value on the output and the power rails. The clamp simulation is used for characterizing the ESD diodes on the output. Then the characterization tool uses the DEC algorithm to get power and ground clamp values. The pullup and pulldown simulations are used for calculating the impedance of pullup (PU) and pulldown (PD) segments respectively. The resistance is calculated on the termination voltage, which is VDDQ/2 for most cases. ISSO_PU and ISSO_PD simulations are used to calculate the noise coming from the power and ground rails. The Vt waveforms are used to see the transition speed, the VOH an VOL values. The rise/fall_gnd and rise/fall_sup differ from each other by the 50 *Ohms* termination resistance (for _sup simulation, the resistance is connected to the VDDQ and for _gnd simulation, it is connected to the ground). For these simulations, the input signal is ideal (1 *ps* transition time) as per IBIS standard. The testbenches for It and Vt simulations are the same except for the probe values. The impedance of the IBIS models can be calculated from the pullup(pulldown) and Vt simulations [2]. Three-state output buffer consists of pull up/down characteristics, ESD structure and package parameters (Fig. 1).

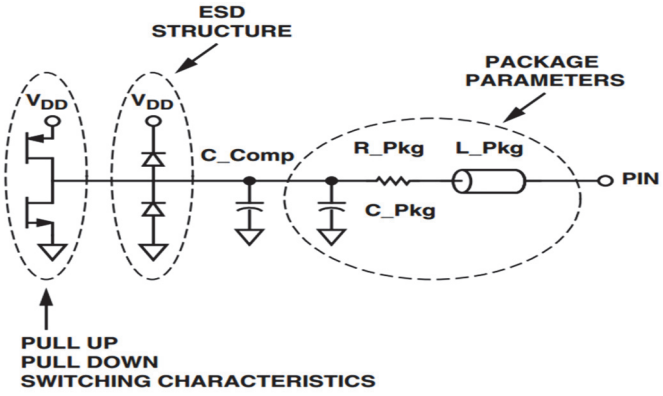

Fig. 1. Three-State Output Buffer

In case of the ISSO_PU simulation, the driver is in a high state, the voltage source of the VDD sweeps form –VDDQ to VDDQ. In case of ISSO_PD simulation the driver is in a low state and the voltage source of the VDD sweeps

form –VDDQ to VDDQ. In case of pullup/pulldown simulation the driver is in a high/low state, voltage source of the VDD and voltage source of the VSS have DC values and the Vtable_1 sweeps form –VDDQ to 2*VDDQ. The GND and power clamp data need to be subtracted from the pull-up and pull-down data. Otherwise, the simulator takes this into account twice. The ramp rate (dV/dt) describes the transition time when the output is switching from the current logic state to another logic state. It is measured at the 20% and 80% points with a default resistive load of 50 *Ohm*. The falling and rising waveforms show the time it takes the device to go from a high to low and from a low to high when driving a resistive load connected to ground and VDD. For a standard push/pull CMOS, four different waveforms can be generated: two rising and two falling (Fig. 2). In each case, one is with the load connected to VDD and the other with the load connected to GND.

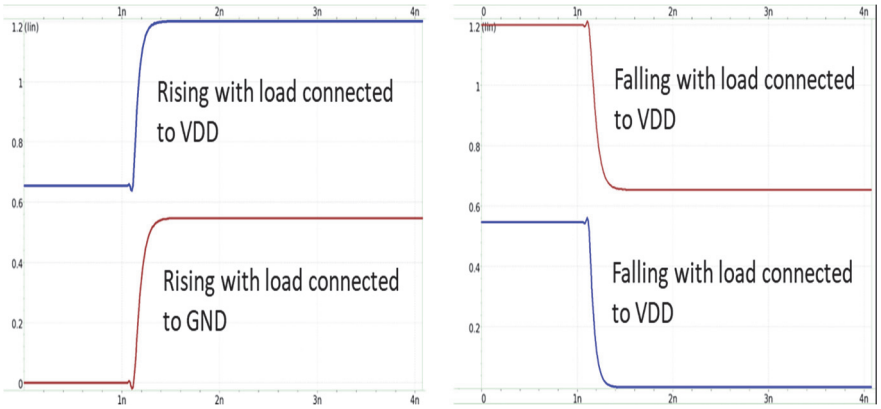

Fig. 2. V-T waveforms of IBIS model with both terminations

Currently used IBIS models and their restrictions. There are types of IBIS models that are currently being used. The first one is called clipped IBIS model which contains all Iv and If tables but contain only the edge part of the Vt and It tables [3]**.** The Vt and It tables have 1 *ps* step which gives better accuracy for edges. But for higher frequencies it is not good to use clipped model, as it may not include correct VOH and VOL as well as overshoot and undershoot [4]. This may cause to a bad correlation with SPICE simulations on high frequencies. That is why non_clipped IBIS models are used to exclude those mismatches. But with non_clipped models, the edge of Vt and It waveforms have 10 *ps* step due to table data point restriction. The restriction states that IBIS model table should not contain more than 999 data points, or the ibischk6 parser will find errors in the IBIS model, and the simulator that will be used for IBIS simulations will not parse the data correctly [5]. To show the comparison of correlations between 10 *ps* step IBIS vs SPICE and 1 *ps* IBIS vs SPICE simulations have been done (Fig. 3).

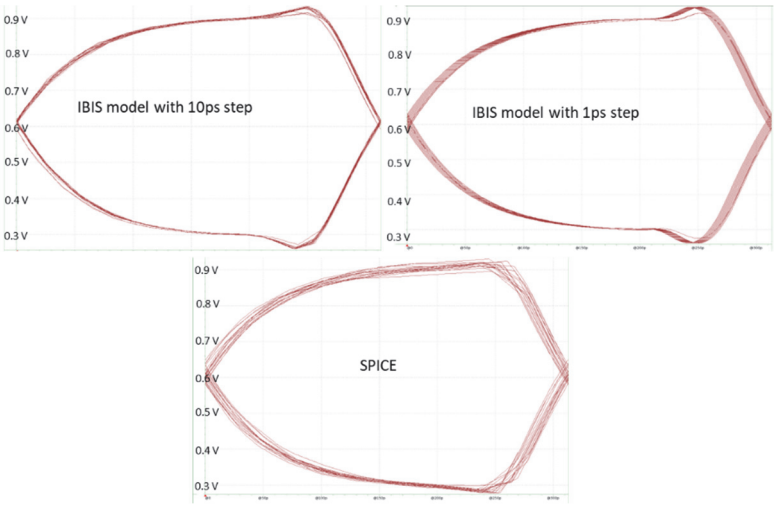

Fig. 3. Simulation results with 10ps,1ps IBIS models and the SPICE

The proposed solution and simulation results. To exclude the restrictions that clipped and non_clipped models have, it is proposed to have an IBIS model with a variable step, where the edge of the Vt and It waveforms have 1 *ps* step size and the DC portions of the waveforms have variable steps. This way the edge will be most accurate, and there will be no loses as in clipped model. This approach will give an opportunity to have better correlation with SPICE. To achieve that, automation script has been developed which separates the edge part from the DC part and generates the IBIS tables with separate steps by considering that the combined data points should not exceed 999 data points. The start and end points of the edge are given by the user. The user should open the Vt and It raw SPICE data, check the start and end points of the edge and manually put those values in the automation script [6].

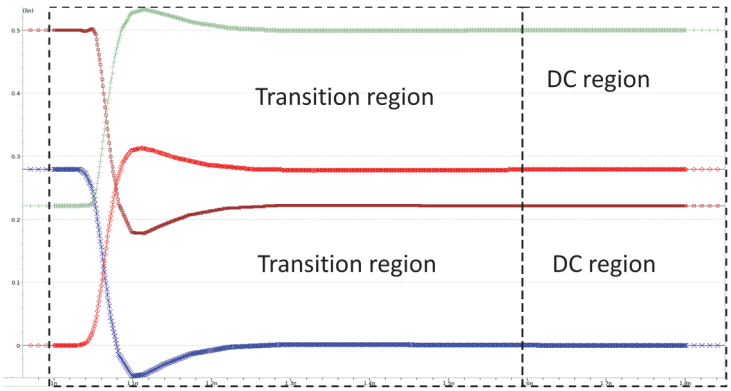

Fig. 4. Transition and DC regions of the Vt and It waveforms

Fig. 4 shows the transition and DC regions of the Vt and It waveforms. During the variable step IBIS model generation, the user should take into account the transition time start and end point of all PVT corners. As the IBIS model includes tables for 3 PVT corners the end point should be the value of the furthest end point between PVT corners. Generally, it is the value of the SS corner because the edge of the SS corner is the slowest [7]. This approach can also be used to exclude overclocking issues during high frequency simulations [8]. The Table below shows the results of 3 IBIS models (10 *ps* step,1 *ps* step and variables step) and the SPICE simulations.

Table

Summary table

	Crosspoint (*mV*)	EYE height (*mV*)	EYE width (*ps*)
SPICE	128	283	313
1 *ps* IBIS model	133	283	312
10 *ps* IBIS model	135	283	311
Variable step IBIS model	129	283	313

Simulations results of the Table above are taken from the EYE diagram (Fig. 5).

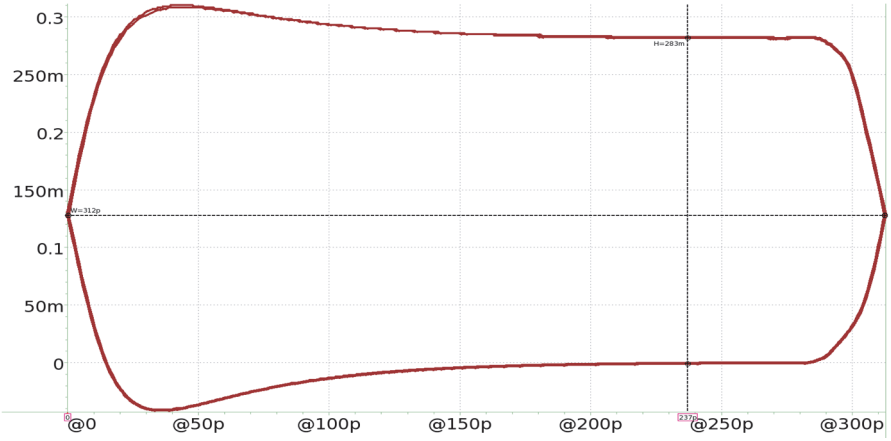

Fig. 5. EYE diagram

Conclusion. A new approach to increase the accuracy of the IBIS model has been proposed and designed using the Galaxy Custom Designer tool [9]. The two types of the IBIS models have been discussed and pointed out the limitations of those models. The new approach gives an opportunity to have an IBIS model that correlates with SPICE better than the other two models, exclude the overclocking issues for high frequency IBIS models. To exclude human error while generating the variable step IBIS model, automation script has been developed.

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ՓՈՓՈԽԱԿԱՆ ՔԱՅԼԻ ՕԳՏԱԳՈՐԾՄԱՄԲ ՄՈՒՏՔ/ԵԼՔ ԿՐԿՆԻՉԻ ՏԵՂԵԿԱՏՎՈՒԹՅԱՆ ՄՈԴԵԼԻ ՃՇՏՈՒԹՅԱՆ ԼԱՎԱՐԿՈՒՄԸ

Ինտեգրալ սխեմաների արտադրության՝ բոլոր ժամանակներում արտադրանքը շուկա դուրս բերելու արագությունը եղել է բոլոր արտադրողների հիմնական խնդիրը: Ապրանքների ուշացման հիմնական պատճառը միշտ եղել է փորձարկում կատարող գործիքների արագագործության ունակությունը: Հիմնական սիմուլյատորը, որն օգտագործում է յուրաքանչյուր արտադրող, SPICE նմանակման գործիքն է, որով փորձարկումը կարող է տևել մինչև ամիսներ ամբողջ հաղորդիչ/ընդունիչ հանգույցի մոդելավորման դեպքում: Սակայն 1990-ականներից սկսած, մուտք/ելք կրկնիչի տեղեկատվության (ՄԵԿՏ) մոդելների ներդրմամբ, թեստավորման ժամանակը կտրուկ նվազել է:

Առաջարկվում է փոփոխական քայլով ՄԵԿՏ մոդելներ ստեղծելու մեթոդ, որը կօգնի՝ բարձրացնելու ՄԵԿՏ մոդելի ճշգրտությունը ազդանշանի ամբողջականության մոդելավորման ժամանակ և ավելի լավ կկապակցի SPICE սիմուլյացիաների հետ: Առաջարկվող մեթոդը կարող է կիրառվել բոլոր տեսակի հաղորդիչ հանգույցների և ՄԵԿՏ մոդելների դեպքում:

Առանցքային բառեր. հաղորդիչ, ազդանշանի ամբողջականություն, փոփոխական քայլ, ճշտություն, ՄԵԿՏ:

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ПОВЫШЕНИЕ ТОЧНОСТИ МОДЕЛИ СПЕЦИФИКАЦИИ ИНФОРМАЦИИ О БУФЕРЕ ВВОДА/ВЫВОДА С ПОМОЩЬЮ ПЕРЕМЕННОГО ШАГА

Во все времена производства микросхем скорость вывода продукта на рынок была главной проблемой для всех производителей. Основной причиной позднего выпуска продуктов всегда была скорость инструментов, выполняющих тестирование. Основным симулятором, который использует каждый производитель, является SPICE, но с его помощью моделирование всего макроса TXRX может занять несколько месяцев. Начиная с 1990-х годов, с появлением моделей спецификации информации о буфере ввода/вывода (СИБВ), время тестирования резко сократилось.

Предлагается метод генерации моделей СИБВ с переменным шагом, который позволит повысить точность модели СИБВ во время моделирования целостности сигнала и будет лучше коррелировать с моделированием SPICE. Предложенный метод может быть реализован для всех типов драйверов и моделей СИБВ.

Ключевые слова: передатчик, целостность сигнала, переменный шаг, точность, СИБВ.