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IBIS MODEL OUTPUT IMPEDANCE CORRECTION APPROACH USING CCCS

With the CMOS technology size scaling aggressively and the transmitter (TX) output resistance becoming smaller and smaller, it becomes necessary to have a good impedance correlation between TX and receiver (RX). The mismatch between the impedances can cause a noise and a response which will dramatically decrease the efficiency of the circuit. Nowadays, those mismatches are being tested using IBIS (Input/output Buffer Information Specification) models owing to low cost and testing speed.

A method is proposed to use a current-controlled current source (CCCS) which will decrease the mismatch and make it less than 1%. The proposed method can be implemented for all types of TX drivers and IBIS models.

Keywords: transmitter, receiver, impedance mismatch, CCCS, IBIS.

Introduction. In all times of IC manufacturing, the speed of getting your product on the market has been the main problem for all manufacturers. The main reason for late products has always been the speed of the tools that do the testing. The main simulator which every manufacturer uses is the SPICE simulator, but with the SPICE simulator it can take up to months to simulate the whole TXRX macro. But since the 1990s with the introduction of the IBIS models, the testing time has decreased dramatically [1]. At first, the IBIS models included only 2 types of tables current vs. voltage (Iv) and voltage vs. time (Vt). But because IBIS models were just models for TX, they wouldn't give the same result as the SPICE simulation. That is why, the standard of the IBIS models has changed since then. During the development of the IBIS model, developers created a new type of IBIS model called IBIS-AMI. IBIS-AMI models run in a special-purpose SerDes channel simulator, not in a SPICE-like simulator and consist of two text files (*.ibs and *.ami) plus a platform-specific machine code executable file (*.dll on Windows, *.so on Linux). IBIS-AMI support statistical and so-called time-domain channel simulations, and three types of IC model ("impulse-only," "GetWave-only," and "dual mode"). Nowadays the standard IBIS model has a wider usage than the IBIS-AMI model. The standard IBIS model includes 16 simulations for each PVT corner which can be seen in Fig. 1. The simulation can be divided into four groups, which are Iv (current vs. voltage), Vt (voltage vs. time), If (current vs. frequency) and It (current vs. time).

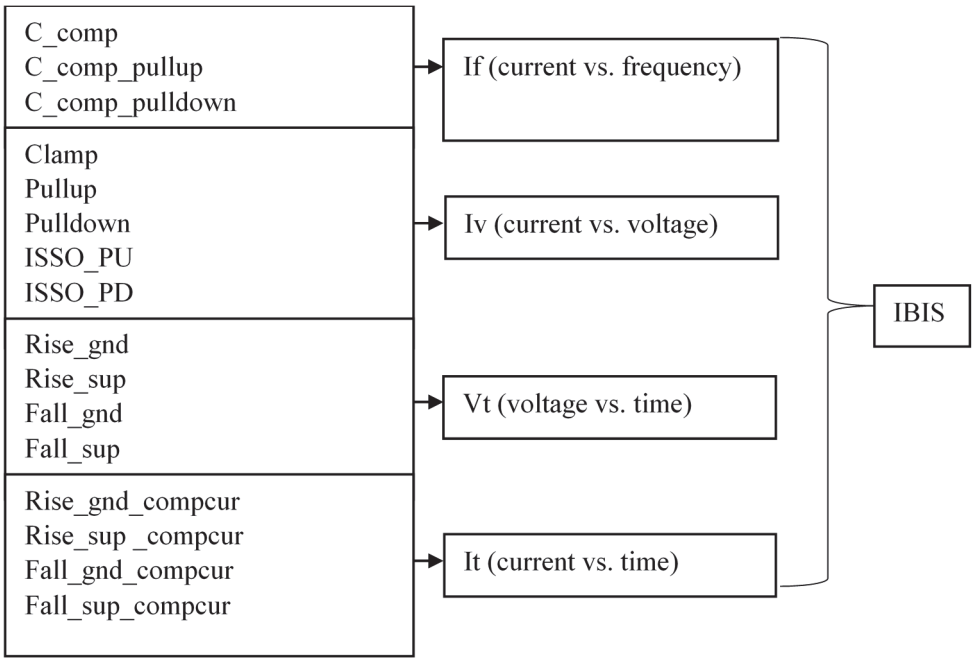


Fig. 1. Simulations needed for IBIS generation

The If simulations are used for calculating the capacitance value on the output and the power rails. The clamp simulation is used for characterizing the ESD diodes on the output. Then the characterization tool uses the DEC algorithm to get power and ground clamp values. The pullup and pulldown simulations are used for calculating the impedance of pullup (PU) and pulldown (PD) segments respectively. The resistance is calculated on the termination voltage, which is VDDQ/2 for most cases. ISSO_PU and ISSO_PD simulations are used to calculate the noise coming from the power and ground rails. The Vt waveforms are used to see the transition speed, the VOH an VOL values. The rise(fall)_gnd and rise (fall)_sup differ from each other by the 50 *Ohms* termination resistance (for _sup simulation the resistance is connected to the VDDQ and for _gnd simulation it is connected to the ground). For these simulations, the input signal is ideal (1p transition time) as per IBIS standard. The testbenches for It and Vt simulations are the same except for the probe values. The impedance of the IBIS models can be calculated from the pullup(pulldown) and Vt simulations. The testbenches for the Vt(It) can be seen in Fig. 2 and Iv tables can be seen in Fig. 3.

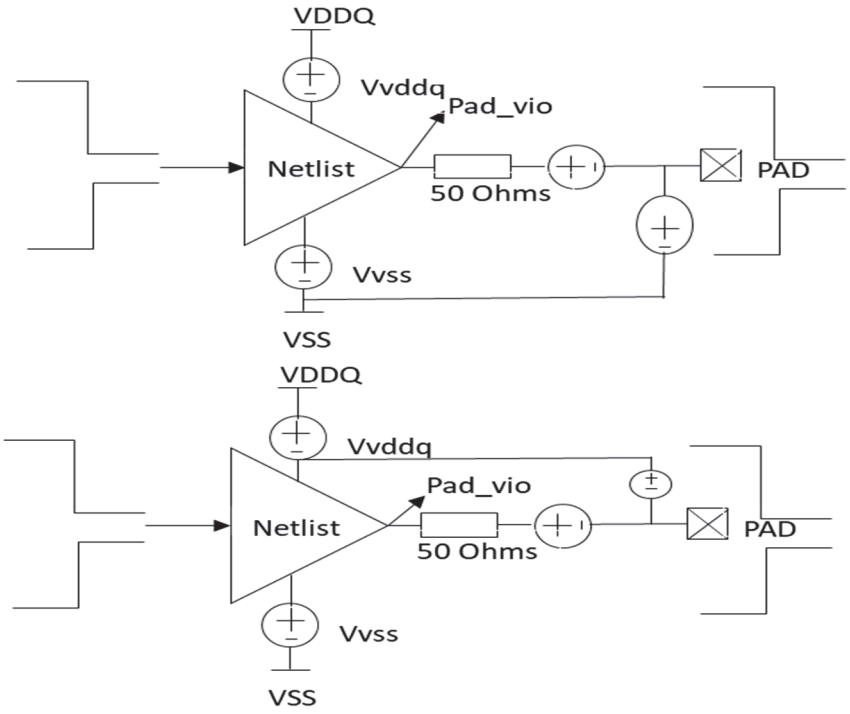


Fig. 2. Testbenches for _gnd and _sup Vt(It) simulations

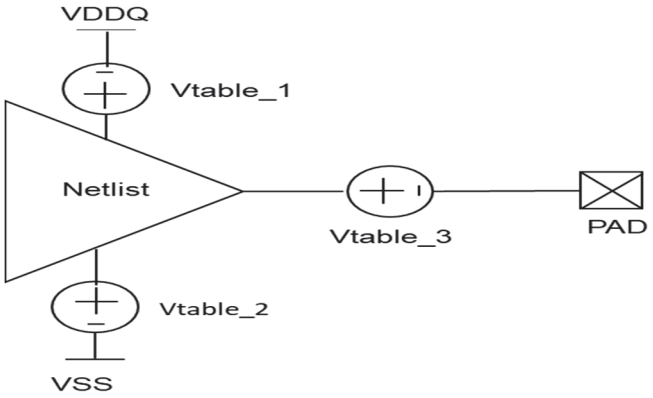


Fig. 3. Testbenches for Iv simulations

In case of the ISSO_PU simulation, the driver is in a high state, Vtable_2 and Vtable_3 have DC values and the Vtable_1 sweeps form –VDDQ to VDDQ. In case of ISSO_PD simulation the driver is in a low state, Vtable_1 and Vtable_3 have DC values and the Vtable_2 sweeps form –VDDQ to VDDQ. In case of pullup(pulldown) simulation the driver is in a high(low) state, Vtable_1 and Vtable_2 have DC values and the Vtable_1 sweeps form –VDDQ to 2*VDDQ.

The impedance mismatch impact on the output signal. To present the impedance mismatch impact on the output signal, two cases are considered: Case 1: 60 *Ohms* output impedance with 60 *Ohms* termination.

Case 2: 60 *Ohms* output impedance with 120 *Ohms* termination.

The testbenches to show the difference are shown in Fig. 4.

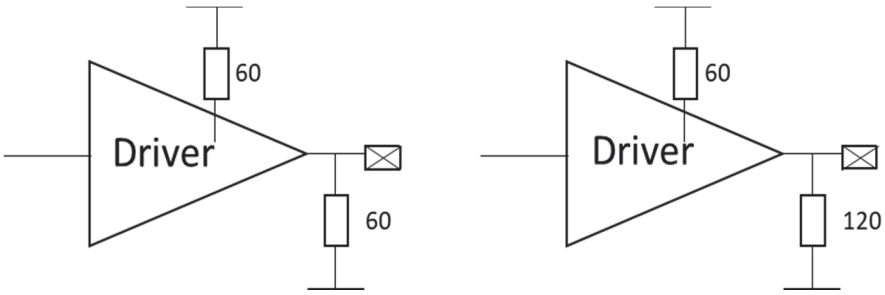
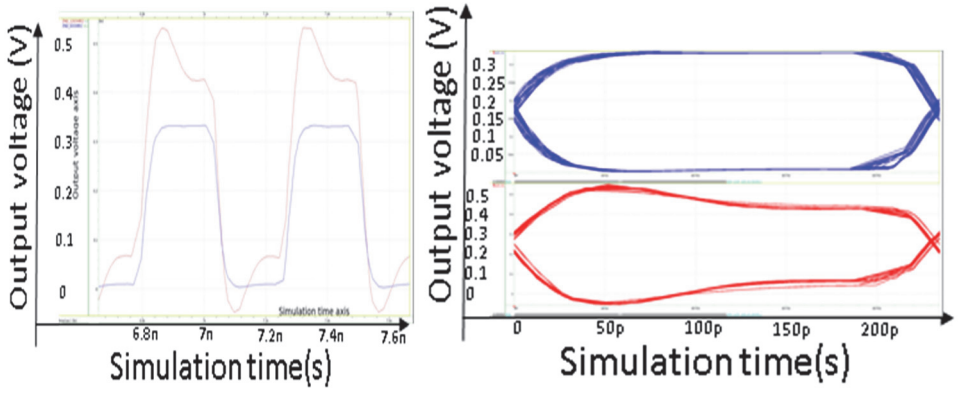


Fig. 4. Testbenches used for showing the impedance mismatch

In the first case, the output impedance of the driver is equal to the RTT impedance which represents the input resistance of RX, so there should be no signal return and noises. But due to impedance mismatch in the second testbench, there will be noise and signal return [2]. To see the difference, the same full swing input signal has been given to both inputs. To see the mismatch, the eye diagram and Vt waveforms should be looked at. The waveforms are shown in Fig. 5. The red waveform in Fig. 5 represents the case for the 60 *Ohms* RTT resistance and the blue one represents the case with the 120 *Ohms* RTT resistance. The results show that when we use equal resistances, we don't get any reflection on the output. But for the 120 *Ohms* case, there is reflection on the output signal, and the settling time becomes longer [3].



a) b)

Fig. 5. a) Vt waveforms for both cases b)EYE diagrams for both cases

The proposed solution and simulation results. Fig. 5 shows the importance of impedance mismatch. So, it is proposed to have an impedance correction approach that will give better impedance match. The approach is to add 2 current-controlled current sources to control the output impedance of the driver. The approach has been applied for the raw driver [4], but as the IBIS model has become the main way to represent and test the driver, we must have the same approach for IBIS models. The approach is to add the CCCS in the IBIS generating process to have our desired impedance value. The main difficulty is to find the correct ratio by which the output current will be controlled. An automation script which finds the correct ratio and puts the correct ratio values in the testbenches has been created. The CCCS values are controlled separately to have an ability to have 2 different values between pullup and pulldown impedances. The simplified model of the testbenches used in the IBIS generation is presented in Fig. 6. CCCS_PU is responsible for adjusting the PU resistance, whereas the CCCS_PD is responsible for PD resistance. In this paper, an ideal CCCS is being used. To control the CCCS we need to have a voltage source (VSOURCE) connected to the PAD to be able to calculate the current on the PAD. And after having the controlling current, which is the PAD current, the ratio of CCCS is adjusted. To be able not to turn on both CCCSs at the same time, the designer must put max=0 in the testbench, where the CCCS is called. Putting max=0 helps with that, because the current flowing towards PAD is always positive and the current coming from the PAD is negative.

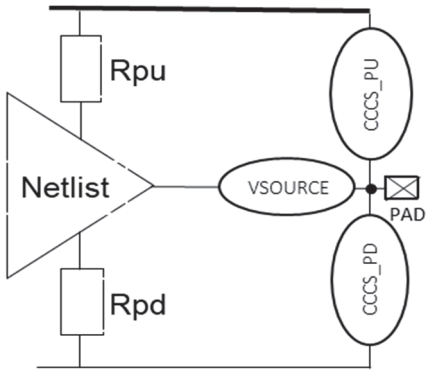


Fig. 6. A simplified model of the testbenches

3 IBIS models have been created. The first model is a standard model which has a 40 *Ohms* output impedance for all three PVT corners (TT FF SS) [5].

For the second model, it has been decided to have +10% impedance for the SS case and -10% impedance for the FF case using a calibration circuit. The third model should have the same impedance requirements as the second model, but it should use the proposed method [6]. The results are summarized in Table 1.

Table 1

Summary table

		IBIS		SPICE	
	PVT	Rpu (*Ohms*)	Rpd (*Ohms*)	Rpu (*Ohms*)	Rpd (*Ohms*)
First model	TT	59.123	59.324	59.11179	59.29795
	FF	59.637	59.6139	59.62123	59.60889
	SS	58.4066	57.4424	58.3967	57.45891
Second model	TT	59.123	59.324	59.11179	59.29795
	FF	53426	54.0123	53.42699	54.0101
	SS	66.5673	66.2606	66.52813	66.2663
Third model	TT	59.123	59,.324	59.11179	59.29795
	FF	54.0102	54,0076	54	54
	SS	66.0184	659972	66	66

Table 2 shows the difference between IBIS vs nominal, SPICE vs nominal and SPICE vs IBIS [7].

Table 2

Summary table

	PVT	IBIS DIFF		SPICE DIFF		IBIS vs SPICE Diff	
		Rpu DIFF *(%)*	Rpd DIFF (%)	Rpu DIFF (%)	Rpd DIFF (%)	Rpu DIFF (%)	Rpd DIFF (%)
First model	TT	1.46	1.12	1.48	1.17	0.0189	0.0439
	FF	0.605	0.64	0.631	0.651	0.026	0.008
	SS	2.655	4.26	2.672	4.235	0.016	0.028
Second model	TT	1.46	1.12	1.48	1.17	0.0189	0.0439
	FF	10.956	9.979	10.955	9.831	0.0018	0.004
	SS	10.945	10.434	10.88	10.443	0.0588	0.0086
Third model	TT	1.46	1.12	1.48	1.17	0.0189	0.0439
	FF	9.983	9.987	10	10	0.0188	0.014
	SS	10.03	9.99	10	10	0.0278	0.0042

IBIS DIFF column shows the difference between IBIS impedance and the nominal impedance which, in this paper, is 60 *Ohms*. The SPICE DIFF column shows the difference between SPICE impedance and the nominal impedance. The IBIS vs SPICE DIFF column shows the difference between SPICE and IBIS.

Conclusion. A new approach to correct the output impedance of the IBIS model has been proposed and designed using SAED 14 *nm* FinFet technology [8]

and with the usage of Galaxy Custom Designer tool [9]. The phenomena of impedance mismatch have been examined on the driver. The standard methods for impedance mismatch correction don't give good correlation between impedances. With the new approach, the designer can have the desired output impedance for the driver. The approach has been used in IBIS generation which gives an opportunity to have an IBIS model which can be used to test the newly corrected driver in top simulations and save crucial time and resources.

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National Polytechnic University of Armenia. The material is received on 25.01.2023.

Հ.Վ. ՎԱՐԴԱՆՅԱՆ

IBIS ՄՈԴԵԼԻ ԵԼՔԱՅԻՆ ԴԻՄԱԴՐՈՒԹՅԱՆ ՇՏԿՄԱՆ ՄՈՏԵՑՈՒՄ՝ ՀԿՀԱ-Ի ՕԳՏԱԳՈՐԾՄԱՄԲ

ԿՄՈԿ տեխնոլոգիաների չափերը, ագրեսիվորեն մասշտաբավորման և հաղորդչի ելքային դիմադրության փոքրացման պատճառով, պահանջում են ունենալ դիմադրությունների լավ համապատասխանեցում հաղորդիչ և ընդունիչ հանգույցների միջև: Դիմադրությունների տարբերությունը կարող է դառնալ աղմուկի և ազդանշանի վերադարձի պատճառ, որը չափազանց կփոքրացնի շղթայի արդյունավետությունը: Ներկայումս այդ տարբերությունները թեստավորվում են՝ օգտագործելով ՄԿԻՍ (մուտք/ելք կրկնիչի ինֆորմացիայի սպեցիֆիկացիա) մոդելներ, որի պատճառները գինը և թեստավորման արագությունն են:

Առաջարկվում է հոսանքով կառավարվող հոսանքի աղբյուրի (ՀԿՀԱ) օգտագործման մեթոդ, որը կնվազեցնի վերոհիշյալ անհամապատասխանությունը և այն կդարձնի 1%-ից պակաս: Առաջարկվող մեթոդը կարող է օգտագործվել յուրաքանչյուր տեսակի հաղորդիչ հանգույցների և ՄԿԻՍ մոդելների դեպքում:

Առանցքային բառեր. հաղորդիչ, ընդունիչ, դիմադրությունների անհամապատասխանություն, ՀԿՀԱ, ՄԿԻՍ:

А.В. ВАРДАНЯН

ПОДХОД К КОРРЕКЦИИ ВЫХОДНОГО ИМПЕДАНСА МОДЕЛИ СПЕЦИФИКАЦИИ ИНФОРМАЦИИ О БУФЕРЕ ВВОДА/ВЫВОДА С ИСПОЛЬЗОВАНИЕМ ИСТОЧНИКА ТОКА С РЕГУЛИРУЕМЫМ ТОКОМ

Поскольку размер КМОП технологии агрессивно уменьшается, а выходное сопротивление передатчика (ТХ) становится все меньше и меньше, возникает необходимость иметь хорошую корреляцию импеданса между ТХ и приемником (RX). Несоответствие между импедансами может вызвать шум и реакцию, которые резко снижают эффективность схемы. В настоящее время эти несоответствия проверяются с использованием моделей СИБВ (спецификация информации о буфере ввода/вывода) из-за низкой стоимости и скорости тестирования.

Предлагается метод использования источника тока с регулируемым током (ИТРТ), который позволяет уменьшить рассогласование и сделать его менее 1%. Предлагаемый метод может быть реализован для всех типов драйверов ТХ и моделей СИБВ.

Ключевые слова: передатчик, приемник, несоответствие импедансов, источник тока с регулируемым током, спецификация информации о буфере ввода/вывода.