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THE EYE OPENING IMPROVEMENT METHOD FOR A HIGH SPEED CURRENT MODE LOGIC DRIVER

A bandwidth improvement method of current mode logic (CML) drivers, of the integral circuit type specifically designed for high-speed serial data transmission systems is presented. These drivers are characterized by their ability to operate at high frequencies and their ability to provide a high level of signal integrity, which is critical for achieving high data rates and low error rates in high-speed systems. The key advantages of CML drivers such as providing a high level of signal integrity, the circuit topologies, operating modes, and performance characteristics are discussed. Furthermore, the challenges and limitations of CML drivers, as well as the recent advances in the field that enables the use of CML drivers in high-speed systems are also discussed. A driver constructed by the proposed method operating at 112 *Gbps* in PAM4 modulation consumes 9 *mW* under 0.9 *V* supply.

Keywords: SERDES, transmitter, current mode logic, signal integrity, receiver, modulation.

Introduction. The growth of industries such as AI and cloud computing has created a need for faster ways to connect integrated circuit chips. The data center, which houses many servers, can be thought of as the brain of AI and the technology that allows data to flow freely between servers within the data center can be thought of as its bloodstream. Currently, a technology called Serializer/Deserializer (SerDes) is commonly used for high-speed data transmission. It has several benefits over parallel interface, as it reduces the number of pins on a chip and uses equalization to counteract the signal loss at high frequencies. Due to these benefits, SerDes is now the primary solution for high-speed wireline data transmission.

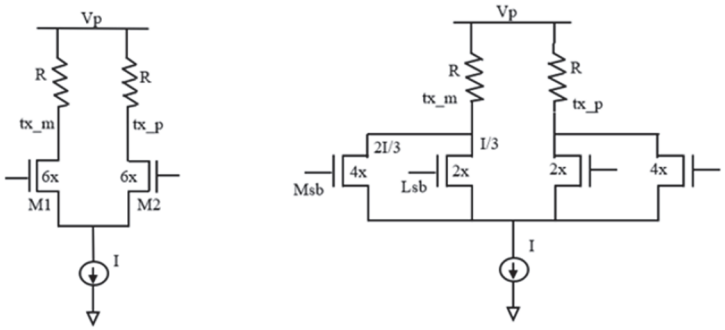
As the need for faster data transmission grows, designing a transmitter that can handle high-speed signals with minimal distortion and loss becomes a key technical challenge. This is because the transmitter consumes the most bandwidth and requires the highest clock frequency of any circuit. If the transmitter cannot transmit high-speed signals effectively, it will be difficult to recover the signal at the receiving end due to the channel loss and degradation. Therefore, designing a low-power and high-performing transmitter is an important aspect of the SerDes design.

The advancements in technology have allowed for improved high performance I/O circuitry, but the bandwidth of electrical channels used for communication

between chips has not kept pace. This highlights the importance of considering four-level pulse amplitude modulation (PAM4), which offers higher efficiency, less loss at high frequencies, and slower clock speeds compared to traditional binary signaling. This has led to PAM4 being implemented in various high-speed I/O standards. To support PAM4 modulation, recent developments in current-mode, voltage-mode and hybrid transmitters, as well as in analog-to-digital converter-based and mixed-signal receivers have been made [1]. However, PAM4 transceivers require more stringent circuit linearity, better equalizers for multi-level interference cancellation, and improved sensitivity compared to systems that use NRZ signaling.

On the transmitter side, using source-series-terminated (SST) voltage-mode drivers allows for the high output swing required for PAM4 modulation with high linearity achieved up to differential output swings equal to the nominal output stage supply. Advanced hybrid drivers that employ current boosting can further improve the output swing. Voltage mode drivers also offer reduced static power consumption relative to current-mode drivers, although at higher data rates this advantage becomes a smaller percentage of the total transmitter power consumption. This is due to large clocking power and the use of output-stage segmentation for equalization setting and impedance control. This segmentation can introduce on-chip interference and results in increased output stage area and power. Another important aspect of the transmitter is the final serializer, where efforts have been made to minimize power consumption in both current-mode and voltage-mode implementations. Additionally, equalization is often also necessary to improve the signal quality.

Current mode logic driver. Fig.1 (a) below shows the circuit of the basic circuit of the CML driver for the NRZ operation.



a) *b)*

Fig. 1. (a) a CML driver for NRZ operation, (b) a CML driver for PAM4 operation

Differential serial data is coming to input devices M1 and M2 accordingly. When input of the M1 transistor is logic 1 and for M2 logic zero the whole I current will flow through the left branch, and the voltage levels at the output will

be $Vp - IR$ for tx_m and vp for tx_p. The diifferential peak-to-peak voltage will be $t_{xp} - t_{xm} = IR - (Vp - IR) = 2IR$.

To allow PAM4 operation intermediate voltage levels should be introduced. For that tx_p should be reduced to some extent and tx_m must be increased by the same amount. To do so, ΔI current must be extracted from the left side and the same amount should be added to the right side. With this voltage level $(I - 2\Delta I)R$ will be obtained. If the ΔI current is subtracted from the right branch and added to the left branch $(-I + 2\Delta I)R$, the voltage level will be obtained. All 4 voltage levels are shown in Fig. 2.

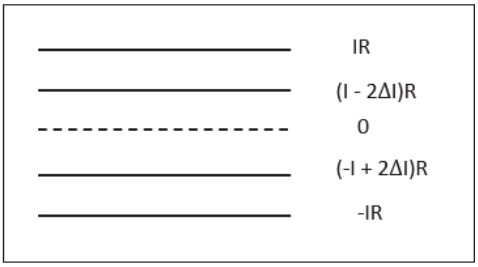


Fig. 2. The voltage level during the PAM4 operation

To perform current substruction approach in Fig.1 (b), can be used. Input transistors are split into 2 parts. Those 2 parts should be binary weighted. The 6x transistor is split to 4xMsb and 2xLsb. When both MSB and LSB are logic one or both are logic, 0 similar to NRZ voltage levels is achieved. Let's consider Msb = 1 and Lsb = 0 case. In this case 2I/3 current will flow through the MSB transistor and I/3 current will flow through the LSB transistor. For this scenario ΔI current from Fig. 2 is equal to I/3. Voltage levels for all possible MSB and LSB combinations are shown in Table.

Table

Voltage Levels

MSB	LSB	tx_m	tx_p	V_diff
1	1	$Vp - IR$	vp	IR
1	0	$Vp - (2/3) * IR$	$Vp - (1/3) * IR$	$IR/3$
0	1	$Vp - (1/3) * IR$	$Vp - (2/3) * IR$	$-IR/3$
0	0	vp	$vp - IR$	$-IR$

Problem description. In modern architectures final 4x1 serialization is performed using quarter rate clocks [2, 3]. The last 4-to-1 serializer plays a crucial role in a quarter-rate transmitter, as it should provide enough bandwidth to support the full-rate output.

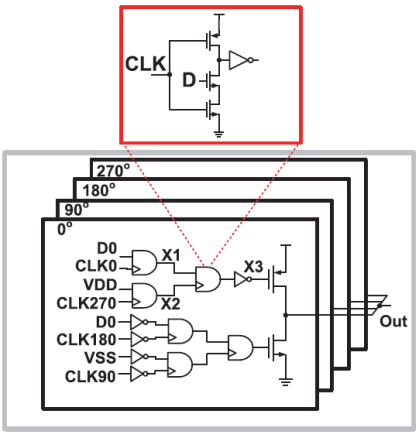


Fig. 3. The block diagram of the divider

However, it can be difficult to achieve this using conventional pass-gate serializers, which have reduced drive strength due to the effective stacking of transistors at the high self-loading output node. The dynamic NAND pre-drivers (Fig. 3) use the input data to qualify a pulse defined by adjacent quarter-rate clock edges, allowing the tri-state inverter-based mux to drive the full-rate output node through only one transistor, similar to a simple inverter, with the input data activating one of the PMOS/NMOS devices [1]. This approach is used for series source terminated voltage driver. As for the current driver, an example how 4x1 serialization and final summation is performed is shown in Fig. 4.

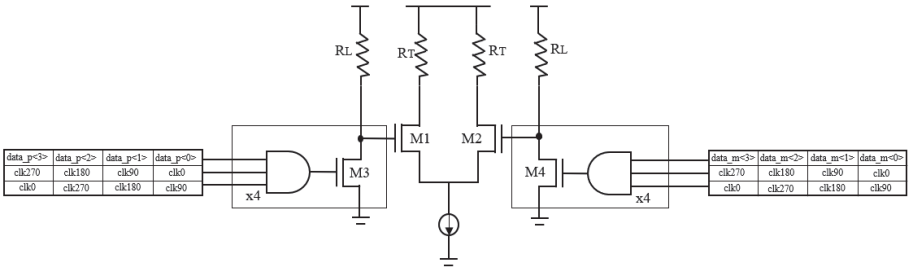


Fig. 4. Current mode driver with 4x1 mux

In the CML, driver current should be steered in the left and right branches to obtain corresponding voltage levels. To properly steer tail current there should be enough voltage swing in RL resistors. If the swing on RL resistors is small residual current will make differential swing voltage smaller. If swing across RL resistors is high, current source will be pinched off for a short period of time. This results in peaking of the output current. Because of the abovementioned issues, the bandwidth degrades over the process, voltage, temperature variations and vertical eye opening

become smaller. This has a direct negative impact on the Bit Error Rate (BER) of transmitter.

The proposed method. Because of the process voltage and temperature variation swing on RL resistors can vary. To compensate that variation, calibration method is proposed. A current mode logic driver with summing node calibration is shown in Fig. 5. An additional current source is introduced which steers the current in the secondary differential pair. The amount of this current can be controlled by a code. Also, 1bit resistance control is added.

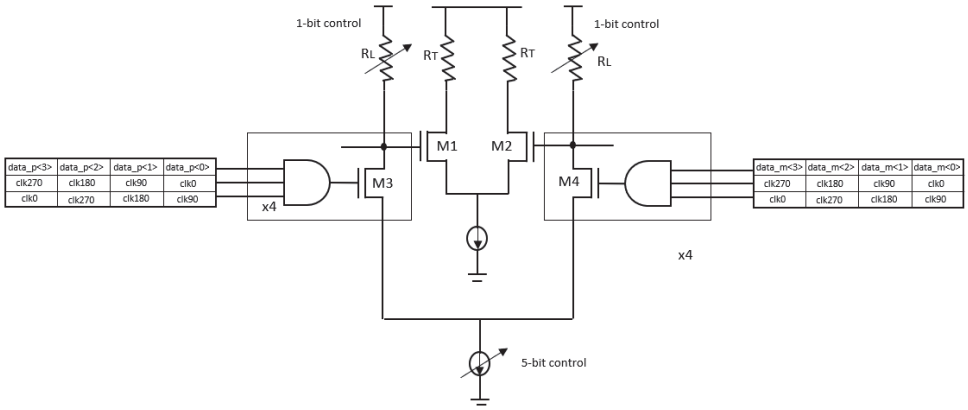


Fig. 5. Current mode driver with 4x1 mux

When calibration starts all data_p bits are logic 1 and data_m bits are logic 0. RL resistors have 1 bit control with load_sel parameter. When it is set to 1 a parallel resistor is connected to the RL resistor and its resistance becomes smaller. In the initial phase of calibration, this bit is set to 1. Curr_code parameter defines the code for the summing node current source. At the beginning, this code is at its middle value. After the initialization process tx_out_p net is compared with reference voltage which can be set by DAC. If tx_out_p is bigger than reference voltage defined by DAC, calibration is ended. There is a check is curr_code on its maximum available value. If no curr_code is changed, use the binary search algorithm. In case of maximum curr_code, load_sel parameter is checked and in case of the value 0, the calibration process ends. If the value is 1, it is set to 0 and the curr_code again is set to its middle code, and the calibration process starts by comparison of tx_out_p and dac_ref voltages.

The verification results of calibration algorithm for typical corner is shown in Fig. 6.

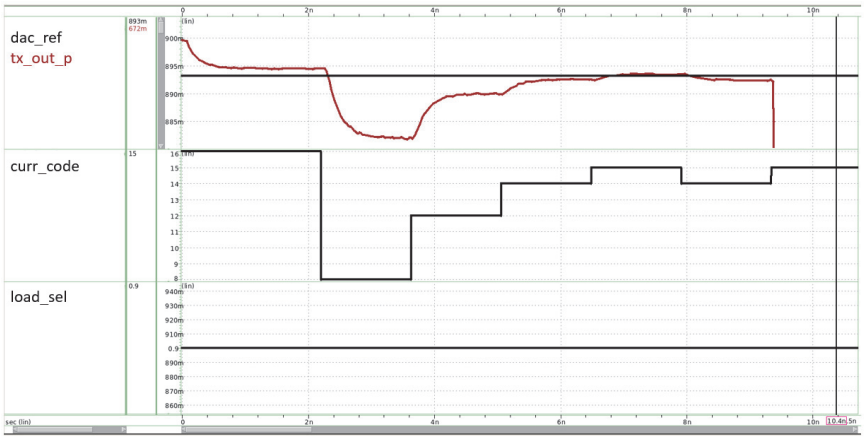


Fig. 6. Summing the node calibration process

Simulation Results. In Fig. 8, two eye diagrams are shown which are obtained via Hspice simulation [4]. The left one is captured using the circuit in Fig. 7 and the right one is captured with the version which includes the described method. As seen from the Figure, the right one has a bigger eye height compared with the left one. Vertical eye opening for the left one is 513 *mV*. For the right one, vertical opening is 635 *mV*. The opening is improved by 122 *mV*. Simulation was performed for the slow corner, low supply voltage using the SAED14 *nm* FinFet technology [5]. For this specific corner calibration code is 27 and load_sel is 0. That means that a parallel resistor is enabled and the overall resistance of RL is smaller. For typical corner code is 15 and load_sel is 1. After checking for multiple critical cases no corner was identified for which code range is not sufficient to cover required operation.

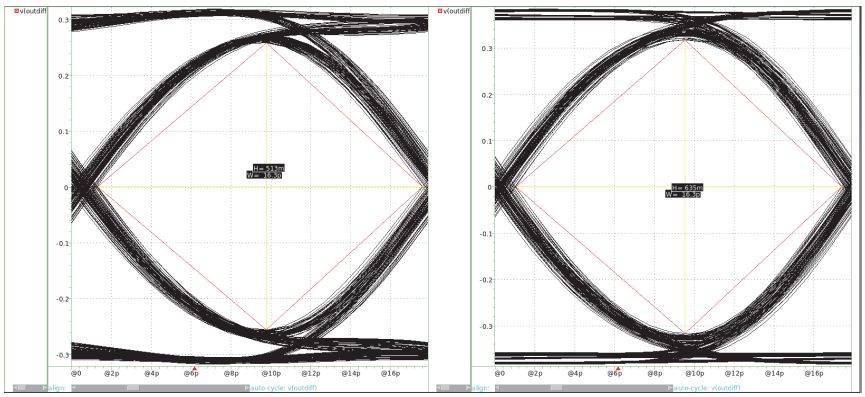


Fig. 7. Eye diagrams for transmitter NRZ mode7

Similar verification is performed for the PAM4 operation as well. Fig. 8 shows the difference of all 3 eye openings again for the slow corner with low

supply voltage. As seen from the Figure, the upper eye vertical opening increases by 28 *mV*, the middle eye opening increases by 33 *mV* and lower eye opening increases by 34 *mV*.

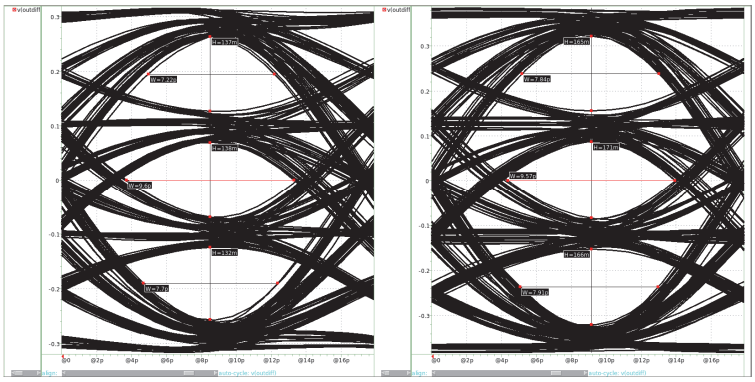


Fig. 8. Eye diagram for Transmitter PAM4 mode

Conclusion. The driver with the proposed method improves the eye vertical opening for NRZ and PAM4 operating modes. It can be used in modern SERDES drivers. For simulations, SAED 14 *nm* FinFet technology is used. By implementing this method, the current consumption for the driver unit decreases by ~100 *uA* without having a negative impact on the output eye opening. The area of the driver with the implemented method increases by 10.6%.

REFERENCES

1. **Sepehrian H., Alie S., Madeira P., and Tonietto D.** 106 Gb/s PAM-4 Transmitter With 2.1 Vppd Swing in 7nm FinFET Process // *2021 Symposium on VLSI Circuits*.- Kyoto, Japan, 2021.- P. 1-2, doi: 10.23919/VLSICircuits52068.2021.9492349.
2. **Roshan-Zamir A., Elhadidy O., Yang H. -W., and Palermo S.** A Reconfigurable 16/32 Gb/s Dual-Mode NRZ/PAM4 SerDes in 65-nm CMOS// IEEE Journal of Solid-State Circuits.- Sept. 2017.- Vol. 52, no. 9.-P. 2430-2447, doi: 10.1109/JSSC.2017.2705070.
3. **Song E., Yang J., Hong S., and Han J.** A 32-Gb/s High-Swing PAM-4 Current-Mode Driver with Current-Bleeding Cascode Technique and Capacitive-Coupled Pre-drivers in 40-nm CMOS for Short-Reach Wireline Communications// 2022 IEEE 65th International Midwest Symposium on Circuits and Systems (MWSCAS). - Fukuoka, Japan, 2022.-P. 1-4, doi: 10.1109/MWSCAS54063.2022.9859487.
4. Hspice Reference Manual, Synopsys Inc.- 2017. -846p.
5. **Melikyan V.**, **Martirosyan M.**, **Piliposyan G.** 14*nm* Educational Design Kit: Capabilities, Deployment and Future// Small Systems Simulation Symposium. - 2018. -P. 42-55.

National Politechnical University of Armenia. The material is received on 07.02.2023.

Հ.Տ. ԳՐԻԳՈՐՅԱՆ

ԱՉՔԻ ԲԱՑՎԱԾՔԻ ԼԱՎԱՑՄԱՆ ՄԵԹՈԴ ԱՐԱԳԱԳՈՐԾ ՀՈՍԱՆՔԻ ՌԵԺԻՄՈՎ ՏԱՆՈՂ ՀԱՆԳՈՒՅՑԻ ՀԱՄԱՐ

Դիտարկվում է հոսանքի ռեժիմով տանող հանգույցի (ՀՌՏՀ), որը ինտեգրալ սխեմայի տեսակ է, հատուկ նախագծված արագընթաց հաջորդական տվյալների փոխանցման համակարգերի համար թողունակության բարելավման մեթոդ: Տանող հանգույցները բնութագրվում են բարձր հաճախականություններով աշխատելու և ազդանշանի ամբողջական բարձր մակարդակ ապահովելու ունակությամբ, ինչը կարևոր է բարձր արագության համակարգերում տվյալների բարձր արագության և սխալի ցածր մակարդակի հասնելու համար: Քննարկվում են ՀՌՏՀ-ների հիմնական առավելությունները, ինչպիսիք են ազդանշանի ամբողջականության բարձր մակարդակի ապահովումը, սխեմայի տոպոլոգիաները, աշխատանքային ռեժիմները և կատարողական բնութագրերը: Վերլուծվում են նաև ՀՌՏՀ-ների նախագծման մարտահրավերներն ու սահմանափակումները, ինչպես նաև ոլորտի վերջին առաջընթացները, որոնք հնարավորություն են տալիս օգտագործել ՀՌՏՀ-ն բարձր արագությամբ համակարգերում: Առաջարկվող մեթոդով հաղորդիչը, որն աշխատում է 112 *Գբիթ/վ* արագությամբ ՊԱՄ4 մոդուլյացիայի դեպքում, սպառում է 9 *մՎտ* 0,9 *Վ* լարման տակ:

Առանցքային բառեր. SERDES, հաղորդիչ հանգույց, հոսանքի ռեժիմի տրամաբանություն, ազդանշանի ամբողջականություն, ընդունիչ հանգույց, մոդուլյացիա:

А.Т. ГРИГОРЯН

МЕТОД УЛУЧШЕНИЯ ОТКРЫТИЯ ГЛАЗКОВОЙ ДИАГРАММЫ ДЛЯ ВЫСОКОСКОРОСТНОГО ДРАЙВЕРА С ЛОГИКОЙ ТОКА

Представлен метод улучшения пропускной способности драйверов с логикой тока (ДЛТ) типа интегральной схемы, специально разработанной для высокоскоростных систем последовательной передачи данных. Эти драйверы характеризуются способностью работать на высоких частотах и обеспечивать высокий уровень целостности сигнала, что имеет решающее значение для достижения высоких скоростей передачи данных и низкого уровня ошибок в высокоскоростных системах. Обсуждаются ключевые преимущества драйверов ДЛТ, такие как обеспечение высокого уровня целостности сигнала, топология схемы, режимы работы и рабочие характеристики. Кроме того, рассматриваются проблемы и ограничения драйверов ДЛТ, а также последние достижения в области, которые позволяют использовать драйверы ДЛТ в высокоскоростных системах. Построенный предложенным методом передатчик, работающий на скорости 112 *Гбит/с* в модуляции ПАМ4, потребляет 9 *мВт* при напряжении питания 0,9 *В*.

Ключевые слова: SERDES, узел передатчика, логика тока, целостность сигнала, узел приемника, модуляция.