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A NOVEL AGING MONITORING CIRCUIT

Year by year there are numerous new requirements set to the lifetime and reliability of integrated circuits (IC), particularly in medical spheres and automotive applications. Consistent with technology downscaling the device reliability issues are increasing, but the quality requirements become stronger. Nowadays the aging phenomenon is one of the critical issues in systems with longer lifetime. Therefore, the monitoring of aging and its consequence compensation have become one of the key parts for today's ICs.

A novel aging monitoring circuit is proposed in this paper. This new monitoring circuit monitors the aging degradation during lifetime of the IC and generates a binary code. This code is applied to the inputs of compensation circuits, which compensates the degradation in the critical blocks throughout their lifetime. Monitoring circuit is realized with a 14 *nm* technology node and simulations proved the results' validity.

Keywords: integrated circuit, aging, monitoring, binary code, compensation.

Introduction. Aggressive down-scaling to lower technology nodes is driven by the thrust for high performance and device density. However, this is accompanied by deterioration of reliability, an increase in the design period, additional input-output pins in case of inserting stabilizing (adjusting) elements, an increase in the surface occupied by them, a larger power consumption current, and some other negative consequences. In the general case, not taking into account the above-mentioned factors lead to a decrease in the yield percentage of ICs, and therefore, in profits [1]. One of the most important factors in the deterioration of the reliability and uninterrupted operation of ICs is the phenomenon of aging, which can cause the entire system to fail over time [2]. The main types of aging are discussed below.

Bias temperature instability (BTI) is an aging phenomenon which leads to threshold voltage variations during the lifetime in the presence of voltage stress at the gate of the transistor, causing the circuit to fail its specifications. A PMOS transistor experiences negative BTI stress when its gate is applied logic 0. The increase in the threshold voltage is partially reversed when the voltage stress is removed (i.e., a logic 1 is applied). A similar phenomenon of positive BTI affects the threshold voltage of NMOS devices when they are stressed and the degradation relaxes with the removal of stress [3,4].

Hot carrier injection (HCI) is caused by the acceleration of carriers (electrons/holes) under lateral electric fields in the channel, to the point where they gain sufficient energy to cause damage, degrading mobilities and threshold voltages [3,4].

Time-dependent dielectric breakdown (TDDB) in gate oxides is an irreversible reliability phenomenon that at the point of breakdown causes an unexpected increase in the conductance of the gate oxide, which causes the current through the gate insulator to increase significantly [5].

In order to neutralize the negative effects of technological deviations, the characteristics of the modern IC blocks are adjusted during the testing or operating stages by means of the programmable input pins. Nevertheless, the addition of each input-output pins is associated with high costs [6]. Alternatively, one can employ circuits to monitor and compensate deviations in ICs and to solve the above mentioned problems [7].

Aging degradation can lead to various accidents in automotive systems, as well as to the reduction of the life span of the ICs installed in human bodies for medical purposes, as a result of which there will be a need for their frequent replacement, which is costly. Therefore, it is important to monitor the aging degradation during the lifetime of ICs and compensate for its consequences when necessary.

The proposed circuit. First, the aging effect is studied on SAED14nm FinFET PMOS based current source (Fig.1) [8]. This current source is used for the purpose of sensing the degradation due to the transistor aging. The source of the PMOS device has been connected to VDD and drain to GND. To the gate was applied bias voltage equal to 0 *V*, to have maximum V_{GS}, and HSPICE simulation has been performed [9]. The current flowing from the drain to source was measured to be equal to 140 *uA*.

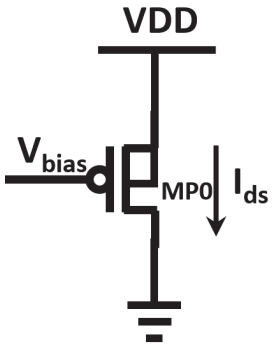

Fig. 1. The designed PMOS device

Aging HSPICE simulation was performed for 10 years. The result shows that I_{ds} has decreased and in 10 years it is equal to 110 *uA*. So, due to aging I_{ds} decreases by 30 *uA*, which is quite a large degradation. Aging HSPICE simulations are performed also up to 10 years with 1-year steps to understand how the I_{ds} changes over the years (Fig. 2).

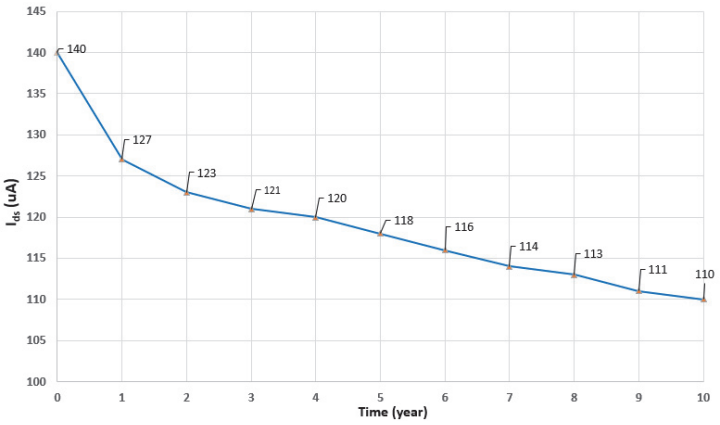

Fig. 2. I_{ds} dependency on years

The largest decrease occurs during the first year, which further emphasizes the need to design an aging monitoring circuit in order to detect the aging degradation and to feedback to the compensation circuits in order to compensate the aging degradation in the critical blocks starting from the first year.

A method developed and based on that circuit has been designed (Fig. 3) for monitoring the aging, which will detect the aging degradation, and depending on that, will generate an appropriate binary code based on the binary search algorithm [10], which can subsequently be used in the aging compensation circuits [11].

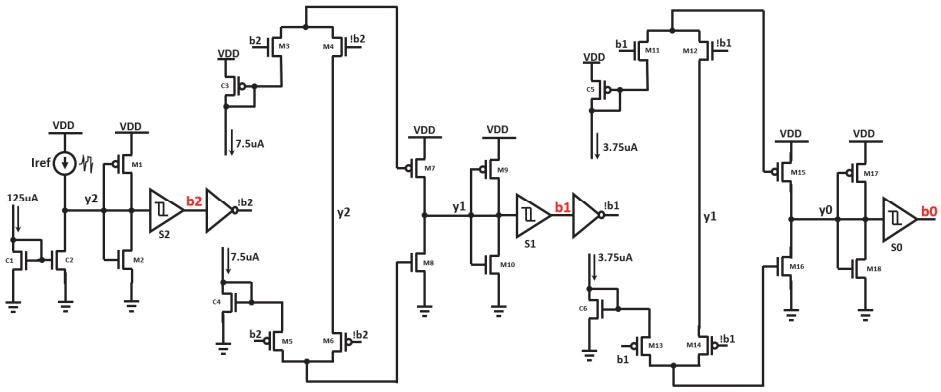

Fig. 3. The aging monitoring circuit designed by ideal current PWL source

In order to check the accuracy of the method and to show the basic principle of operation, firstly the circuit was designed with an ideal current PWL source. The scheme consists of 3 cascades. In the first cascade, an ideal current PWL source with the current reducing from 140 *uA* to 110 *uA* is used. A current mirror is connected in series, which passes 125 *uA* current, which is the half of 140 *uA* and 110 *uA*. The next stage consists of diode-connected M1 (PMOS) and M2 (NMOS) transistors. It is designed in such a way, that when the current flowing through them is the same, the potential of the y2 is equal to VDD/2. This stage serves as a current subtractor. The y2 is also applied to the S2 Schmitt trigger's input (Fig. 4) [12]. The designed Schmitt trigger's threshold voltage is VDD/2, and the Schmitt trigger employs a positive feedback loop which adds the hysteresis and provides a noise margin. The b2 output of the S2 Schmitt trigger is the first bit of the generated digital code. The b2 is inversed to control second cascade. When the Iref is greater than 125 *uA*, the difference between these currents flows through the NMOS transistor, which pulls y2 down, and the output of the S2 Schmitt trigger goes to 0. And when Iref is less than 125 *uA*, the difference between these currents flows through the PMOS transistor, which pulls y2 up, and the output of the S2 Schmitt trigger goes to 1. Thus the first bit of the signal is obtained.

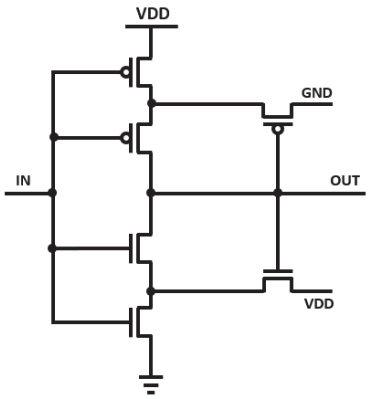

Fig. 4. The designed Schmitt trigger

At the first stage of the second cascade, diode-connected C3 and C4 transistors are passing the 7.5 *uA* current, which is the half of the maximum difference of the first cascade (15 *uA*). Devices M3, M4, M5 and M6 serve as switches. When b2 is 0, M3 and M6 are closed, and devices M4 and M5 are open. Since M5 is open, through M8 passes a 7.5 *uA* current, and M7 connects to y2, so the current flowing through it is equal to the difference between Iref and 125 *uA*. If it is higher than 7.5 *uA,* the difference will flow through the M10 device, which pulls y1 down, and the output of the S1 Schmitt trigger goes to 0. And if it is lower than 7.5 *uA*, the

difference will flow through the M9 device, which pulls y1 up, and the output of the S1 Schmitt trigger goes to 1. The output of the S1 Schmitt trigger (b1) is the second bit of the generated digital code. The b1 is inversed in order to control the third cascade.

The third cascade looks completely the same as the second one, but with the current values equal to 3.75 *uA*, which is the half of maximum difference in the second cascade (7.5 *uA*), also there is no need for inversion. At the output of the third cascade the signal b0 is generated, which is the third bit of the digital code.

To better understand the principle of circuit operation, an example for illustration is considered next. Assume Iref is equal to 135 *uA*. In that case the difference between Iref and 125 *uA* is 10 *uA* that will flow through M2 device, and b2 goes 0. The M5 device opens and through M8 flows the 7.5 *uA* current, at the same time, the M4 also opens and the current difference from the first cascade flows through the M7, namely 10 *uA*. The difference between them (2.5 *uA*) flows through the M10 device, and b1 goes to 0. The M13 device opens and through M16 flows the 3.75 *uA* current, at the same time the M12 also opens and through M15 flows the current difference from the second cascade, namely 2.5 *uA*. The difference between them (1.25 *uA*) flows through the M17 device, and b0 goes to 1. Concluding, in this case, the code is 001.

The next example covers the case when Iref is lower than 125 *uA*. Assume Iref is equal to 115 *uA*. In this case the difference between Iref and 125 *uA* is -10 *uA*, which flows through the M1 device, and b2 goes to 1. The M3 device opens and through M7 flows the 7.5 *uA* current, at the same time, the M6 also opens and through M8 flows the current difference from the first cascade, namely 10 *uA*. The difference between them (-2.5 *uA*) flows through the M9 device, and b1 goes to 1. The M11 device opens and through M15 flows the 3.75 *uA* current, at the same time, the M14 also opens and through M16 flows the current difference from the second cascade, namely 2.5 *uA*. The difference between them (1.25 *uA*) flows through the M18 device, and b0 goes to 0. Hence, in this case, the code is 110.

The simulation results. In order to make sure that the circuit works properly, the HSPICE simulation for the designed circuit was performed. The current value (Iref) of ideal current PWL source changes from 140 *uA* to 110 *uA* (Fig. 5).

Fig. 5. Outputs of circuit depending on the current change

The circuit generates an appropriate 3-bit digital code for each range of current variation (Table).

Table

Generated 3-bit digital code for each range of current variation

ΔIref (uA)	Digital code
0 – 3.75	000
3.75 – 7.5	001
7.5 – 11.25	010
11.25 – 15	011
15 – 18.75	100
18.75 – 22.5	101
22.5 – 26.25	110
26.25 – 30	111

Now that the principle of the circuit operation is clear, next ideal current PWL source is replaced by a biased PMOS transistor working as a current source (Fig. 6).

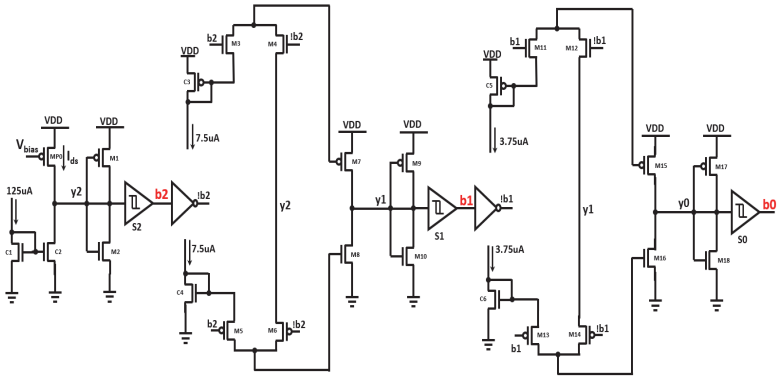

Fig. 6. Schematic view of the proposed novel aging monitoring circuit

For this circuit, aging HSPICE simulations were performed up to 10 years with 1-year steps (Fig. 7).

Fig. 7. Outputs of the designed aging monitoring circuit over the years

The simulations show that the proposed aging monitoring circuit performs as expected by generating a digital code corresponding to the current reduction due to aging degradation over years.

Conclusion. A novel aging monitoring circuit has been proposed and implemented using the SAED 14 *nm* FinFET technology with the help of Custom Compiler tool [13]. The circuit is easily implemented with CMOS technology, using only MOS transistors. Simulations show that the circuit detects the aging degradation by generating a digital code, which can be converted to other types of codes and can be applied to the compensating circuits wherever needed. Due to its simple structure the proposed aging monitoring circuit does not require additional input-output pins on the chip for its operation. Additional testing operations are not needed, either. This leads to the reduction of area, testing time and cost of IC's. Additionally, if more accuracy is needed, the number of digital bits can be increased adding more cascades with the same principle.

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ԾԵՐԱՑՄԱՆ ԵՐԵՎՈՒՅԹՆԵՐԸ ՄՇՏԱԴԻՏԱՐԿՈՂ ՆՈՐ ՍԽԵՄԱ

Տարեցտարի բազմաթիվ նոր պահանջներ են առաջանում ինտեգրալ սխեմաների (ԻՍ) ծառայության ժամկետի և հուսալիության վերաբերյալ, հատկապես բժշկական ոլորտներում և ավտոմոբիլային կիրառություններում: Տեխնոլոգիաների մասշտաբավորման հետ կապված՝ սարքի հուսալիության խնդիրները մեծանում են, բայց որակի պահանջներն ավելի խիստ են դառնում: Մեր օրերում ծերացման երևույթները դառնում են ավելի երկար կյանք ունեցող համակարգերի կարևորագույն խնդիրներից մեկը: Հետևաբար, ծերացման երևույթների մշտադիտարկումը և անհրաժեշտության դեպքում դրա հետևանքների փոխհատուցումը դառնում են այսօրվա ԻՍ-երի առանցքային խնդիրներից մեկը:

Առաջարկվում է ծերացման երևույթները մշտադիտարկող նոր սխեմա: Առաջարկվող սխեման կարող է գրանցել ծերացման երևույթների ազդեցությունը ԻՍ-երի կյանքի ընթացում և գեներացնել երկուական կոդ: Այդ կոդը կարող է փոխանցվել փոխհատուցման սխեմաներին, որոնք կարող են փոխհատուցել անհրաժեշտ բլոկների պարամետրերի վատթարացումը ողջ կյանքի ընթացքում: Մշտադիտարկող սխեման իրականացվել է 14 *նմ* տեխնոլոգիական գործընթացի համար, և արդյունքների վավերականությունն ապացուցվել է հոդվածում ներկայացված մոդելավորումների միջոցով:

Առանցքային բառեր. ինտեգրալ սխեմա, ծերացում, մշտադիտարկում, երկուական կոդ, փոխհատուցում:

С.А. ГУКАСЯН

НОВАЯ СХЕМА МОНИТОРИНГА ЯВЛЕНИЯ СТАРЕНИЯ

С каждым годом предъявляется множество новых требований, касающихся срока службы и надежности интегральных схем (ИС), особенно в области медицины и автомобилестроения. В связи с уменьшением масштаба технологий увеличиваются проблемы, связанные с надежностью устройства, но требования к качеству становятся все более жесткими. В настоящее время явление старения является одной из критических проблем в системах с более длительным сроком службы. Поэтому мониторинг старения и, при необходимости, компенсация его последствий становятся одной из ключевых частей современных ИС.

В статье предлагается новая схема мониторинга старения, которая может отслеживать деградацию из-за старения в течение срока службы ИС и генерировать двоичный код. Этот код может применяться ко входам компенсационных схем, которые компенсируют деградацию в необходимых блоках на протяжении всего срока службы. Схема мониторинга была реализована с помощью технологического процесса 14 *нм*. Доказана достоверность результатов моделирования, проведенного в статье.

Ключевые слова: интегральная схема, старение, мониторинг, двоичный код, компенсация.