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BUILT-IN SELF-TEST AND SELF-CORRECTION METHOD FOR MIXED-SIGNAL INTEGRATED CIRCUITS

In modern integrated circuits the number of devices have strongly increased. As a result, identifying the issues which have an impact on their performance stands out as a very complicated and challenging problem. In digital integrated circuits there are methods which are known, as well as some others which are in the active development stages targeted to enable the built-in self-tests, identify, and report those issues. At that, for mixed signal circuits, where the calculations or functions are performed based on the voltage levels, it is much complicated to develop self-testing mechanisms. A novel method of identifying the lack of clock signal and its duty cycle variation is proposed in this paper. The developed architectures and solutions are capable of detecting the lack of the clock signals, as well as informing the digital parts of the systems about the requirement for the coarse or fine tunings of the clock generation systems outside their autocalibration and loops.

Keywords: built-in self-test, integrated circuits, duty cycle distortion.

Introduction. All modern synchronous integrated circuits' (IC) signal propagation, transfer and receive through the high-speed links is being organized by the CMOS or CML level synchro-signals. Therefore, the quality of the transceiver signals, serialization and deserialization, the data-to-clock alignment, the clock-to-data recovery and other high-speed operations require high-quality clock signals [1,2]. The main contributor of potential failures is the duty cycle distortion of those signals, that is why a lot of studies are being carried out to detect and fix the duty cycle distortions. But those solutions are mainly oriented to improve the duty cycle and get close to 50% value. These improve the system noise immunity, the jitter and skew of the data signals [3]. But these are not covering the scenarios of the autocalibration algorithms getting stuck and the system stops to calibrate the duty cycle value. In such cases, the parallel calibration mechanism should be enabled and it should force the clock generation circuit to correct the duty cycle value so as to get closer to the 50% target. This is assumed to be a self-test and self-correction mechanism inside the mixed signal ICs.

The problem description and the proposed solution. The main problem in solving to which this research is targeted is the automatic duty cycle calculation and correction. An example of good quality data eye diagram vs the one generated with 10% duty cycle distorted clock are presented below (Fig.1).

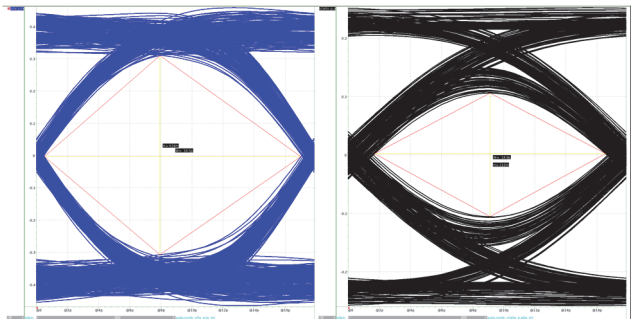

Fig.1. The impact of the clock duty cycle distortion on the eye opening

As it is seen from the results obtained above, the 10% duty cycle distortion results in around 3 times eye vertical opening reduction and 15% horizontal opening distortion. Such the majority of the defined problem stands justified.

To solve the problem the new method of clock signal duty distortion correction has been developed which is based on the 2 main parts: the first part is responsible to detect the existence of the clock at all since there may be scenarios that the clock generation circuits may got stuck and as a result no clock will exist. The second part is responsible for the duty cycle calculation and correction.

The first section of the proposed method is based on the high-speed slicer which is toggling with a rise of clock signal. The schematic implementation of the idea is presented below (Fig.2) where the output of the slicer remains constant 1 if there is no clock signal such that detects the failures inside the high-speed clock generation circuits such as phase-locked-loops (PLL), delay-locked-loops (DLL), injected loop oscillators (ILO) etc [4]. Its output starts to toggle when the clock generation circuit is functionally starting up. To avoid scenarios when the clock generator is locked at the low frequency values or toggling at unexpected frequencies, the high-pass filter is put at the input to reject those components. The R1 and R2 resistor values, as well as the C capacitor value is being calculated based on the high-pass frequency minimum value, i.e. if the expected frequency is 10 *GHz*, the -3 dB point of the C-R network should be at around to 8 *GHz* point. The next stage of the clock detector is CML2CMOS block whose role is to convert the CML domain signal to CMOS levels. The static offset between the inputs of the block is applied by the R1/R2 ratio so as to create hysteresis and toggle the outputs only if the voltage level will be higher than that value. This keeps the positive

output of the block in a static 1 state and the negative output to static 0 state when there is no clock. For further clock recovery or spike rejection, the slicer is put afterwards whose both outputs will be in static 1 state, the clock signal will not present. The final stage of the system is the XOR cell whose output will be in logic 1 state if the clock will present or 0 if it will not. So the clock detector will flag the presence of that signal.

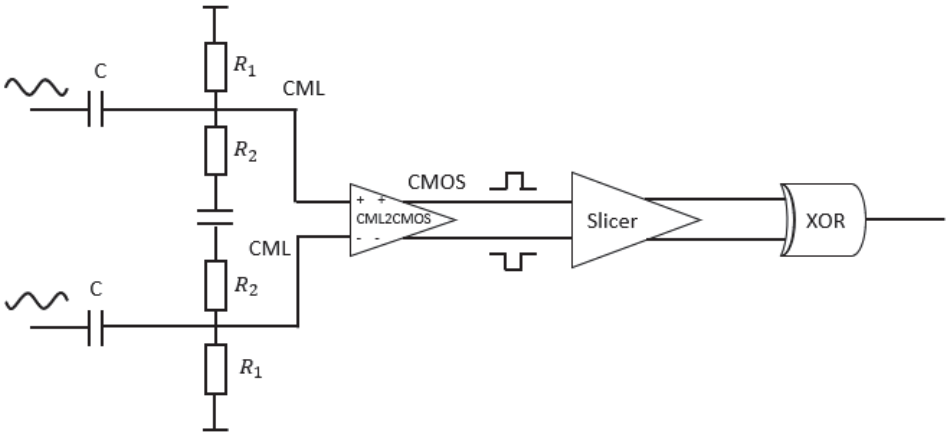

Fig.2. Clock detection implementation

The next part of the paper developed to be responsible for the clock duty cycle distortion is presented below (Fig. 3). It consists of the input multiplexor which selects the clock signal which will propagate to the duty cycle calculation block, the integrator circuit based on the R1-C1 rectifier, the digital-to-analog (DAC) block which converts the digital N-bit binary code to an analog voltage, the C2-R2-C3 low-pass filter which rejects the DAC output noise, as well as the noise coming from the comparator internal switching nodes, the comparator which compares the filtered clk_filt voltage to the Vdac DAC output voltage value.

During the logic 1 state of the s_clk select clock signal the clk_p is applied to the R1-C1 integrator input and the voltage of the clk_filt node gets $V_{clk\_filt} = = Vdd/Duty\_cycle$ value. DAC starts to increase the input binary code until the comparator switches from logic 0 to 1. Such transition means that the system finds the code of the DAC input corresponding to the duty cycle of the clock. During the logic 0 state of s_clk select clock signal the operation is being repeated for the clk_m inverse signal of the clk_p.

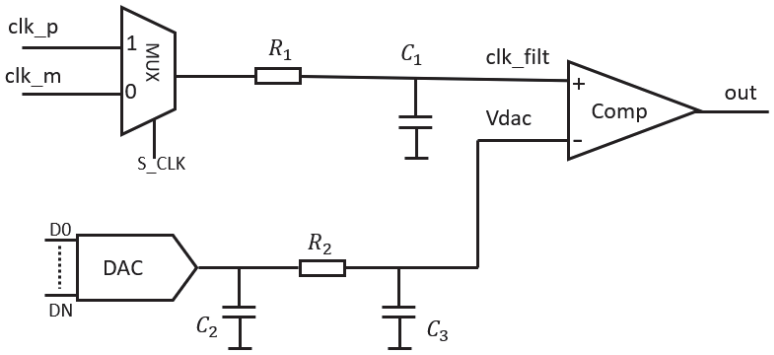

Fig.3. Duty-cycle distortion detection circuit

Results. DAC last significant bit (LSB) value is equal to $LSB = VDD/2^N$, where VDD is the supply voltage value, and N is the resolution of the DAC. 1% of duty cycle distortion is equal to VDD/100. Considering the abovementioned, for 10-bit DAC and 1V VDD value 1 LSB will be equal to around 1 mV and 1% duty cycle distortion will be equal to 10 mV. So, the accuracy of the system designed with 10-bit resolution DAC will be 0.1% duty cycle distortion and it is capable of generating a very accurate report about the actual clock quality. For high-speed systems up to ±2.5% duty cycle distortion value may still be acceptable, so the 8-bit minimum resolution of the DAC may be acceptable (Table).

Table

Summary of the results

Parameter Name	Expected Results	
	Min	Max
DAC resolution (*bit*)	8	-
Duty cycle distortion detection (*%*)	-2.5	2.5
Clock frequency (*GHz*)	1	14
Power consumption (*mW*)	-	3

Conclusion. A novel method and a schematic realization of built-in self-test mechanism for mixed-signal ICs is proposed in this paper. The first proposed solution is aimed at asynchronously detecting the proper generation of the clock signal required for high-speed operations and data transmission. The second solution is targeted to realize self-test and self-report of the clock duty cycle information. This may make the complex designs to easily detect and force the autocalibration mechanism to do coarse and fine tunings of the settings of the clock generation systems such as PLLs, DLLs, ILOs.

REFERENCES

1. **Lee Y., Choi Y., Kim C.** 24-Gb/s Input-Data-Independent Clock and Data Recovery Utilizing Bit-Efficient Braid Clock Signaling with Fixed Embedded Transition for 8K-UHD Intrapanel Interface // IEEE Solid-State Circuits Letters. – Canada, 2019. - P. 21-24.
2. **Li M., Lu Y., Yang Y.** PLL-Based Clock and Data Recovery for SSC Embedded Clock Systems // 2019 International SoC Design Conference (ISOCC). - Jeju, Korea (South), 2019. – P. 309-310.
3. **Clark K., Liu Z.** Modeling the Performance of the Clock Phase Caching Approach to Clock and Data Recovery // Journal of Lightwave Technology.– Italy, 2022.- P. 1681-1689.
4. **Rim A., Intisssar T., Mohamedr M.** Fault coverage analysis of selection circuit based BIST for RF CP-PLL // 2016 13th International Multi-Conference on Systems, Signals & Devices (SSD). - Leipzig, Germany, 2016. - P. 552-557.

National Polytechnical University of Armenia. The material is received on 29.03.2023.

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ԽԱՌԸ ԱԶԴԱՆՇԱՆԱՅԻՆ ԻՆՏԵԳՐԱԼ ՍԽԵՄԱՆԵՐԻ ՀԱՄԱՐ ՆԵՐԴՐՎԱԾ ԻՆՔՆԱԹԵՍՏԱՎՈՐՄԱՆ ԵՎ ԻՆՔՆԱԿԱՐԳԱԲԵՐՄԱՆ ՄԵԹՈԴ

Ժամանակակից ինտեգրալ սխեմաներում տարրերի քանակը էականորեն մեծացել է: Ուստի դրանց վարքագծի վրա բացասաբար անդրադարձող խնդիրների հայտնաբերումը դարձել է բարդ մարտահրավեր: Թվային ինտեգրալ սխեմաներում գոյություն ունեն ինչպես հայտնի, այնպես էլ ակտիվ մշակման փուլում գտնվող լուծումներ, որոնք միտված են ինքնաթեստավորման միջոցով հայտնաբերելու և գրանցելու այդ խնդիրները: Մինչդեռ խառը ազդանշանային սխեմաներում, որտեղ որպես հաշվարկների հիմք ծառայում են ազդանշանների լարման արժեքները, ինքնաթեստավորման մեթոդների ներդրումը հանդիսանում է առավել բարդ խնդիր: Աշխատանքի շրջանակներում առաջարկվել է սինքրոազդանշանի բացակայության և լցման գործակցի տատանման հայտնաբերման մեթոդ: Մշակված ճարտարապետությունները և լուծումները ունակ են հայտնաբերելու սինքրոազդանշանի բացակայությունը և համակարգերի թվային հանգույցներին տեղեկացնելու այդ ազդանշանների՝ համակարգերի ինքնակարգաբերման մեխանիզմներից անկախ կոպիտ և ճշգրիտ կարգաբերման անհրաժեշտության մասին:

Առանցքային բառեր. ներդրված ինքնաթեստավորում, ինտեգրալ սխեմա, լցման գործակցի աղավաղում:

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ВСТРОЕННЫЙ МЕТОД САМОПРОВЕРКИ И САМОКОРРЕКЦИИ ДЛЯ ИНТЕГРАЛЬНЫХ СХЕМ СМЕШАННЫХ СИГНАЛОВ

В современных интегральных схемах (ИС) число элементов существенно увеличилось, в результате чего решение проблем, влияющих на их эффективность, представляет собой сложную задачу. В цифровых ИС имеются как известные методы, так и методы, находящиеся в активной стадии разработки, которые предназначены для включения встроенного самотестирования, выявления и сообщения об этих проблемах. При этом в смешанных сигнальных схемах, где в основе расчетов выступают значения напряжения сигналов, внедрение методов самотестирования намного сложнее. В статье предлагается новый метод определения отсутствия тактового сигнала и изменения его коэффициента заполнения. Разработанные архитектуры и решения способны обнаруживать отсутствие тактовых сигналов, а также информировать цифровые части систем о необходимости грубой или точной настройки систем генерации тактовых импульсов вне их контуров автокалибровки.

Ключевые слова: встроенная самопроверка, интегральная схема, искажение коэффициента заполнения.