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THE OUTPUT NOISE REDUCTION OF A LOW-TO-HIGH SUPPLY VOLTAGE LEVEL-SHIFTER

A new approach for reducing output noises in the level-shifter is presented. The level-shifters which are intended for making the high-voltage amplitude signal from low-voltage amplitude signal, has a big issue related to the output noises. The noises that come from parasitic capacitances and other sources become much higher in the output as the circuit increases the amplitude of the input signal in the output, so it also increases the noises. These level-shifters also have the delay time issue. The delay time range between the input signal and output signal is not so low. Using the capacitances in the output for reducing the noises can increase the delay time range, which is not a good feature for the circuit. The new method reduces the output noises without increasing the delay time range, also it increases the area of the circuit with a little percent. By using this method in 32nm technology, the area of the circuit increases by 14% and the noise error decreases by 68%.

Keywords: level-shifter, capacitor, resistor, invertor, comparator.

Introduction. In electronics, a level shifter, (logic-level shifter, voltage level translator) is a circuit for signal translation from one voltage level to another, allowing compatibility between the circuits with different voltage requirements. Level shifters are used in modern systems to bridge domains between processors, logic and other circuits. The three most common logic levels are $1.8V$, $3.3V$, and $5V$. Levels above and below these voltages are also used. Level shifters have a wide application in interfacing legacy devices, also in SD cards, SIM cards CF cards, audio codecs, UARTs, etc.

The two main types of the level-shifters are the circuits which translate the high voltage to low voltage and the ones which translate low voltage to high voltage. The first type is simpler than the second, because getting a low voltage signal from a high voltage does not require a complex structure of a scheme. Also, as the circuit is simple and low output voltage does not require high power consumption, there are no such circumstances that can lead to big noises in the output.

In case of level-shifters which translate a low voltage signal to a high voltage, the working principle of the circuit is more complicated. The circuit structure has some components that bring about noises in the output, also the high

voltage switch causes a bigger amplitude of generated noises. The more complicated is the circuit of the level-shifter, the higher will be the noises in the output signal. So, there is a requirement to use an approach which will help to get an accurate high-voltage output signal for the level-shifter.

Literature review. There are several methods and approaches for reducing the output noises for different level-shifter circuits. For example in [1] a level shifter for noise and leakage suppression is presented. The level shifter is insensitive to noise on the input and also reduces the leakage current.

A level-shifter circuit characterized by high noise immunity and improved capacity is proposed in [2]. In difference to the conventional structure, the proposed circuit adopting two cross-coupled p-type transistors realizes the selective filtering ability by exploiting the path which filters out the noise. A differential noise cancellation scheme is designed to enhance the noise immunity further.

An improved noise immune level-shifter with gate-emitter voltage detection is presented in [3]. The circuit includes detection and pull down modules with process matching robustness and low circuit complexity. The noise is removed by monitoring the interval of the gate-emitter voltage variation and locking the output logic at the noise coming period.

A high-voltage level shifter with noise shielding is presented in [4]. The main principle is to determine whether there is noise through signal changes. When there is noise, the designed level shifter's output is locked by the noise shielding circuit. So, the designed level-shifter has infinite immunity, and it is not affected by the supply voltage, or processes.

A switched-capacitor level-shifting technique with sampling noise reduction for rail-to-rail input range instrumentation amplifiers is presented in [5]. In the proposed circuit, two adaptive level-shifting (ALS) schemes are combined with the two input stages of an Indirect Current-Feedback (ICF) instrumentation amplifiers.

A level-shifter for low power application is presented in [6]. The proposed schemes take advantage of the stacking technique's advantages of lower leakage current and also of the reduced leakage power. But the reduced supply voltage includes problems such as low voltage swing, insufficient noise margin, currents escaping from a leak. Power loss has increased to constitute a significant part of power dissipation as technology advances into the submicron range.

A level shifter for low power applications with a body bias technique is presented in [7]. In the work, three new innovative designs of the level shifter in the 0.35 μm technology using body bias approach are introduced. Issues of small voltage swing, insufficient noise margin, leakage currents are originating with the scaling of the power supply voltage.

The proposed low-to-high supply voltage level-shifter circuit. The experiments are carried out on the simple circuit of level-shifter, which is shown in Fig.1.

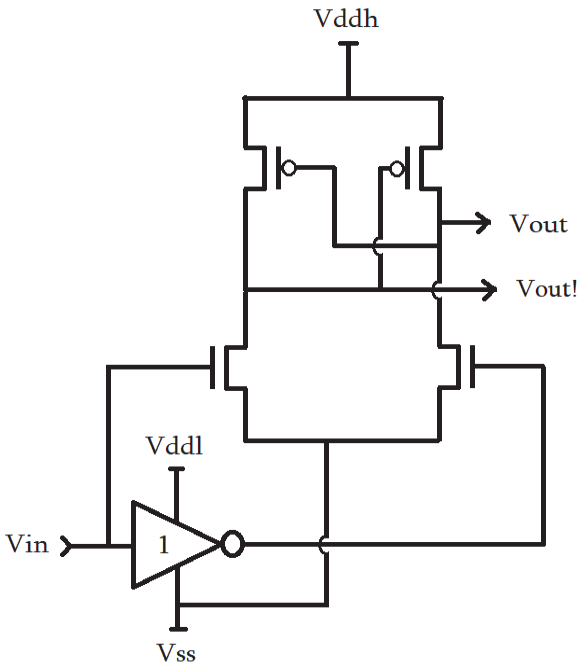

Fig.1. Primary circuit of the low-to-high supply voltage level-shifter (1 – invertor, Vout -straight output, Vout! – inverse output)

The comparator with high supply voltage generates high noises in the output. Using a capacitor in the output can solve the issue with noises, but it can lead to a bigger delay time range between the input and output signals, and it is not preferred as the delay time is long without using a capacitor because of a big output rise-fall time. So, there's a requirement to develop a method by which the delay time range will not increase and the output noises will reduce. The idea that can lead to the expected results use a transmission gate between the straight output and the inverse output, so that it will be on at the input switch moment with a very short time and will compensate the noises of the straight and inverse outputs. At the constant signal time it must be off.

Two chains with the capacitor and the resistor are connected to the input. The resistor of one chain is connected to the ground and the node between the resistor and the capacitor reaches the high voltage in a short time when the input signal changes from 0 to VDDL. That node is connected with the n-type transistor of the transmission gate, so, the n-type transistor appearing on a triode region compensates the noises of the straight and inverse outputs at the rise time.

Also, the resistor of a second chain is connected to the high supply voltage source and the node between the resistor and capacitor gets to the lower voltage from VDDH in a short time when the input signal changes from VDDL to 0. That node is connected with the p-type transistor of the transmission gate, so, the p-type transistor appearing on a triode region compensates the noises of the straight and inverse outputs at the fall time. By this approach, we get an output signal with reduced noises without increasing the delay time range. The circuit of the optimized level-shifter is shown in Fig.2.

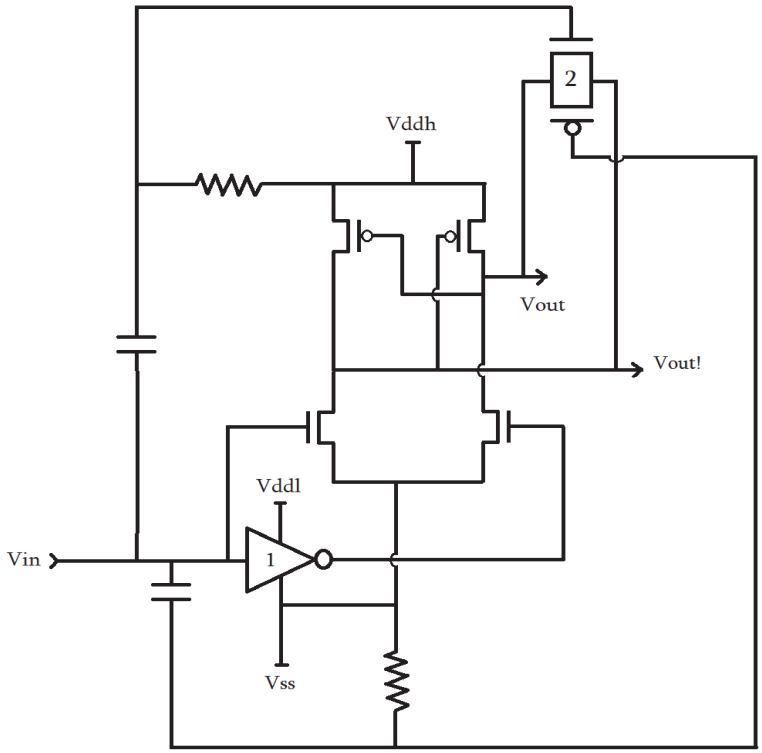

Fig.2. The optimized circuit of low-to-high supply voltage level-shifter (1 – invertor, 2 – transmission gate, Vout -straight output, Vout! – inverse output)

Simulation results. The main block of a low-to-high supply voltage level-shifter is designed. Simulations are performed using the HSPICE simulator (described in [8]) for a number of PVT corners including 3 main conditions (TT, FF and SS processes with respective voltage and temperature values). Here the results of the TT typical corner are presented. The circuit is designed and simulation is performed in the 32 *nm* technology. The primary circuit of the level-shifter designed in 32 *nm* technology is shown in Fig.3. Low supply voltage (VDDL) is 1.2 *V*, high supply voltage (VDDH) is 3.3 *V*, and the signal frequency is 1 *G*.

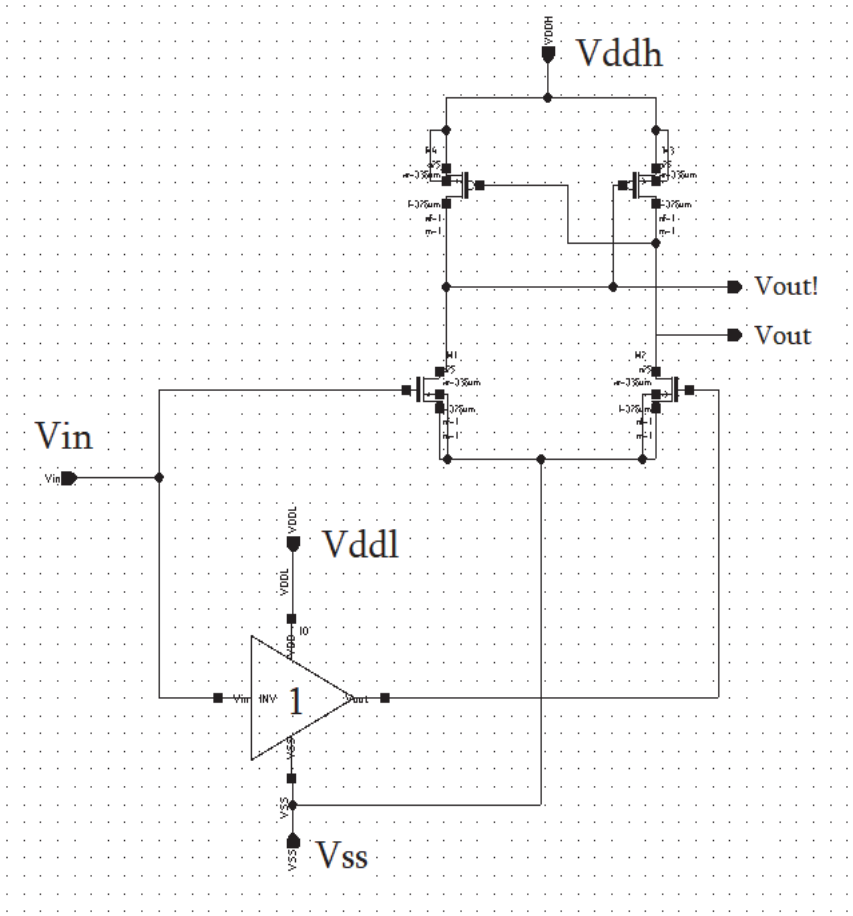

Fig.3. The primary circuit of low-to-high supply voltage level-shifter designed in 32 nm technology (1 - invertor)

The optimized low-to-high supply voltage level-shifter is shown in Fig.4.

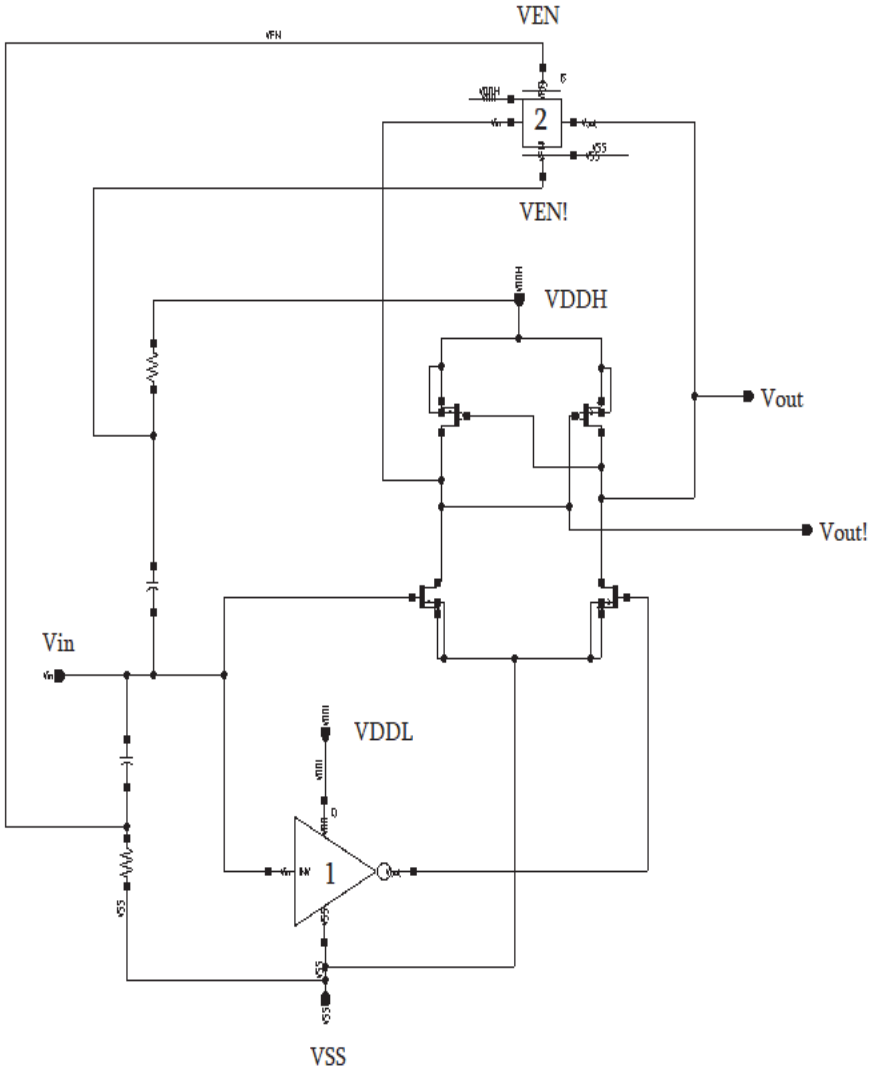

Fig.4. The optimized circuit of low-to-high supply voltage level-shifter designed in 32 nm technology (1 – invertor, 2 – transmission gate)

The added two capacitors, two resistors and the transmission gate increase the area of the circuit by 14%. The input and output signals of the primary level-shifter are shown in Fig.5.

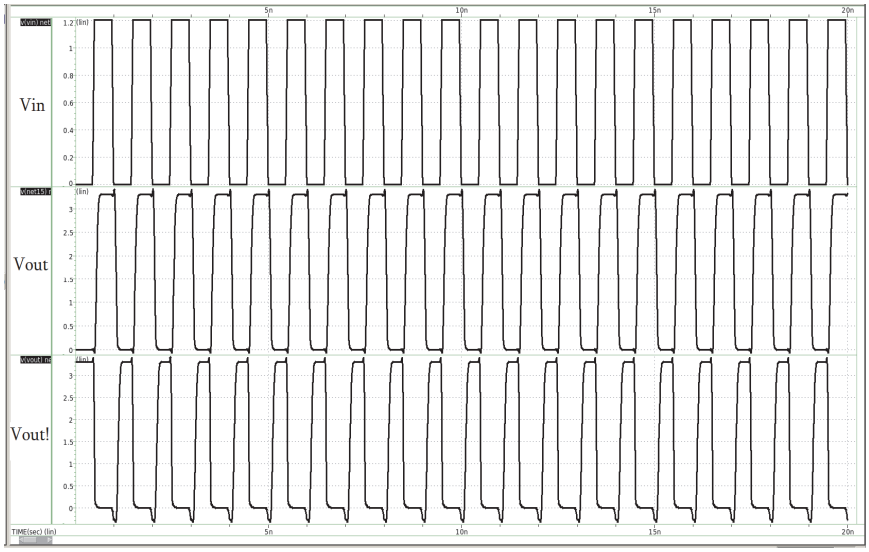

Fig.5. The input and output characteristics of the primary level-shifter (Vin – input signal, Vout – straight output signal, Vout! – inverse output signal)

The input and output signals of the optimized level-shifter are shown in Fig.6.

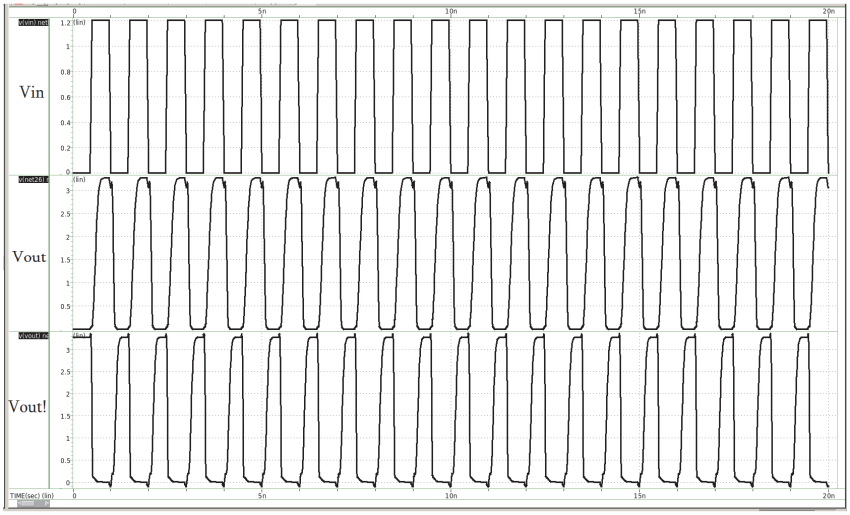

Fig.6. The input and output characteristics of the optimized level-shifter (Vin – input signal, Vout – straight output signal, Vout! – inverse output signal)

Noises of the output signal become less by 68% in the output signal by using the method.

Conclusion. A new method for noise reduction of the low-to-high supply voltage level-shifter is presented. In those level-shifters the higher is the supply

voltage, the higher will be the noises in the output signal, also the bigger the delay time range between the input and output signals. The experiments are carried out on the simple level-shifter circuit with an invertor and a comparator. By using the new method 2 capacitors, 2 resistors and one transmission gate are used. The advantage of this method is that it increases the area of the circuit by a very low percent in any technology, it does not increase the delay time range between the input and output signals in difference with output capacitors (which can also be required for the output noise reduction), it decreases the noises in the output with high percent and this method can be used almost in any type of low-to-high supply voltage level-shifter. By using the method, the area of the circuit increases by 14% and the noise strength decreases by 68% in the low-to-high supply voltage level-shifter designed in 32 *nm* technology.

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ՑԱԾՐԻՑ ԲԱՐՁՐ ՍՆՈՒՑՄԱՆ ԼԱՐՄԱՆ ՓՈԽԱՆՑՄԱՄԲ ԱՍՏԻՃԱՆԱՅԻՆ ՓՈԽԱՐԿԻՉԻ ԵԼՔԱՅԻՆ ԱՂՄՈՒԿՆԵՐԻ ՆՎԱԶԱՐԿՈՒՄԸ

Ներկայացված է աստիճանային փոխարկիչում ելքային աղմուկների նվազեցման նոր մոտեցում: Աստիճանային փոխարիչները, որոնք նախատեսված են ցածր ամպլիտուդային լարմամբ ազդանշանից բարձր ամպլիտուդային լարման ազդանշան ստանալու համար, մեծ խնդիր ունեն՝ կապված ելքային աղմուկների հետ: Աղմուկները, որոնք առաջանում են պարազիտային ունակություններից և այլ աղբյուրներից, ելքային ազդանշանում ավելի են մեծանում, քանի որ սխեման մեծացնում է մուտքային ազդանշանի ամպլիտուդը ելքում, ուստի մեծացնում է նաև աղմուկները: Այս աստիճանային փոխարկիչն ունի նաև հետաձգման ժամանակի խնդիր: Նրա մուտքային ազդանշանի և ելքային ազդանշանի միջև ուշացման միջակայքն այնքան էլ ցածր չէ: Աղմուկները նվազեցնելու համար ելքային ունակությունների օգտագործումը կարող է մեծացնել հետաձգման ժամանակի տիրույթը, ինչը լավ հատկանիշ չէ սխեմայի համար: Նոր մեթոդը նվազեցնում է ելքային աղմուկները՝ առանց ուշացման ժամանակի տիրույթը մեծացնելու, ինչպես նաև փոքր տոկոսով է մեծացնում շղթայի մակերեսը: Այս մեթոդը 32 նանոմետր տեխնոլոգիայի մեջ օգտագործելու դեպքում շղթայի մակերեսը մեծանում է 14%-ով, իսկ աղմուկի սխալանքը նվազում է 68%-ով:

Առանցքային բառեր. աստիճանային փոխարկիչ, կոնդենսատոր, ռեզիստոր, շրջիչ, կոմպարատոր:

А.А. БАБАДЖАНЯН, С.Х. ХУДАВЕРДЯН

МИНИМИЗАЦИЯ ВЫХОДНЫХ ШУМОВ ПРЕОБРАЗОВАТЕЛЯ УРОВНЯ С ПЕРЕХОДОМ ОТ НИЗКОГО ИСТОЧНИКА НАПРЯЖЕНИЯ ДО ВЫСОКОГО

Представлен новый подход к снижению выходных шумов в преобразователе уровня. У преобразователей уровня, предназначенных для преобразования высоковольтного амплитудного сигнала из низковольтного амплитудного сигнала, есть большая проблема, связанная с выходными шумами. Шумы, исходящие от паразитных емкостей и других источников, становятся намного выше на выходе, поскольку схема увеличивает амплитуду входного сигнала на выходе, поэтому она также увеличивает шумы. Другая проблема связана с временем задержки. Диапазон времени задержки между входным сигналом и выходным сигналом не так уж мал. Использование емкостей на выходе для уменьшения шумов может увеличить диапазон времени задержки, что не очень хорошо для схемы. Новый метод позволяет уменьшить выходные шумы, не увеличивая диапазон времени задержки, а также увеличить площадь схемы на небольшой процент. При использовании этого метода в технологии 32 *нм* площадь схемы увеличивается на 14%, а шумовая ошибка уменьшается на 68%.

Ключевые слова: переключатель уровня, конденсатор, резистор, инвертор, компаратор.