ISSN 0002-306X. Proc. of the RA NAS and NPUA Ser. of tech. sc. 2022. V. LXXV, N4

UDC 621.3.049.77 MICROELECTRONICS

DOI: 10.53297/0002306X-2022.v75.4-527

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# THE AGING INFLUENCE MINIMIZATION METHOD FOR OPERATIONAL AMPLIFIERS WITH THIN OXIDE TRANSISTORS

Nowadays CMOS technology feature size is being scaled aggressively. Supply voltage is not proportionally scaled, gate dielectric thickness is reduced and as a result, the devices are subjected to stronger electric fields, thereby causing stress on transistor. Stress causes aging degradation, which can lead to dramatic consequences on mobile devices, aircraft, military systems, or medical devices.

A method is proposed for designing two types of operational amplifiers with usage of only thin oxide devices, which are protected from stress conditions, namely from aging degradation. The proposed methods can also be implemented on other types of operational amplifiers.

***Keywords***: CMOS, stress, aging, thin oxide device, operational amplifier.

***Introduction.*** Continued scaling in modern submicron technologies leads to challenges in the design of integrated circuits (ICs). The increase of deviations in inter-circuit and intra-circuit ICs which is specific to 14nm and smaller technologies, as well as dramatic increase of the influence of various short-channel phenomena, complicate the design process [1]. Aging is one of those phenomena that leads to the deterioration of the reliability of the blocks. Therefore, not taking aging into account results in decrease in the yield of the ICs, and consequently decrease the profit [2].

Aging is the degradation of circuit performance during the time. It is mainly due to the degradation of the gate oxide and of the interface between the gate dielectric and silicon over time [3]. Two major aging effects are:

- Hot Carrier Injection (HCI): High electric field near the Si–SiO2 interface causes electrons or holes to gain sufficient energy from the electric field for crossing the interface potential barrier and enter into the oxide layer, which causes an increase in threshold voltage ($V_{th}$) and mobility degradation [4];
- Bias Temperature Instability (BTI): Threshold voltage shifts after a negative bias for PMOS, and positive bias for NMOS is applied at elevated temperatures. BTI has two phases:

1. Stress phase: Traps are generated at the Si-SiO2 interface and gate dielectric causing the magnitude of the threshold voltage to increase.

2. Relaxation phase: Some of the interface traps are removed causing the Vth to decrease, but the recovery cannot completely compensate the effect of the stress phase.

Consequently, the overall effect of BTI is an increase in the magnitude of threshold voltage and decrease in $I_{ds}$ (linear/saturation) over time [5, 6].

In some technological processes below 5 nm semiconductor manufacturing companies are facing difficulties for fabrication of transistors with thick gate oxide, which necessitates to replace all thick oxide devices with thin oxide devices, thereby causing difficulties at the design stages [7]. Inside the modern ICs, a major role are playing analog parts, which are responsible for receiving, processing, and transferring the information from one system to the other, furthermore they also are the most sensitive parts of ICs [8]. The majority of them, of which most important are operational amplifiers, are using high supply voltages for having high DC gain and a large working range [9]. Hitherto operational amplifiers are designed with thick oxide devices, and their replacement with thin oxide can cause stress, because of high supply voltages. Stress conditions between two terminals of a thin oxide transistor are lower than for a thick oxide transistor. All thin oxide transistors are designed and fabricated to have a maximum voltage difference between terminals (gate-drain ($V_{GD}$), gate-source ($V_{GS}$), drain-source ($V_{DS}$)) equal to low supply voltage, and using them in high supply voltage analog blocks can cause stress on those devices, which will lead to more aging degradation. This problem needs a solution to make the devices work under non-stress conditions.

**The proposed solution and simulation results.** In order to solve the device overstress issue and to provide acceptable conditions for the device functionality, cascading and connecting floating nodes to the bias voltage methods could be used (Fig.1) [10]. With these simple methods devices will be under working conditions defined by factories (no stress) and will have much longer lifetime. Generally, the cascode transistors gate receives bias voltage which limits source voltage of NMOS below bias voltage and source voltage of PMOS above bias voltage, otherwise transistors will be closed. The correctly chosen bias voltage value for cascode devices will lead to a desirable effect, that is no stress in the circuit.

The vpbias and vnbias values could be generated using voltage dividers or bandgap reference, with proper matching techniques in layout the voltage should not vary more than 5%. The PB and NB signals are also for protecting devices from stress, they can be applied from multi output level converters [11]. For PB signal low level is vpbias and high level is VDDH, and for NB signal it is 0 and vnbias correspondingly.

These methods have been used to solve overstress issues in 2 types of operational amplifiers, which will be introduced and discussed in detail in the next sections.

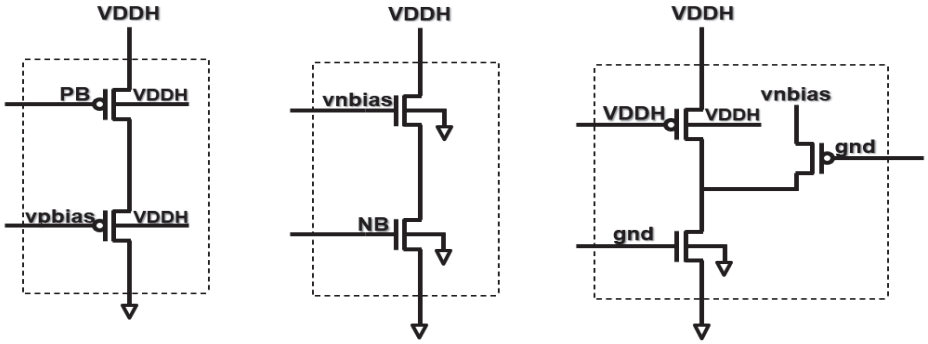


*Fig. 1. Cascading and connecting floating nodes to the bias the voltage methods*

**1. The Two-Stage operational amplifier.** Two-stage is one of most common types of operational amplifiers, which is to provide high DC gain and is usually used inside the biasing circuits. The schematic view (Fig. 2) and HSPICE simulation results (Fig. 3) of the two-stage operational amplifier designed by SAED14*nm* FinFET technology are presented below [10, 12, 13].

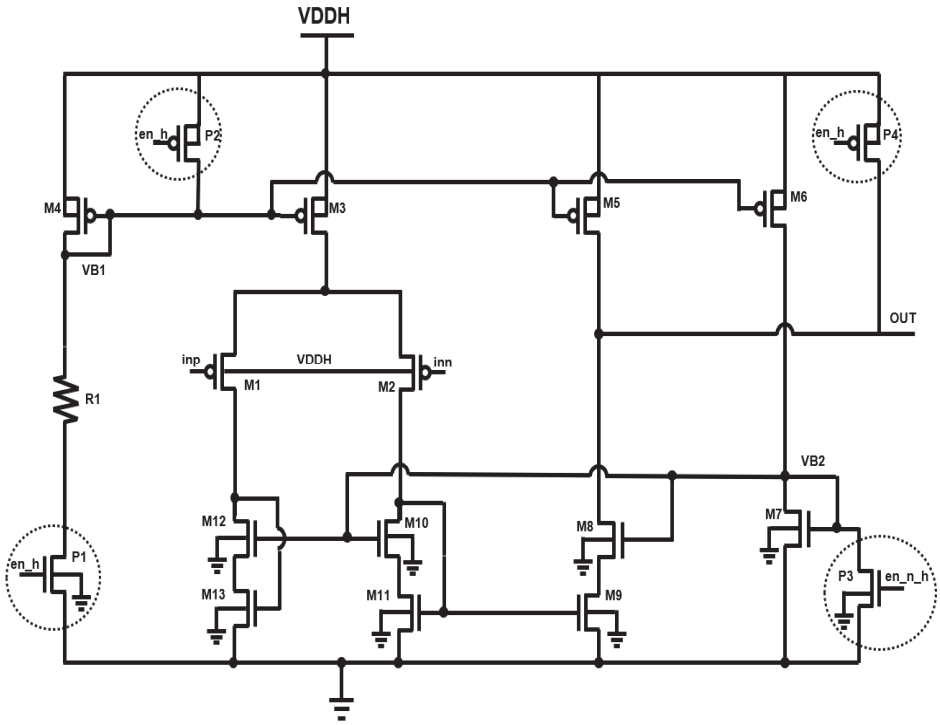


*Fig. 2. Schematic view of the two-stage op-amp*

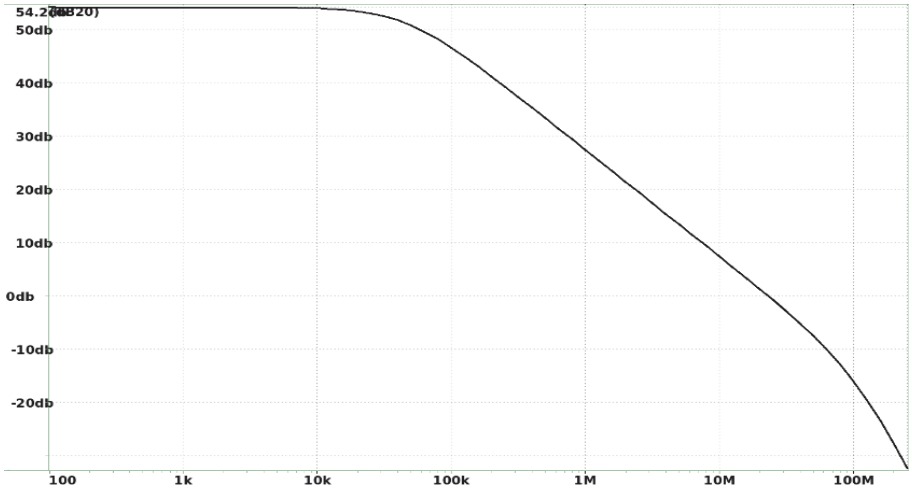


*Fig. 3. Ac characteristic of the designed two-stage op-amp*

The transistors indicated in dashes are used to enter circuit to the power down mode. The P1, P2 and P3 transistors cut all the paths for the current flow, and P4 pulls up output to VDDH. Nowadays, almost all circuits have the power down mode, some circuits can even spend more time of their life in that mode than in the normal operating mode. Thus, it's necessary to take into account the design challenges at power down mode in order to avoid stress, which can cause aging degradation.

To evaluate the aging effect on the parameters of the two-stage operational amplifier, we need to perform aging simulations. The goal of the aging simulation is to estimate the lifetime of circuits and correct any transistor with significant degradation or performance shift. For that investigation, semiconductor manufacturing companies are providing their own aging models which accurately describe the degradation of devices during lifetime.

In order to examine the aging degradation of the designed two-stage operational amplifier, the SPICE simulations for lifetime of 10 years have been performed in 2 operating modes: normal operation mode and power down mode. During normal operation mode it was found that there is no significant aging degradation on the main devices, and the degradation of $I_{ds}$ and $V_{th}$ parameters is in acceptable ranges, except the P1 power down device. As a result, the op-amp main parameters didn't experience significant change. Instead, in the power down mode serious aging degradations were observed for some main devices and power down devices, which leads to the reduction of DC gain approximately by 14 db. In Table 1, devices are presented that have significant $V_{th}$ and $I_{ds}$ shifts in the normal and power down modes.

*Table 1*

*$V_{th}$ and $I_{ds}$ variation for most degraded devices for the two-stage op-amp*

| Transistor name | Normal operation mode | | Power down mode | |
|---|---|---|---|---|
| | $\Delta V_{th}$ (*mV*) | $\Delta I_{ds}$ (*%*) | $\Delta V_{th}$ (*mV*) | $\Delta I_{ds}$ *(%)* |
| M6 | 22 | 2.1 | 175 | 17.4 |
| M8 | 19 | 1.8 | 172 | 16.9 |
| P1 | 152 | 15.5 | 127 | 12.8 |
| P2, P4 | 0.1 | 0.1 | 198 | 21.6 |
| P3 | 0.1 | 0.1 | 198 | 21.6 |

The degradation of P1 power down device during normal operation mode is due to its control signal, which varies from 0 to VDDH domain. During normal operation mode P1 is open, control signal is VDDH level and $V_{GS}$ is VDDH, which is not permissible and causes stress.

During power down mode P2 and P4 power down devices should be open, and their control signal is 0, so $V_{GS}$ and $V_{GD}$ is VDDH. The P3 device gate is connected to the VDDH level signal, thus $V_{GS}$ and $V_{GD}$ is VDDH. The P1 device is operating in the off mode and gate voltage is 0 but the P2 device drives the P1 drain to VDDH, thus $V_{GD}$ for P1 is VDDH, which is not allowed either and causes stress, although it is in the off mode. The M6 device is in the off mode, because P2 drives the M6 gate to VDDH, and P3 drives the M6 drain to 0, so $V_{GD}$ is VDDH for M6. The M8 device is also in the off mode, because P3 drives the M8 gate to 0, and P4 drives the M8 drain to VDDH, so M8 $V_{GD}$ is VDDH.

The results achieved show that there is no problem in the normal operation mode but there are problems during the power down mode, which needs to be solved. In order to solve the observed problems, the following modifications have been realized in the amplifier:

1. The power down enable signal has been separated for NMOS and PMOS devices. Additionally, their logic 0 and logic 1 domains have been changed, using multi output level converter (from 0 to vnbias for NMOS, and from vpbias to VDDH for PMOS).

2. The cascading method has been used by adding the D1, D2 and D3 devices (indicated in red dashes) (Fig. 4).

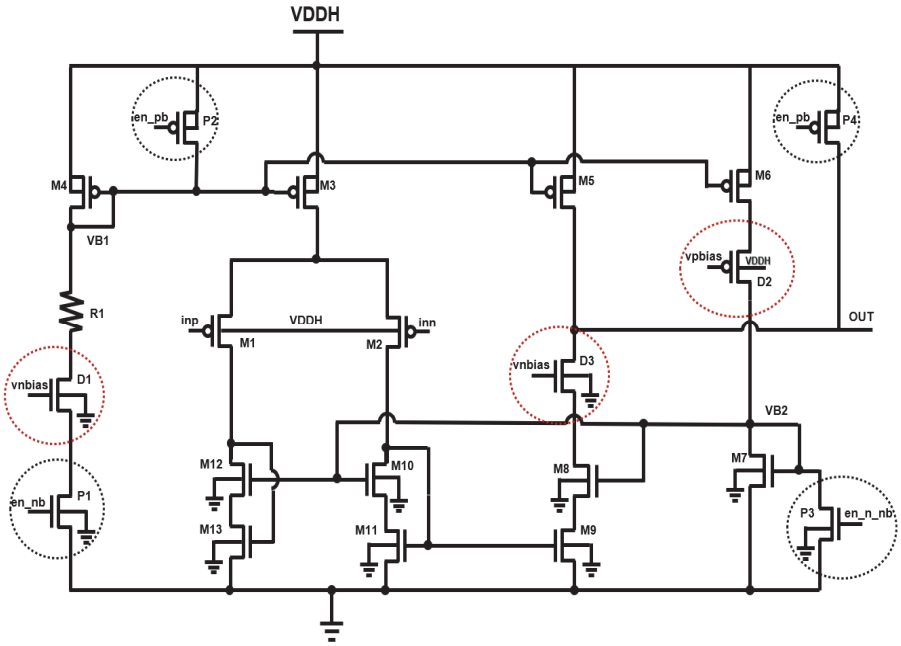


*Fig. 4. Schematic view of the two-stage op-amp after modifications*

D1, D2 and D3 are cascode devices and they do not change the functionality of the circuit but will protect functional and power down devices from stress. After these changes, aging simulations have been performed and it was found that the problems are solved and there is no significant degradation either in normal mode, or in power down mode (Table 2). The main parameters have not been changed either.

*Table 2*

*$V_{th}$ and $I_{ds}$ variation for the two-stage op-amp after modifications*

| Transistor name | Normal operation mode | | Power down mode | |
|---|---|---|---|---|
| | $\Delta V_{th}$ ($mV$) | $\Delta I_{ds}$ (%) | $\Delta V_{th}$ ($mV$) | $\Delta I_{ds}$ (%) |
| M6 | 18 | 1.7 | 0.1 | 0.1 |
| M8 | 15 | 1.2 | 0.1 | 0.1 |
| P1 | 17 | 1.4 | 0.1 | 0.1 |
| P2, P4 | 0.1 | 0.1 | 6 | 1.2 |
| P3 | 0.1 | 0.1 | 6 | 1.2 |

**2. Folded-Cascode operational amplifier.** Folded-cascode operational amplifiers are widely used inside voltage regulators to provide high DC gain. Below are presented the schematic view (Fig. 5) and the HSPICE simulation results (Fig. 6) of the folded-cascode operational amplifier designed by SAED 14*nm* FinFET technology [10].

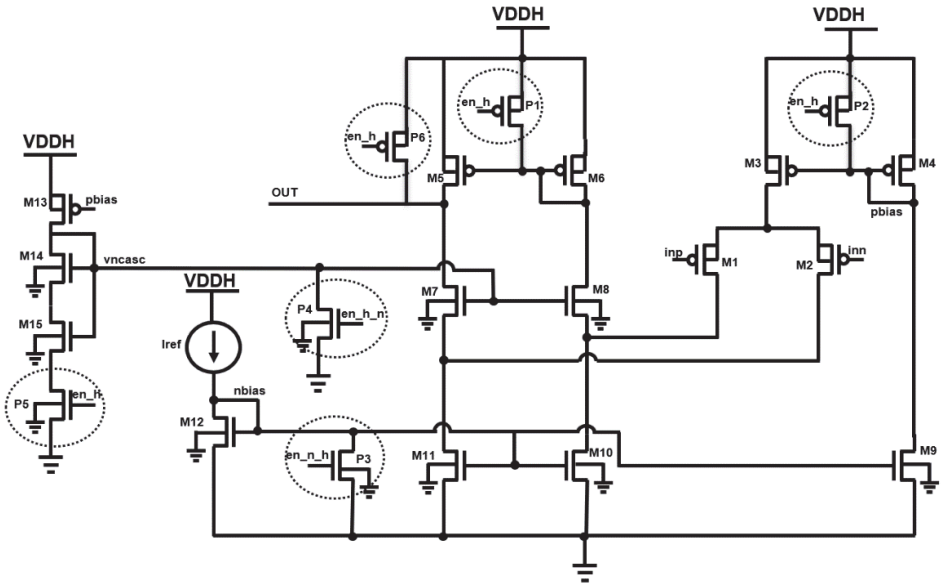


*Fig. 5. Schematic view of the folded-cascode op-amp*

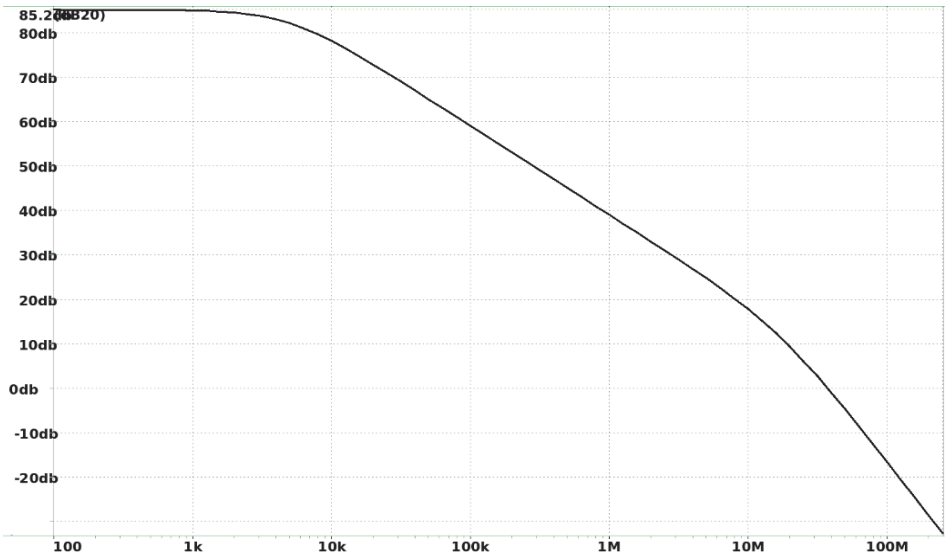


*Fig. 6. AC characteristic of the designed folded-cascode op-amp*

The transistors indicated by dashes are used to enter the circuit into the power down mode. The P1, P2, P3, P4 and P5 transistors cut all the paths through which a current can flow, and P6 pulls up the output to VDDH.

To investigate the aging degradation of the designed folded cascode operational amplifier the SPICE simulations for 10 years have been performed for

2 operating modes: normal operation mode and power down mode. In normal operation mode it was detected that there is no significant aging degradation on the main devices, and the degradation of $I_{ds}$ and $V_{th}$ parameters is in acceptable ranges except the P5 power down device, as a result, the main parameters have not been changed significantly. At the same time in the power down mode, severe aging degradations were observed for some main devices and power down devices, which leads to the reduction of DC gain approximately by 19 *db*. After 10 years of aging, the obtained results for devices with significant $V_{th}$ and $I_{ds}$ shifts for normal and power down modes are presented in Table 3.

*Table 3*

*$V_{th}$ and $I_{ds}$ variation for most degraded devices for the folded-cascode op-amp*

| Transistor name | Normal operation mode | | Power down mode | |
|---|---|---|---|---|
| | $\Delta V_{th}$ ($mV$) | $\Delta I_{ds}$ (%) | $\Delta V_{th}$ ($mV$) | $\Delta I_{ds}$ (%) |
| M7, M8 | 24 | 3.1 | 192 | 19.6 |
| M9 | 20 | 2.8 | 198 | 20.1 |
| P1, P2, P6 | 0.1 | 0.1 | 252 | 24.2 |
| P3, P4 | 0.1 | 0.1 | 254 | 24.3 |
| P5 | 148 | 14.2 | 0.1 | 0.1 |

The degradation of the P5 power down device in the normal operation mode and another power down devices in the power down mode are due to their control signal causing stress, which have been discussed in previous section.

In the power down mode the M9 device is off because P3 drives M9 gate to 0 and P2 drives M9 drain to VDDH, so $V_{GD}$ is VDDH. Devices M7 and M8 are under the same conditions and are also operating in the off mode because P4 drives M7 and M8 gates to 0, P6 drives M7 and P1 drives M8 drains to VDDH, so for both $V_{GD}$ is VDDH and the sources are floating.

The obtained results indicate that there is no problem in normal operation mode but there are problems in the power down mode to which solutions should be given. To solve the problems that have arisen, the following changes have been implemented in the amplifier:

1. The power down enable signal has been separated for NMOS and PMOS devices. Additionally, their logic 0 and logic 1 domains have been changed, using multi output level converter (from 0 to vnbias for NMOS, and from vpbias to VDDH for PMOS).

2. The cascading method has been used by adding the D1 device (indicated in red dashes).

3. Added the D2, D3 and D4 devices for the connecting the floating nets to vnbias in the power down mode (indicated in red dashes).

4. The P4 NMOS device has been replaced by the PMOS device and the source has been changed from GND to vnbias (indicated in red dashes) (Fig. 7).

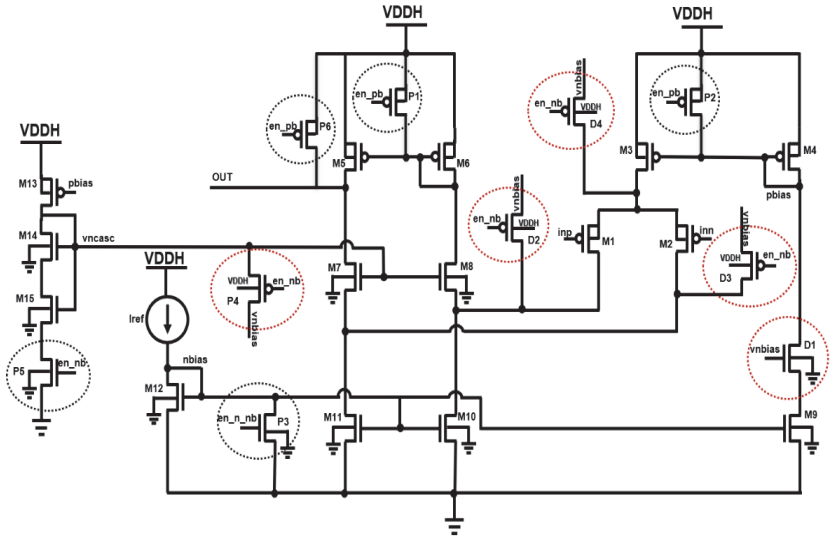


*Fig. 7. Schematic view of the folded-cascode op-amp after modifications*

The D1 device will prevent the M9 device from stress. Now the P4 device will drive the gates of M7 and M8 devices to vnbias, meanwhile D2 and D3 will drive sources of M7 and M8 to vnbias. Thus, they will be closed and not liable to stress, because there will be no stress conditions between the terminals.

After those changes, aging simulations have been performed and it was found that problems are solved and there is no significant degradation either in normal mode or in the power down mode (Table 4). The main parameters have not changed either.

*Table 4*

*Vth and Ids variation for folded-cascode op-amp after modifications*

| Transistor name | Normal operation mode | | Power down mode | |
|---|---|---|---|---|
| | $\Delta V_{th}$ ($mV$) | $\Delta I_{ds}$ (%) | $\Delta V_{th}$ ($mV$) | $\Delta I_{ds}$ (%) |
| M7, M8 | 22 | 2.9 | 0.1 | 0.1 |
| M9 | 18 | 2.6 | 0.1 | 0.1 |
| P1, P2, P6 | 0.1 | 0.1 | 20 | 2.8 |
| P3, P4 | 0.1 | 0.1 | 20 | 2.8 |
| P5 | 17 | 2.1 | 0.1 | 0.1 |

**Conclusion.** Two types of operational amplifiers have been designed with the SAED 14 nm FinFet technology by using the Galaxy Custom Designer tool

[14]. Schemes have been designed only using thin oxide devices. The phenomena of aging have been examined on the designed amplifiers during normal operation and power down modes. With standard architecture it was found that there is a serious aging impact on the main parameters of amplifiers especially in the power down mode, due to stress conditions on the thin oxide devices. New schematic solutions have been implemented to prevent stress conditions on the devices, which improved the variation of Ids and Vth parameters due to aging degradation in a 10 year lifetime.

The summary table of the designed amplifiers before and after the proposed design updates, with a 10-year aging is summarized in Table 5.

*Table 5*

*Summary table*

| Parameter | Two-stage | | Folded-cascode | |
|---|---|---|---|---|
| | Before | After | Before | After |
| DC gain (*dB*) | 40.2 | 54.2 | 66.2 | 85.2 |
| $\Delta V_{th}$ (*mV*) | 198 | 18 | 254 | 22 |
| $\Delta I_{ds}$ (%) | 21.6 | 1.7 | 24.3 | 2.9 |

In conclusion, the proposed methods can be implemented on all types of operational amplifiers for decreasing degradation due to aging.

***Acknowledgment.*** *The work was supported by the Science Committee of RA, in the frames of the research project № 21T-2B002.*

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## ԲԱՐԱԿ ՕՔՍԻԴԻ ՇԵՐՏՈՎ ՏՐԱՆԶԻՍՏՈՐՆԵՐՈՎ ՕՊԵՐԱՑԻՈՆ ՈՒԺԵՂԱՐԱՐՆԵՐԻ ԾԵՐԱՑՄԱՆ ԵՐԵՎՈՒՅԹՆԵՐԻ ԱՋԴԵՑՈՒԹՅԱՆ ՆՎԱԶԵՑՄԱՆ ՄԵԹՈԴ

Ներկայումս ԿՄՈԿ տեխնոլոգիաների չափերը գերակտիվորեն մասշտաբավորվում են, սակայն սնման լարումները համապատասխան կերպով չեն մասշտաբավորվում, փականի դիէլեկտրիկի հաստությունը փոքրանում է, ինչի արդյունքում սարքերը ենթարկվում են ուժեղ էլեկտրական դաշտի ազդեցության՝ առաջացնելով սթրես տրանզիստորներում։ Սթրեսը առաջացնում է ծերացում, որը կարող է հանգեցնել անդառնալի հետևանքների շարժական սարքերի, ինքնաթիռների, ռազմական համակարգերի կամ բժշկական սարքերի դեպքերում։

Առաջարկվում է երկու տեսակի օպերացիոն ուժեղարարների նախագծման մեթոդ՝ օգտագործելով միայն բարակ օքսիդի շերտով տրանզիստորներ, որոնք պաշտպանված են սթրեսային պայմաններից, այսինքն՝ ծերացումից։ Առաջարկվող մեթոդները կարող են կիրառվել նաև այլ տեսակի օպերացիոն ուժեղարարների դեպքում։

***Առանցքային բառեր.*** ԿՄՈԿ, սթրես, ծերացում, բարակ օքսիդի շերտով տրանզիստոր, օպերացիոն ուժեղարար։

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# МЕТОД МИНИМИЗАЦИИ ВЛИЯНИЯ СТАРЕНИЯ ОПЕРАЦИОННЫХ УСИЛИТЕЛЕЙ НА ТОНКИЕ ОКСИДНЫЕ ТРАНЗИСТОРЫ

В настоящее время размер функции технологии комплементарных металл-оксид-проводников (КМОП) агрессивно масштабируется. Напряжение питания масштабируется непропорционально, толщина диэлектрика затвора уменьшается, в результате чего устройства подвергаются более сильным электрическим полям, вызывая тем самым стресс на транзисторах. Стресс вызывает старение, которое может привести к драматическим последствиям для мобильных устройств, самолетов, военных систем или медицинских устройств.

Предлагается метод проектирования двух типов операционных усилителей с использованием только тонких оксидных устройств, защищенных от стрессовых воздействий, а именно - от старения. Предлагаемые методы могут быть реализованы и на других типах операционных усилителей.

***Ключевые слова:*** КМОП, стресс, старение, транзистор с тонким оксидным слоем, операционный усилитель.