ISSN 0002-306X. Proc. of the RA NAS and NPUA Ser. of tech. sc. 2022. V. LXXV, N3

UDC 621.382.323 **MICROELECTRONICS**

DOI: 10.53297/0002306X-2022.v75.3-398

N.D. YEZAKYAN, A.E. YESAYAN, J-M. SALLESE

VERILOG_A IMPLEMENTATION OF NANOWIRE JUNCTIONLESS ISFET COMPACT MODEL AND READ-OUT CIRCUIT DESIGN

In this paper, we implement nanowire (NW) junctionless (JL) ISFET model in Verilog-A hardware language. The Verilog-A implementation would allow the NW ISFET integration with signal processing circuits. The simulated by the code pH values are compared with the corresponding data from COMSOL simulations, and a good agreement is observed. The readout circuit based on amperometric switched- capacitors schemes is designed. The readout circuit has introduced good linearity in pH values range from 3 to 7.

Keywords: Nanowire, ISFET, PH-sensor, readout circuit.

Introduction. Since the first application of Ion-Sensitive Field Effect Transistors (ISFET) as bio-chemical sensors [1], the technological evaluation of ISFETs has passed from planar to 1D (e.g. nanowire) geometries [2-4]. Nanowire (NW) geometry is very attractive for sensor applications as the high surface to volume ratio and comparable to biomolecule sizes, result in very high sensitivity [2,3]. The fabrication of NW does not require complicated technologies making the NW-based sensor production more reliable and commercially attractive [3,4].

In line with experimental realization of these new generation of ISFETs, the compact analytical modelling is essential for the device optimization. A uniformly doped NW ISFET can be treated as junctionless (JL) NW ISFET and this modeling approach has been presented in [5,6]. The ISFET model is based on JL NW FET model presented in [7], which was later explicitly formulated in [8]. The developed NW JL ISFET model allows an accurate description of the influence of physical and geometrical parameters on device pH sensitivity [9]. In this paper, we implement the explicitly formulated NW JL ISFET model introduced in [6] in Verilog-A, to run it in circuit simulator and present readout circuit design for the first level realization.

Methodology: Implementation of JLNW ISFET Compact model in a circuit simulator. The SIMetrix simulator core is chosen for our simulations, since it gives the possibility of coding and modeling in real time. This tool gives flexibility to make modifications in the code, and to use the same model again. The software offers simulation languages, such as PSPICE, HSPICE, and Verilog-A,

etc [10]. We implement the model in Verilog-A hardware language as it is less error prone, support for buses, optional parameter range checking; always-faster evaluation speed required in the NR loop, always-lower memory footprint is required.

1. Analytical explicit model. For the sake of clarity, at first, we will introduce the NW JL ISFET model main equations in an analytical form. The semiconductor NW charge and current calculations are based on the NW JL FET model presented in [7,8], and generalized for NW JL ISFET in [5,6]. The NW JL ISFET structure and band diagram are presented in Fig. 1.

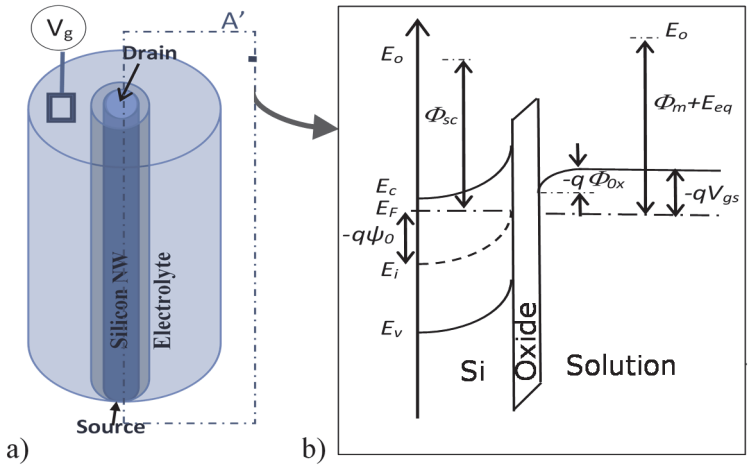

Fig. 1. The structure of the NW JL ISFET (a), and the energetic diagram of vertical cut (b)

The relationship between the bulk pH in electrolyte and the gating potential on the oxide surface (Φ_G) is given by the following equation:

$$2.3\left(\mathrm{pH_{zpc}}-\mathrm{pH}\right)=\frac{\Phi_G}{U_T}\frac{V_{gs}^{*}}{U_T}\operatorname{arcsinh}\left(\frac{C_{eff}(\Phi_G-V_{gs}^{*})-Q_{sc}}{qN_s\delta}\right), \quad (1)$$

where Q_{sc} is the total charge density in the semiconductor, $\Phi_G = V_{gs}^{*} + \Phi_{ox}$, where Φ_{ox} is the potential drop across the electrolyte (see Fig. 1(b)), and V_{gs}^{*} is the effective gate voltage applied to the reference electrode inserted in the electrolyte. All other parameters in equations (1)-(3) are well defined in [6].

The increase of pH in the bulk electrolyte causes the depletion of the semiconductor channel, consequently, for $pH > \mathrm{pH_{zpc}}$, the JL ISFET will operate in depletion if $V_{gs}^{*} \le V_{FB}$, where $V_{FB} = U_T \cdot ln\left(\frac{N_D}{n_i}\right)$. Once the device operates in depletion, we can use the explicit charge [8]:

$$Q_{SC}(\Phi_G, V) = -C_n + Q_D^* \sqrt{1 - \frac{8Q_D C_{Si} U_T}{Q_D^{*2}} \ln\left(1+\exp\frac{\Phi_G - V - V_T + f_{sm}\cdot V_\delta}{U_T}\right)}. \quad (2)$$

By substituting (3) into (2), the bulk pH is explicitly defined for a given Φ_G, whereas Φ_G will be defined from the drain current equation by substituting the drain current value measured by the sensor.

The explicit drain current equation for the NW JLFET is:

$$I_{Dep}(\Phi_G, V_D, V_S) = \frac{\pi R}{L}\mu\left\{\left(\frac{1}{8C_{si}} - \frac{1}{4C_{ox}}\right) Q_{sc}{}^2\Big|_{V_S}^{V_D} - \frac{1}{12Q_d C_{si}} Q_{sc}{}^3\Big|_{V_S}^{V_D} + \left(\frac{Q_d}{2C_{ox}} + 2\,U_T\right) Q_{sc}\Big|_{V_S}^{V_D} - \right.$$
$$\left. - U_T Q_d \, ln\left(1 + \frac{Q_{sc}}{Q_d}\right)^2\Big|_{V_S}^{V_D}\right\}. \quad (3)$$

The Verilog-A code of NW JL ISFET model starts with the initialization of “disciplines.vams” and "constants.vams" libraries, then constants such as geometrical and physical parameters, as well as variables used in the model are defined. Finally the main part of the model starts. For clarity, two pieces from the model code are presented in Appendix 1.

By measuring the sample, we fix the measured current, therefore, in SIMetrix simulator the drain current value is considered to be known. We have validated pH values calculated at a given drain current by the circuit simulator with the corresponding data from COMSOL simulations. The comparison is illustrated in Fig. 2, and indeed very good agreement is observed. The difference between the data from these simulations is less than 0.01 for PH range from 3 to 8.

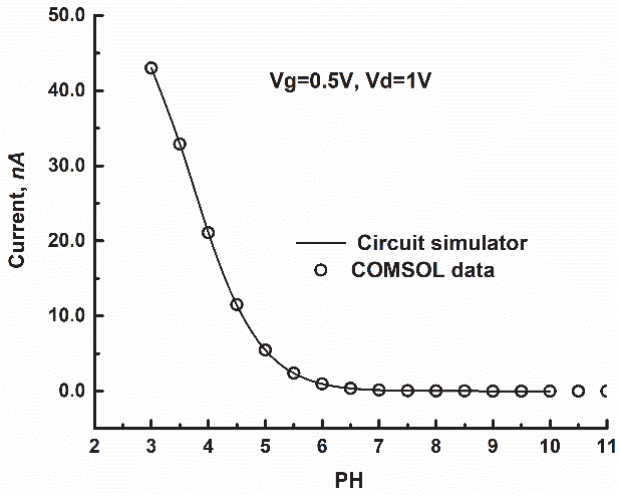

Fig. 2. Current dependence on pH calculated from COMSOL and SIMetrix

2. Readout circuit for NW JL ISFET. The next step is to design a readout circuit for the NW JL ISFET. There are different readout circuit types: (i) potentiometric; (ii) amperometric; and (iii) impedance-based [11, 12]. Amperometric techniques require three electrodes, namely "working" (sensor), "reference", and "auxiliary" electrodes, consequently as we use three-electrode configuration (reference, drain, and source), the amperometric measurement configuration is the correct choice.

A classic switched-capacitors reset mechanism, that also performs correlated-double sampling circuit, we choose as a reference for designing our amperometric measurement circuit [11, 13].

The designed readout circuit is presented in Fig. 3. The circuit consists of the following blocks: 1) NW_JL ISFET model configuration circuit; 2) The first stage current amplification; 3) The second stage current amplification; 4) Current to voltage converter circuit. We have used two stage current amplification circuits, namely 3 LM7171 op-amps, which are known as very high speed, high output current, and voltage feedback amplifiers [14]. For simplicity, op-amp voltage supply sources are not shown here.

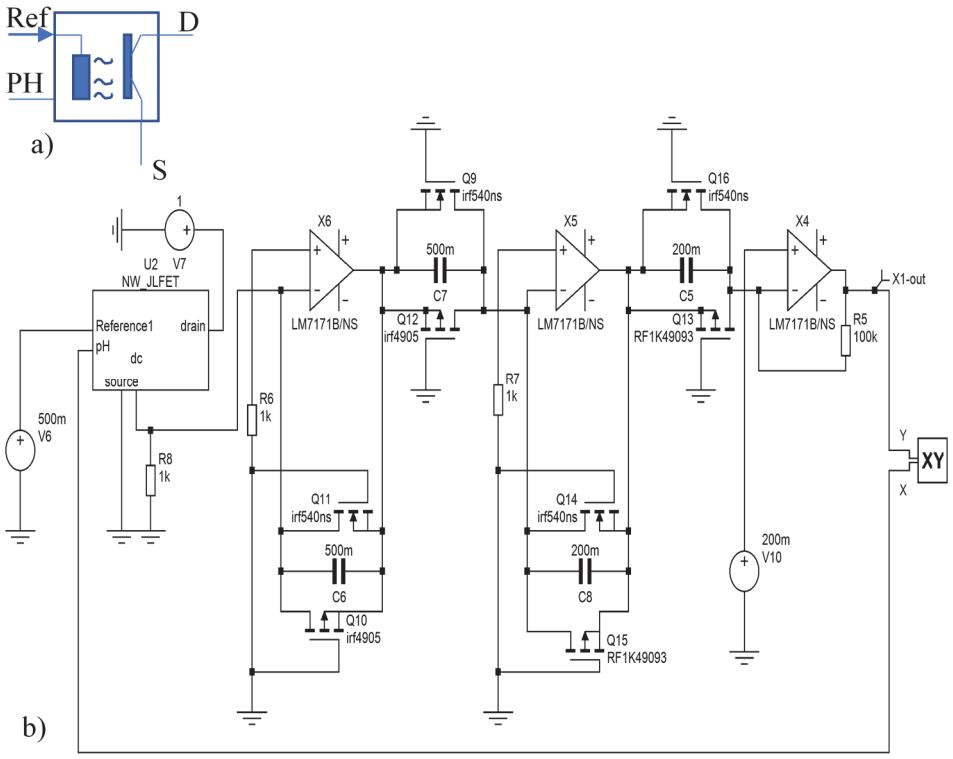

Fig. 3. (a) Sub-circuit block of JLFET, (b) Amperometric switched-capacitors circuit

The sub-circuit, illustrated in Fig. 3 (a), consists of: Reference (Ref), Drain (D-) and Source (S) electrodes and (pH)-solution pH value. In Reference and Drain pins we set 0.5V and 1 V DC power supplies respectively. The first block (U2 block) simulates the NW JL ISFET model written in Verilog-A. The measured drain current is given to dc output pin of U2 -NW_JLFET block (see Fig. 4 (b)). The calculated PH value is set to pH pin.

In addition, we calculate the circuit output voltage versus the output current in dc pin. The current data correspond to pH values varying from 3 to 7. The calculations are presented in Fig. 4. It is seen that the designed circuit exhibits a good linearity.

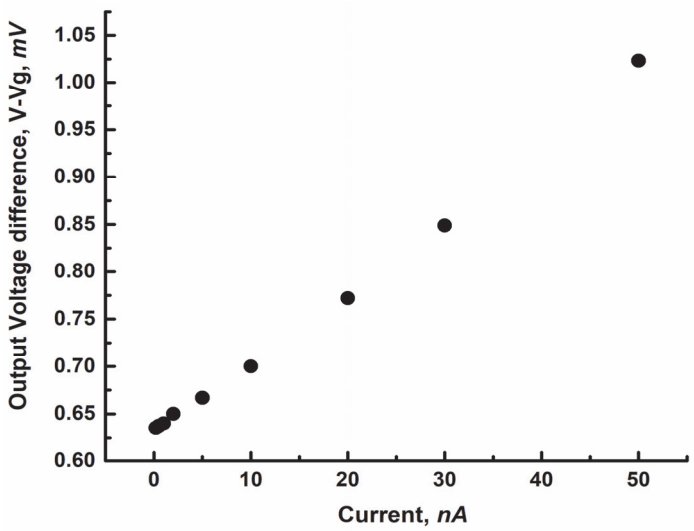

Fig. 4. The circuit current to output voltage conversion

Conclusion. The analytical compact model of the NW JL ISFET has been implemented in Verilog-A, and the measuring circuit of ISFET has been designed. The sensing readout circuitry of ISFET has been developed on the basis of switched-capacitors amperometric schemes. The pH sensor circuit exhibits good linearity.

Acknowledgements. The work was supported by the Science Committee of RA, in the frames of the research project № 21T-2B321. In addition, the authors would like to acknowledge Seed Funding Grant (UNIGE).

Appendix 1.

Here are presented two main pieces of Verilog_A code.

//Libraries are called and the main parameters are already defined.

```
for (i=0; i<20; i=i+1)
    begin
    k=0;
for (i=1;i<2000; i=i+1)
    begin

        fsms    =   0.5-0.5*tanh (0.2 * (FIG-V(source)-VT)/UT)   ;
        fsmd    =   0.5-0.5*tanh (0.2 * (FIG-V(drain)-VT)/UT)    ;

        QDeps   =   -QD*Cn + QDa* sqrt
                                  (


        QDepd   =   -QD*Cn +
        QDa* sqrt(1-8*(1/(QDa*(1+Cn))*Csi*UT*ln

        Idep = pi*R/LSi * u * ((1/(8*Csi)-
            FIG =FIG - 5E-4;
         I(drain)<+ Idep;
        if (abs(Idep-ID)<0.6*pow(10,-n))
            begin
                k=k+1;
                Av  =   0.072;
                VGeff   =   V(Reference1)   -   Av;
                PH  =   -(
                if (k==1)
                    begin
                $strobe ("FIG=",,FIG);
                //$strobe ("flatband=", ,VFB);
                $strobe ("ID=",,Idep);
                $strobe ("pH",,PH);
                $strobe ("none",,   );
                    end
    end
```

// equations are shown in short form

```
for (i=0; i<20; i=i+1)
            begin

            if (k<0.1) n=n+1;
            k= 10 *k;
            end

        for (i=1;i<2000; i=i+1)
            begin

            fsms    =   0.5-0.5*tanh (0.2 * (FIG-
            fsmd    =   0.5-0.5*tanh (0.2 *

                QDeps   =   -QD*Cn + QDa* sqrt
                                        (


                QDepd   =   -QD*Cn + QDa* sqrt(1-

                Idep = pi*R/LSi * u * ((1/(8*Csi)-
                    Av  =   0.072;
                        VGeff   =   V(Reference1, source)
                        -   Av;
                        PH  =   -(
                    FIG =FIG - 5E-4;
                if (abs(Idep-ID)<1*pow(10,-n))
                    begin
                        k1=k1+1;

                        if (k1==1)
                            begin
            end
                //PH= PH+0.5;
        end
```

REFERENCES

1. **Hal R.V., Eijkel J., and Bergveld P.** A novel description of ISFET sensitivity with the buffer capacity and double-layer capacitance as key parameters // Sens. Actuators B, Chem.-1995.- 24. -P.201–205.
2. **Patolsky F., and Lieber C.M.** Nanowire nanosensors // Mater. Today.-2005.- 8(4).-P.20–28.
3. **Ramgir N.S., Yang Y., Zacharias M.** Nanowire-Based Sensors // Small.-2010.-6(16).-P.1705–1722.
4. Junctionless gate-all-around nanowire field-effect transistors with an extended gate in biomolecule detection / **C.W. Chen, R.Z. Lin, L.C. Chiang, et al** // Jpn. J. Appl. Phys.-2019.-58(2).-P.027001.
5. **Yesayan A., Jazaeri F., and Sallese J.-M.** Analytical Modeling of Double-Gate and Nanowire Junctionless ISFETs // IEEE Trans. on Electron Devices.-2020.-67.-P.1157-1164.
6. **Yesayan A., and Sallese J. -M.** Compact Analytical Model of Nanowire Junctionless ISFET // 28th International Conference on Mixed Design of Integrated Circuits and System.- Krakow, Poland, June 2021.-P. 31-34.
7. A common core model for junctionless nanowires and symmetric double-gate FETs / **J.M. Sallese, F. Jazaeri, L. Barbut, et al //** IEEE Trans. Electron Devices.-2013.-60(12).-P. 4277–4280.
8. **Yesayan A., Prégaldiny F., and Sallese J.M**. Explicit drain current model of junctionless double-gate field-effect transistors // Solid. State. Electron.-2013.-89.-P.134–138.
9. **Yesayan A., Petrosyan S., Papiyan A., Sallese J-M.** Theoretical Studies of Nanowire Ion-Sensitive Field Effect Transistor // J. Contemp. Phys.- 2021. -56. -P. 324–331. https://doi.org/10.3103/S1068337221040071
10. **O'Halloran, P.** 'Verilog-A in SPICE//MOS-AK, December 2014.- Berkeley, CA, 2014.
11. CMOS Interfaces for Internet-of-Wearables Electrochemical Sensors: Trends and Challenges / **M. Dei, J. Aymerich, M. Piotto, et al** // Electronics.-2019.-8.-P.150.
12. ISFET-based sensors for (bio)chemical applications: A review / **S. Cao, P. Sun, G. Xiao, et al** // ELSA.-2022.-P.e2100207.
13. Ultra-low-noise CMOS current preamplifier from DC to 1 MHz / **G. Ferrari, M. Farina, F. Guagliardo, et al** // Electronics letters.-2009.-45 (25).
14. LM7171 SNOS760C–May 1999–revised September 2014, https://www.ti.com/lit/ds/symlink/lm7171.pdf

Institute of Radiophysics and Electronics NAN RA, Yerevan State University. The material is received on 01.10.2022.

Ն.Դ. ԵԶԱԿՅԱՆ, Ա.Է. ԵՍԱՅԱՆ, Ժ-Մ. ՍԱԼԼԵՍ

ՆԱՆՈԼԱՐԱՅԻՆ ԱՆ-ԱՆՑՈՒՄԱՅԻՆ ISFET ՄՈԴԵԼԻ VERILOG-A ԻՐԱՑՈՒՄԸ ԵՎ ԿԱՐԴԱՑՈՂ ՇՂԹԱՅԻ ՆԱԽԱԳԾՈՒՄԸ

Իրականացվել է նանոլարային ան-անցումային իոնազգայուն դաշտային տրանզիստորի մոդելի իրացումը Verilog-A լեզվով: Մոդելի Verilog-A իրացումը թույլ է տալիս իոնազգայուն տրանզիստորի ազդանշանի մշակման սխեմաների միմյանց ինտեգրում: Ստացված pH արժեքները համեմատվել են COMSOL մոդելավորման համապատասխան տվյալների հետ, և նկատվել է տվյալների լավ համաձայնություն: Նախագծվել է ընթերցման սխեմա՝ հիմնված ամպերաչափիչ անջատիչ կոնդենսատորներով սխեմաների վրա: Ընթերցման սխեման ցուցաբերել է լավ գծայնություն pH-ի 3-ից 7 արժեքների միջակայքում:

Առանցքային բառեր. նանոլար, իոնազգայուն ԴՏ, PH – տվիչ, ընթերցող շղթա:

Н.Д. ЕЗАКЯН, А.Э. ЕСАЯН, Ж-М. САЛЛЕЗ

РЕАЛИЗАЦИЯ КОМПАКТНОЙ МОДЕЛИ НАНОПРОВОЛОЧНОГО БЕСПЕРЕХОДНОГО ISFET НА ЯЗЫКЕ VERILOG-A И ПРОЕКТИРОВАНИЕ СХЕМЫ СЧИТЫВАНИЯ

Реализована модель нанопроволочного бесперехoдного ионно-чувствительного транзистора на языке Verilog-A, что позволяет проводить его интегрирование со схемами обработки сигналов. Сопоставление полученных значений pH с соответствующими данными расчетов COMSOL показало хорошее совпадение. Спроектирована схема считывания на основе амперометрических схем с переключаемыми конденсаторами. Данная схема считывания обеспечивает хорошую линейность в диапазоне значений pH от 3 до 7.

Ключевые слова: нанопроволока, ионно-чувствительный транзистор, pH-сенсор, схема считывания.