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A MODEL FOR CALCULATING THE PROPAGATION DELAY OF DIGITAL ELEMENTS CONSIDERING THE RADIATION IMPACT

This paper proposes a model for calculating the propagation delay of digital elements taking into account radiation-induced single event transients (SET). The main idea of this work is to determine the propagation delay of digital elements in integrated circuits (IC) without running the circuit level simulation. Analytical equations are derived to calculate the propagation delay of logic gates. The propagation delay of NAND gates chain is evaluated with proposed analytical formulas and with HSPICE simulation. The comparison of the evaluation results between HSPICE simulation and the model shows that the created analytical model forecasts the propagation delay of digital elements with a 90.3% of accuracy. This model can be integrated into the design process of radiation hardened ICs.

Keywords: single event transients (SET), Technology Computer-Aided Design (TCAD), complementary metal-oxide-semiconductor (CMOS), propagation delay, analytical model, single event upsets (SEU), soft errors, linear energy transfer (LET), radiation effect.

Introduction. Digital integrated circuits (IC) are widely used in electronic systems which operate in different environments such as aerospace and nuclear reactors. In such environments, ICs are under the influence of high radiation. Energetic particles formed in the radiation zone hit the sensitive region of ICs and form new electron-hole pairs. The generated electron-hole pairs may lead to a transient pulse which can alter several parameters of CMOS digital elements. The propagation delay is one of the parameters which could be altered by radiation. The generated transient pulse is known as a single event transient (SET). The SET formation and propagation through the entire logic may change the states of latches or other memory elements [1]. This kind of degradation can be masked by several factors which can eliminate the SET's propagation. It is known that there are temporal, logical and electrical masking factors [2]. Although those masking factors cancel the SET error, the correct behavior of ICs is not guaranteed in all circumstances.

The consideration of the SETs becomes more important with the process and technology scaling. Several researches show that with the scaling of the technology, electronic devices will be increasingly susceptible to SETs [2]. Such vulnerability can cause degradation of parameters of digital elements which may lead to serious issues. Therefore, the development of new and reliable SET

sensitivity analysis methods, which will be used in the design process of IC is crucial. Several SET analysis and methods require circuit level simulation. However, circuit level simulation and circuit analysis, considering SETs depending on the amount of the transistors in the design can be time consuming. The number of transistors in ICs is growing, which manifests the need for development of new methods in other abstraction levels of the design flow [1]. The main goal of this study is to provide an analytical model, which will determine digital IC's propagation delay dependency on the SET effect without using the circuit-level simulation.

The SET impact on 2-input NAND gate propagation delay. High energy particles in radiation environment such as neutrons, heavy ions, protons or alpha particles strike the surface of the CMOS circuits forming SET effect. Generally, the SETs occur on the OFF-state transistors as the generated electron-hole pairs collected by the drain [2].

In HSPICE, the SET can be represented as a current spike which is modelled, by using a double exponential current source [3]. The equation (1) illustrates the current pulse function [4]:

$$I_{SET} = I_{peak} * \frac{\left(e^{-\frac{t-t_{SET_{end}}}{\tau_2}} - e^{-\frac{t-t_{SET_{start}}}{\tau_1}}\right)}{\cos(\Theta)}, \quad (1)$$

where I_{peak} - is the maximum amplitude of the current, τ_1 - the collection time constant of the junction, and τ_2- the time constant of the initial establishment of the ion track, t_{SET_start} – is the SET strike moment, t_{SET_end} – the end of SET, θ - the impact angle of a high energy particle to the surface of the circuit in radians. The total current goes up as the angle of the incident particle rises. The approximate maximum current is linearly proportional to the energy of the particle (2):

$$I_{peak} = \frac{Q}{(\tau_1 - \tau_2)}, \quad (2)$$

where Q is the amount of the collected charge.

The equations show that the amplitude of the current pulse I_{SET} and the duration of the current pulse T_{SET} are the major influencing parameters to be considered in calculation of the propagation delay. The duration of the SET is calculated by equation (3):

$$T_{SET} = t_{SET_{end}} - t_{SET_{start}}. \quad (3)$$

As an example of impact of a high-energy particle strike, a 2-input NAND gate is modelled with the above explained double exponential current pulse function. Fig.1 presents the mechanism of injection of the double exponential current source on the sensitive transistors of the NAND gate.

Assume that input A of the NAND gate is set to logic ”1” and input B changes over time. The moment that the input B switches from logic “1” to logic “0” transistors M2 and M4 are at the OFF state which means they are vulnerable to the SETs. In Fig 1a. the SET strike at the sensitive M2 transistor is shown. The current pulse generation at the moment of switching from “1” to “0” leads to rising of low to high propagation delay Fig 1b.

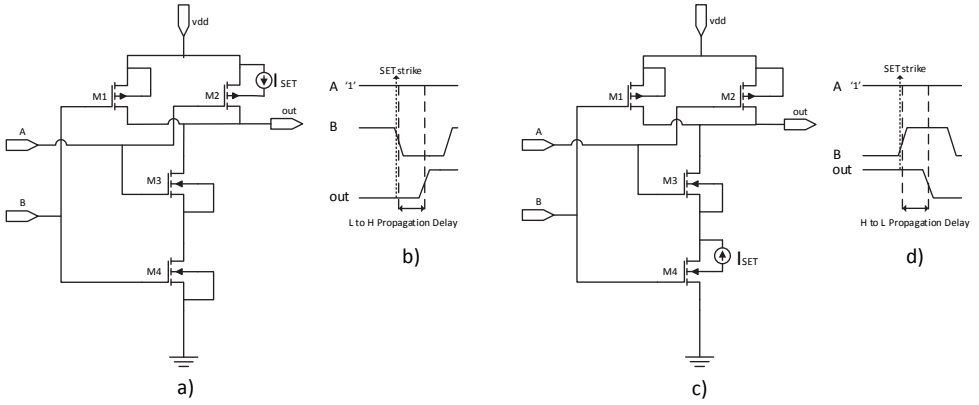

Fig.1. Injection of double exponential current source on a) sensitive M2 transistor b) low to high propagation delay formation after the SET strike c) the SET impact at the sensitive transistor M4 d) high to low propagation delay formation after the SET strike

On the other hand, when input B changes from logic “0” to logic “1” transistors M3 and M4 are defenseless against the SETs. In Fig 1c SET impact at the sensitive transistor M4 is presented. In this case high to low propagation delay rises when input B changes from logic “0” to “1” Fig. 1d. a SET strike on a NMOS transistor is simulated with a current injected between the drain of the transistor and out the body of the transistor. The SET impact on a PMOS transistor is simulated with a current flowing through the body to the drain of the device.

Such behavior of logic gates after they are exposed to SET radiation effect leads to the increase of propagation delay. If the event occurs in the critical parts of IC, single event upsets (SEU) or soft errors [2] can be formed.

HSPICE transient analysis for different radiation levels is performed to calculate high to low and low to high propagation delays of a 2-input NAND gate by injecting a double exponential pulse given by (1) at SET sensitive transistors M2 and M4. The linear energy transfer (LET) of the energetic particle and current

pulse parameters are given in Table 1 which are gathered from TCAD simulations [4] and other realistic statistical data [5].

Table 1

Current pulse parameters

Q[fc]	$\tau_1[ps]$	$\tau_2[ps]$	$T_{SET}[ps]$	θ [rad]	LET [$MEV\ cm^2mg^{-1}$]
8	10	20	12	30	0.25
10	10	20	23	30	1
100	10	20	50	30	10
300	10	20	80	30	14.47
525	10	20	110	30	25.31
801	10	20	140	30	38.62
990	10	20	250	30	47.74
1200	10	20	270	30	57.86

HSPICE simulation results of 2-input NAND gate for low to high propagation delay ($T_{L\to H}$) are presented in Table 2 [6]. $T_{L\to H}$ rises with the increase of the amplitude (I_{SET}) and the duration (T_{SET}) of the current pulse. An example of such simulation is presented in Fig. 2, when T_{SET} = 80 ps and I_{SET} = 800 μA. The results show that the $T_{L\to H} = 99.814\ ps$.

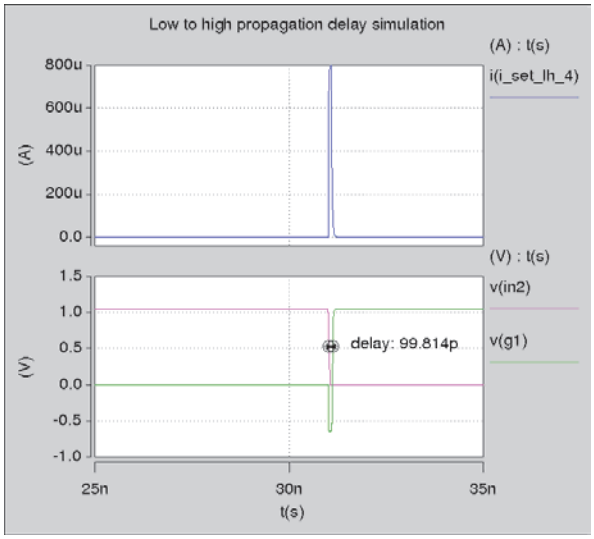

Fig.2. HSPICE simulation results for2-input NAND gate low to high propagation delay when T_{SET} = 80 ps and I_{SET} = 800 μA

Table 2

HSPICE Simulation results for 2-input NAND gate low to high propagation delay

$T_{SET}[ps]$	$I_{SET}[\mu A]$	$T_{L\to H}[ps]$
12	140	16.90
23	677	39.57
50	740	68.27
80	800	99.81
110	1650	143.32
140	1900	177.12
250	1600	283.67
270	1700	304.91

Similarly, 2-input NAND gate's HSPICE simulation results for high to low propagation delay $T_{H\to L}$ are presented in Table 3. High to low propagation delay also gets bigger when the amplitude (I_{SET}) and the duration (T_{SET}) of the current pulse values rise.

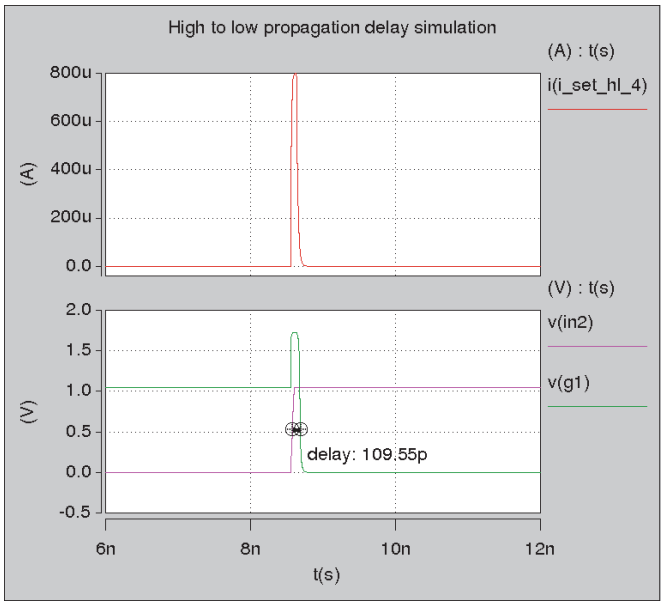

Fig.3. HSPICE simulation results for 2-input NAND gate high to low propagation delay when T_{SET} = 80 ps and I_{SET} = 800 μA

Table 3

HSPICE Simulation results for 2-input NAND gate high to low propagation delay

$T_{SET}[ps]$	$I_{SET}[\mu A]$	$T_{H\to L}[ps]$
12	140	18.56
23	677	48.99
50	740	77.99
80	800	109.55
110	1650	154.04
140	1900	186.67
250	1600	293.44
270	1700	314.67

An HSPICE simulation example of high to low propagation delay is presented in Fig. 3, where the delay is equal to $109.55\ ps$.

The proposed technique to calculate propagation delay of digital elements considering the radiation exposure. Based on HSPICE simulation results presented in Tables 2 and 3, analytical equations for low to high (4) and hight to low (5) propagation delay calculation of 2-input NAND gate are proposed. The equations are created using Wolfram Mathematica tool's [7] "fit data" algorithms.

$$T_{PD_{L\to H}} = 30.9632 + 0.102407 * T_{SET} + 0.00233277 * T_{SET}^2 - 4.77198e^{-6} * * T_{SET}^3 - -0.0784258 * I_{SET} + 0.00128404 * T_{SET} * I_{SET} - 7.62958e^{-7} * T_{SET}^2 * * I_{SET} + +1.16931e^{-5} * I_{SET}^2 - 5.184347e^{-7} * T_{SET} * I_{SET}^2 - 2.763716e^{-8} * * I_{SET}^3, \quad (4)$$

$$T_{PD_{H\to L}} = -16.5627 + 0.938275 * T_{SET} - 0.0045319 * T_{SET}^2 + 0.0000113 * * T_{SET}^3 + 0.205052 * I_{SET} + 0.000658129 * T_{STE}\, I_{SET} - 2.26109e^{-6} * * T_{SET}^2 I_{SET} - -0.0002773 * I_{SET}^2 - 6.81333e^{-8} * T_{STE} I_{SET}^2 + 1.15608e^{-7} * * I_{SET}^3. \quad (5)$$

The Fig. 4 3D plot compares the HSPICE simulation (dotted plot) and the analytical calculation (4) results (solid plot) of low to high propagation delay. The results are approximately equal. Which confirms the effectiveness of equation (4).

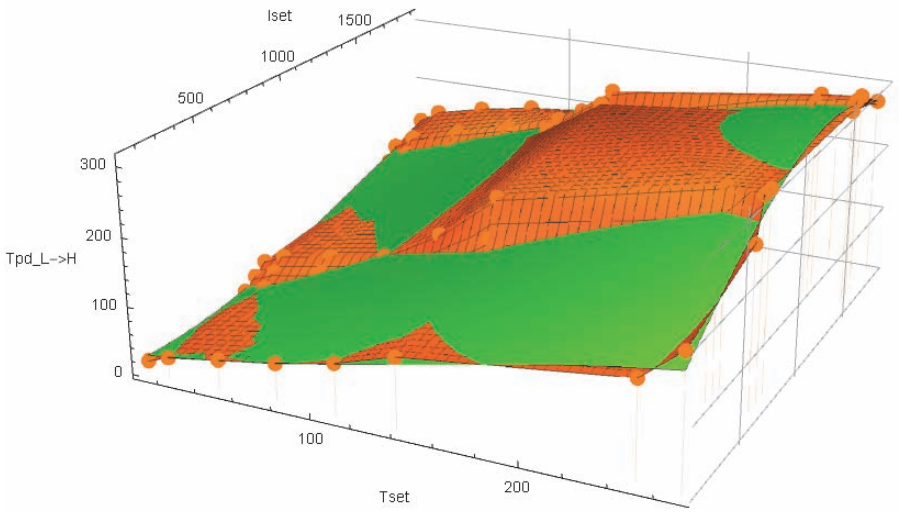

Fig.4. The 3D plot comparison of 2-input NAND gate's *low to high propagation delays measured with HSPICE simulation "dotted plot" and with analytical equation "solid plot"*

Moreover, table 4 shows the propagation delay results with the SET duration of $T_{SET} = 80\ ps$ and the current pulse level with $I_{SET} = 800\ [\mu A]$. The absolute percentage error between the results of HSPICE simulation and equation (4) is 1.3 %.

Table 4

The comparison of 2-input NAND gate *low to high propagation delay evaluation using HSPICE simulation and the analytical equation.*

$T_{SET}[ps]$	$I_{SET}[\mu A]$	$T_{L\to H}[ps]$ (Analytical Equation)	$T_{L\to H}[ps]$ (HSPICE)	Absolute percentage error %
80	800	101.2	99.81	1.3

Fig. 5 represents the 3D plot comparison of HSPICE simulation (dotted plot) and the results of high to low propagation delay obtained using equation (5) (solid plot). The results are almost the same which means that equation (5) is effective to be used in high to low propagation delay calculation as well.

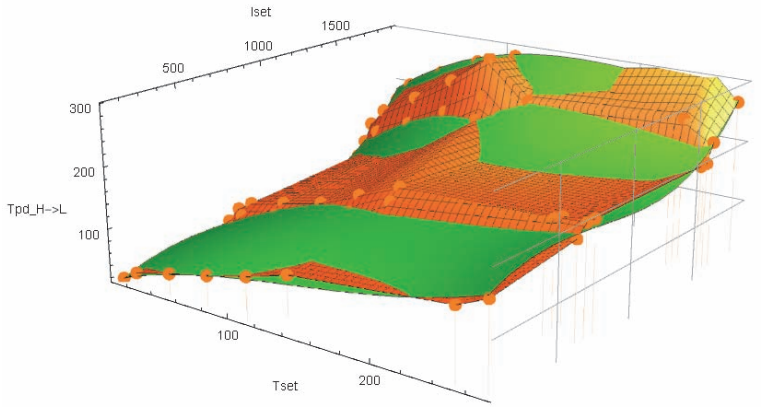

Fig.5. The 3D plot comparison of 2-input NAND gate's *high to low propagation delays dependency on T_{SET} and I_{SET} measured with HSPICE simulation "dotted plot" and with analytical equation "solid plot"*

Table 5 shows the high to low propagation delay results with the SET duration $T_{SET} = 80\ ps$ and the current pulse level with $I_{SET} = 800\ [\mu A]$ resulting after the SET the influence. The absolute percentage error is 1.3%.

Table 5

The comparison of high to low propagation delay evaluation using HSPICE simulation and the analytical equation

$T_{SET}[ps]$	$I_{SET}[\mu A]$	$T_{L\to H}[ps]$ (Analytical Equation)	$T_{L\to H}[ps]$ (HSPICE)	Absolute percentage error %
80	800	108.05	109.55	1.3

Model validation. To prove the effectiveness of the proposed method, assume that there are ten 2-input NAND gates connected one after another as a chain of inverters. The SET strikes on the first NAND gate (Fig.6) with an input voltage Vin = 1.05 V and Vdd = 1.05 V. Using the proposed analytical equations, the propagation delay of the entire circuit can be evaluated by equation (6) [8]:

$$T_{PD} = \left(\frac{T_{PD_{L\to H}} + T_{PD_{H\to L}}}{2}\right) + 9 * Avarage(T_{NAND\_delay}) \qquad (6)$$

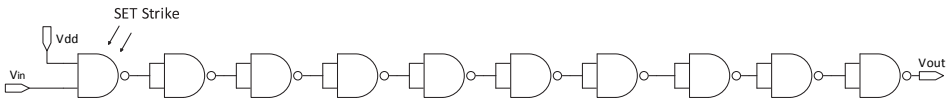

Fig.6. Ten 2-input NAND gates connected to each other as a chain of inverters exposed to a SET radiation effect

The propagation delay measurement results of the chain of NAND gates exposed to radiation are presented in Table 6. HSPICE simulation and analytical equation evaluation results are presented correspondingly in the "HSPICE T_{PD}" and "Analytical Equation T_{PD}" columns.

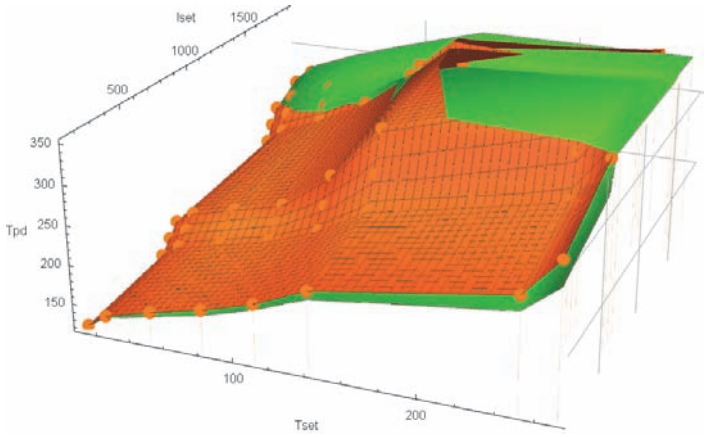

Fig.7. 3D plot comparison of chain of ten NAND gates propagation delay, measured with HSPICE simulation "dotted plot" and with analytical equation (4) "solid plot"

Fig. 7 presents the 3D plot comparison of the chain of NAND gates propagation delay, measured with HSPICE simulation (dotted plot) and with analytical equation (5) (solid plot).

The results obtained from HSPICE simulation and analytical model are listed in Table 6.

Table 6

Ten 2-input NAND chain propagation delays extracted from the Analytical Equation and HSPICE measurements

$T_{SET}[ps]$	$I_{SET}[\mu A]$	HSPICE T_{PD} [ps]	Analytical Equation T_{PD} [ps]
12	140	119.62	119.60
23	677	152.53	147.22
50	740	181.51	174.08
80	800	213.67	202.04
110	1650	257.56	294.66
140	1900	290.38	350.89
250	1600	396.95	342.69
270	1700	418.17	350.70

To prove the accuracy of the analytical model the Mean Absolute Percentage Error has been calculated (MAPE). Using the model proposed in this work, MAPE is equal to 9.76%. This means that the model provides the necessary accuracy to be

used in the design of digital ICs, considering that radiation induces the SET effects to the calculate the propagation delay of integrated circuits without the need to run SPICE-like simulations. Moreover, the machine execution times in case of the analytical model and SPICE simulation are compared. HSPICE simulations and modeling of the particle strike at NAND gates chain, takes more than 3 minutes. While using the analytical equations, the evaluation time of the propagation delay is less than 30 seconds. This shows that by using the proposed model, the design of a radiation-hardened integrated circuit can be sped up for more than 6 times.

Conclusion. An accurate and efficient analytical model for determining the digital element's propagation delay dependency on the single event transient effect (SET) is proposed. By using the model, the propagation delay of digital elements can be calculated without circuit level simulations. The SET generation through logic gates is modelled based on TCAD simulation and statistical data.

The Comparison of the results obtained by the model, with circuit level simulation results shows that, the delay calculation using the proposed analytical model is close to HSPICE simulation results. The accuracy of the model is 90.3% and the design of radiation-hardened digital IC can be sped up for more than 6 times. The model validation results prove that this analytical model is suitable to be used in digital IC design flow for determination of the CMOS circuit sensitivity to radiation-induced SETs.

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ՌԱԴԻԱՑԻՈՆ ՃԱՌԱԳԱՅԹՄԱՆ ԱԶԴԵՑՈՒԹՅՈՒՆԸ ՀԱՇՎԻ ԱՌՆՈՂ ԹՎԱՅԻՆ ՏԱՐՐԻ ՀԱՊԱՂՈՒՄՆԵՐԻ ՀԱՇՎԱՐԿՄԱՆ ՄՈԴԵԼ

Առաջարկվում է ինտեգրալ սխեմաներում (ԻՍ) տրամաբանական տարրերի հապաղումների հաշվարկման նոր մոդել՝ հաշվի առնելով ռադիատցիոն ճառագայթման արդյունքում առաջացած եզակի պատահարի ժամանակային անցման երևույթը (ԵՊԺԱ): Աշխատանքի նպատակն է ԻՍ-ում տրամաբանական տարրերի հապաղման ժամանակի որոշումը՝ առանց տրանզիստորների մակարդակի մոդելավորման: Հապաղման ժամանակի որոշման նպատակով արտածվել են վերլուծական բանաձևեր: Վերլուծական բանաձևերի և HSPICE տրանզիստորների մակարդակի մոդելավորման միջոցի օգտրագործմամբ չափվել է «ԵՎ-ՈՉ» տրամաբանական տարրերից բաղկացած շղթայի հապաղման ժամանակը: Առաջարկվող մոդելի և HSPICE տրանզիստորների մակարդակի մոդելավորման միջոցի արդյունքների համեմատությունը ցույց է տվել մոդելի 90.3% ճշգրտությունը: Մոդելը կարող է կիրառվել ժամանակակից ռադիացիոն ճառագայթման նկատմամբ կայուն ԻՍ-երի նախագծման գործնթացում:

Առանցքային բառեր. եզակի պատահարի ժամանակային անցման երևույթ, ԿՄՕԿ, հապաղման ժամանակ, վերլուծական բանաձև, եզակի պատահարի խափանում, անցողիկ սխալներ, էներգիայի գծային փոխանցում, ռադիացիոն ճառագայթման երևույթ:

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МОДЕЛЬ РАСЧЕТА ЗАДЕРЖКИ РАСПРОСТРАНЕНИЯ СИГНАЛА ЦИФРОВЫХ ЭЛЕМЕНТОВ С УЧЕТОМ РАДИАЦИОННОГО ВОЗДЕЙСТВИЯ

Представлена модель для расчета задержки распространения сигнала цифровых элементов с учетом радиационных кратковременных переходных процессов. Основная цель данной работы заключается в определении задержки распространения сигнала цифровых элементов в интегральных схемах (ИС) без потребности моделирования на схематическом уровне. Выявлены аналитические уравнения для вычисления задержки распространения логических элементов. Измерены задержка распространения цепочки И-НЕ с помощью аналитических уравнений и симуляции на схематическом уровне с помощью инструмента HSPICE. Сравнение результатов измерений показывает, что созданная модель обеспечивает расчет задержки распространения цифровых элементов с точностью до 90,3%. Эта модель может быть интегрирована в процесс проектирования радиационно-устойчивых ИС.

Ключевые слова: кратковременные переходные процессы, система автоматизированного проектирования (САПР), комплементарная структура металл-оксид-полупроводник (КМОП), аналитические уравнения, одиночные ионизирующие частицы, мягкие ошибки, линейная передачи энергии, задержки распространения сигнала, радиационный эффект.