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FUNCTIONAL TESTING SCENARIOS FOR EMBEDDED MEMORIES IN AUTOMOTIVE SOC

Periodic testing of embedded memory devices in modern system-on-chips (SoC) is becoming an increasingly common requirement. Automotive is one of the largest semiconductor markets with the requirement of in-filed testing of embedded memories. Hardware implementation of test algorithms in memory built-in self-test (BIST) scheme allows in-field testing only with predefined instructions which restricts flexibility of system test in mission mode. In this paper, different scenarios for memory testing in mission mode is proposed, which are controlled and configured by microcontrollers Safety Manager.

Keywords: built-in self-test, in-field test, memory test, automotive.

Introduction. At the moment, the automotive industry is one of the fastest growing sectors in semiconductors industry. The reason for such growth is the rapid technological progress and the increasing need of more power systems in automobiles. The tendency for greater safety and better driving experience is forcing automakers to continually integrate more and more Electronic Control Units (ECU) like Advanced Driver Assistance Systems (ADAS) and In-Vehicle Infotainment (IVI) into their vehicles. Some of the examples of such systems are adaptive cruise control, parking assistance, automotive emergency braking, lane change assistance, and so forth. The failure in those systems could damage the health of people, thus they have very high safety and reliability requirements.

These high demands in the automotive motivated the emergence of the ISO 26262 standard [1]. This standard defines the requirements for achieving an acceptable level of risk for electrical and/or electronic systems intended to be used in the automotive. The final product can be qualified with one of the automotive safety integrity levels (ASIL) A-D. In ISO 26262 ASIL classifications are used to express the level of risk reduction to prevent hazards. ASIL D is the highest level and ASIL A is the lowest. The ASIL level calculated for the given hazard is then assigned to the safety goal. ASIL is determined based on a combination of the probability of exposure, the possible controllability by a driver, and the possible outcome severity if a critical event occurs.

The automotive industry has a strong need for flexible and reusable test architectures, which will ensure effective and low-cost solutions for mission mode fault detection abilities in SoCs. These requirements and the need of extensive

verification due to safety-critical environments requires firmware development to happen concurrent with hardware development.

In the next section of this paper testing modes for the automotive are presented. Section 3 describes a testing strategy for automotive memories in the field. Finally, section 4 concludes the paper.

1. Testing modes for automotive. In order to have a high level of safety and reliability of automotive memories, there is a need to have robust test and repair solutions not only at the production mode but also in the field. Traditional manufacturing tests are not applicable for the field testing, so there are several solutions proposed in this regard [2,3]:

- Power-on Self-test (POST);
- Periodic testing for permanent fault detection;
- Error Correcting Codes (ECC) for transient fault detection.

1.1. Production Mode Testing. One of the conceptual requirements for an automotive is the supreme product quality, which can be assured with high yield and low DPPM criteria for the produced chips. During the manufacturing process, it is achieved with the help of efficient test and repair algorithms. There are already efficient test algorithms developed which provide full coverage for each class of faults, but they have different complexities and therefore different runtime requirements.

1.2. Power-on mode testing. Enabling the test also in the field is a specific requirement for functional safety-oriented applications. In contrast to manufacturing, in the field, the requirements to the test are more stringent due to number of area, power and time-related constraints. Therefore, several alternative solutions are proposed aimed at meeting them. One such type of an in-field test is POST. The main goal of POST is to quickly test whether all devices are properly connected and accurately function before the car is turned on and report if any problem is found. The other functionality of POST is related to the memory repair. During the manufacturing, the repair signature is stored in the eFuse array, and that information must be sent to memory at power-on. Since the POST time is short, there is a strong requirement to transfer that information faster.

1.3. Mission mode testing. Another type of the in-field test which is used in the mission mode is Periodic test. Periodic test ensures that the device has not become unsafe since the POST was performed. The Periodic self-test starts at least once per safety interval, which is defined by safety-critical devices as a period of time during which failure can occur. The first difference of POST and Periodic test is that during the Periodic test, there is no need to have a repair option. The main goal of Periodic test is to check if there is an issue in a device, and inform driver about it. The second difference is that they have different test flows.

The other type of testing used in the mission mode is the error correction code (ECC) [4,5]. The techniques discussed above targeted the testing of hard faults, nevertheless, in order to adhere safety and reliability requirements there is a need to address also the soft errors occurring in the mission mode.

2. Memory testing strategy in the mission mode. Automotive industry has a strong need for flexible and reusable test architectures, which will ensure efficient and low-cost solutions ensuring advanced fault detection capabilities for SoCs in the mission mode. The generated Firmware allows to have programmable test solutions, which should be controlled by the Safety Manager of the corresponding MCU [6]. The case study in this section demonstrates the proposed strategy of testing embedded memories in automotive SoCs during Power-on Self-test mode and Mission mode. The strategy is based on the following instructions:

1. Grouping the memories of the same cluster (e.g., memories for Audio Player, memories for Engine Control, memories for Advanced Driver Assistance Systems (ADAS), etc);
2. Selection of the test algorithm for the corresponding memory group.

Fig. 1 demonstrates the scenario of testing the embedded memories during Power-on self-test mode. It consists of the following steps:

1. Checking the safety mechanism:

- Before starting to test the embedded memories, at first, there is a need to make sure that BIST system is functioning correctly.
- For this purpose, faults are injected into the system and status bits are verified.

2. Runing Logic BIST to check the circuit logic including MBIST and ECC logic:

- This is the logical continuation of the first step, where the Logic BIST has invoked to check whether the logical components of the system are functioning correctly.

3. Repairing the memories by loading repair information from NVM:

- After the manufacturing test, those memories which had problems are repaired, and defective rows and columns are replaced with the reserved ones. This information is kept in non-volatile memory (NVM) (e.g., electrical Fuse) and should be loaded by Safety Manager whenever the car is turned on.

4. Selecting the set of test algorithms:

- Selecting the test algorithms means to detect the aging faults which happen after manufacturing.
- The selection of the group of algorithms may also depend on the time that passed after turning off the car last time.

5. Runing memory BIST for the selected group of memories with the chosen set of algorithms:

- After all these steps, the embedded memories should be tested before switching to the mission mode.

6. Initializing the selected memories with predefined data:

- In this step memories are initialized with some predefined data before entering the mission mode.

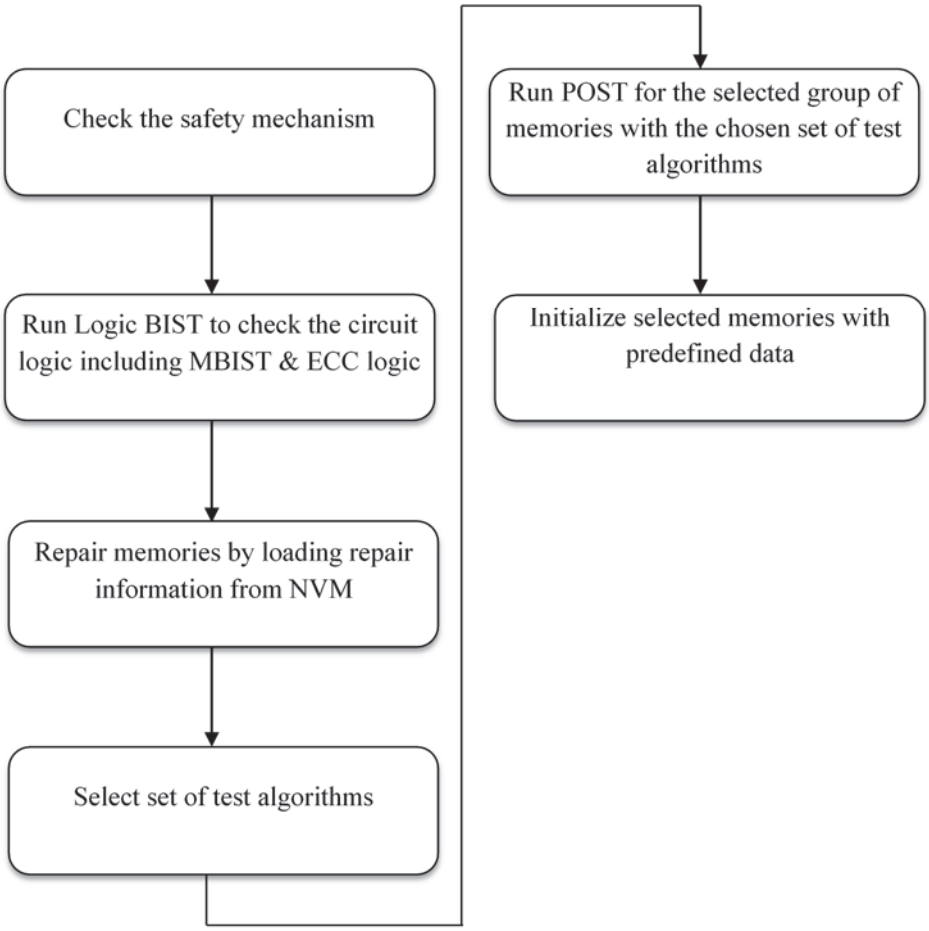

Fig. 1. A Memory testing scenario for the Power-on Self-test

Fig. 2 demonstrates the scenario of testing the embedded memories during the Mission mode. It consists of the following steps:

1. ECC for transient faults:

- Faults are classified as permanent when a device has a failure in multiple intervals. In contrast, transient faults are generating errors only in a single scrub

interval. Experiments indicate that the majority of the observed SRAM faults in the field are transient faults and they are due to single-bit faults. The transient errors and subset of permanent faults can be detected and possibly corrected by Error correcting codes (ECC).

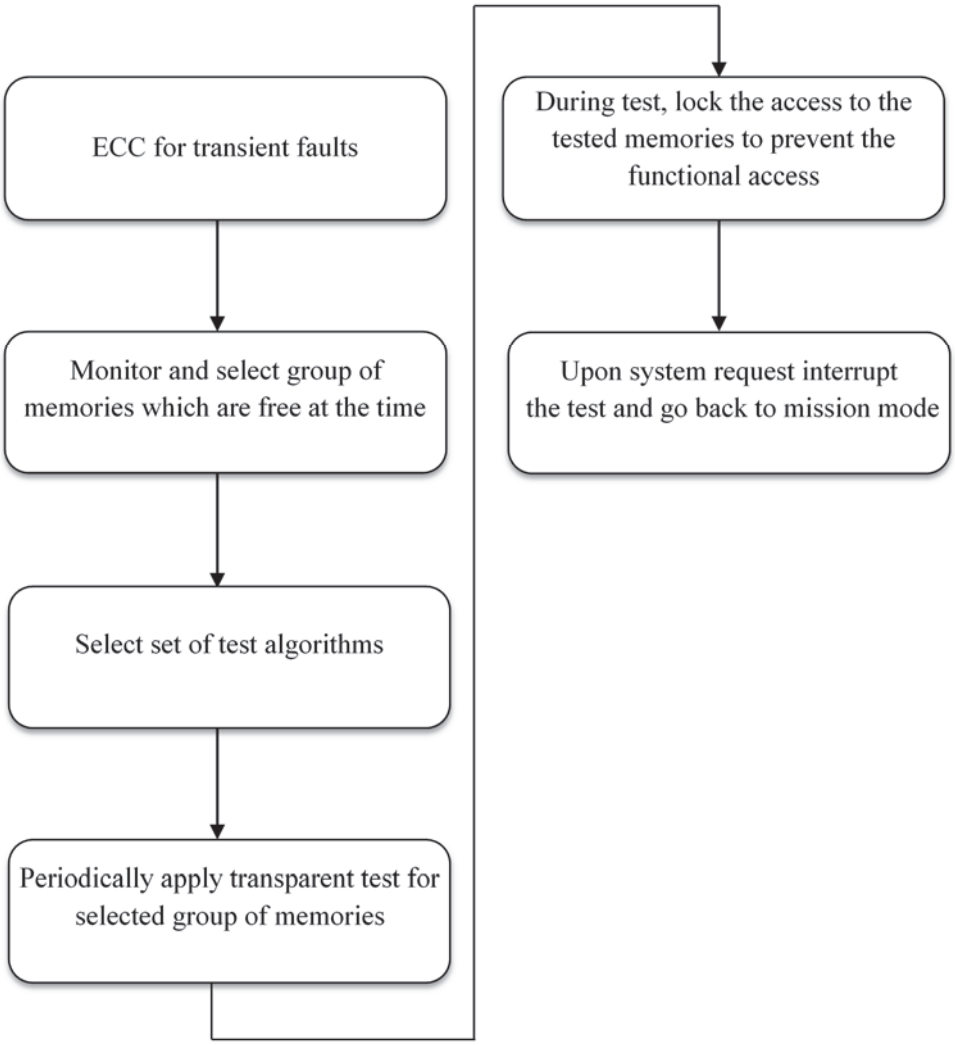

Fig. 2. A memory testing scenario for the Mission mode

2. Monitoring and selecting group of memories which are free at the time:

- During the mission mode, some groups of memories are functioning and some of them are free. Before the test starts, the group of free memories should be found.

3. Selecting the set of test algorithms:

- In this mode also, the selection of appropriate set of test algorithms may depend on different factors.

4. Periodically applying a transparent test for the selected group of memories [7,8]:

- Since memories are in the mission mode, the content should be maintained, therefore, here, a transparent test must be applied. The test is invoked periodically (e.g., 100 *ms*) with a series of short sequence of transactions or bursts.

5. During the test, lock the access to the tested memories to prevent the functional access:

- When memories are in the testing mode the access to them should be prevented in order to keep the memory content safe and have correct the test results.

6. Upon the system request, interrupt the test and go back to the mission mode:

- There may be special cases when access to the memory under the test comes by the system request. Here the test must be immediately stopped, the memory must be reverted, and access must be given to the system.

Conclusion. Meeting the requirements of the ISO 26262 standard becomes more difficult as the device complexities continue to grow. In this paper, at first, the introduction to the automotive industry with the overview of its various aspects, including safety, reliability and testability is introduced. Afterwards, the built-in test solution demands, and concepts are explained for various operating modes of vehicles including production, power-on and mission. Finally, memory testing scenarios are presented for both the Power-on Self-test mode and the Mission mode controlled by the microcontroller Safety Manager.

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Դ.Գ. ՍԱՐԳՍՅԱՆ

ՆԵՐԴՐՎԱԾ ՀԻՇՈՂ ՍԱՐՔԵՐԻ ՖՈՒՆԿՑԻՈՆԱԼ ԹԵՍՏԱՎՈՐՄԱՆ ՍՑԵՆԱՐՆԵՐ ԱՎՏՈՄՈԲԻԼԱՅԻՆ ԲՑՈՒՐԵՂՈՒՄ

Արդի բյուրեղի վրա համակարգերում ներկառուցված հիշող սարքերի պարբերական թեստավորումը դառնում է հիմնական անհրաժեշտություններից մեկը: Ավտոմոբիլային համակարգերը դարձել են կիսահաղորդիչներ օգտագործող ամենամեծ շուկաներից մեկը, որոնք պահանջում են ներդրված հիշող սարքերի թեստավորում ֆունկցիոնալ աշխատանքի ժամանակ: Ներդրված թեստավորման համակարգերում թեստային ալգորիթմների ապարատային իրականացումը թույլատրում է թեստավորում ֆունկցիոնալ աշխատանքի պահին՝ միայն նախապես ծրագրավորված հրամաններով, որը սահմանափակում է թեստավորման ճկունությունը: Հոդվածում ներկայացված են ներդրված հիշող սարքերի թեստավորման տարբեր սցենարներ ֆունկցիոնալ աշխատանքի ընթացքում, որոնք ղեկավարելու է միկրոպրոցեսորը:

Առանցքային բառեր. ներկառուցված թեստավորման համակարգ, թեստավորում ֆունկցիոնալ աշխատանքի պահին, հիշողության թեստավորում, ավտոմոբիլային համակարգեր:

Д.Г. САРКИСЯН

СЦЕНАРИИ ФУНКЦИОНАЛЬНОГО ТЕСТИРОВАНИЯ УСТРОЙСТВ ПАМЯТИ, ВСТРОЕННЫХ В СИСТЕМЫ НА КРИСТАЛЛЕ АВТОМОБИЛЬНЫХ СИСТЕМ

Периодическое тестирование устройств памяти, встроенных в современные системы на кристалле (СнК), становится все более необходимым требованием. Автомобильные системы являются одним из крупнейших рынков полупроводников с требованием тестирования встроенной памяти в реальном времени. Аппаратная реализация тестовых алгоритмов во встроенных системах самотестирования обеспечивает тестирование только с предопределенными инструкциями в функциональном режиме, что ограничивает гибкость тестирования. В статье предлагаются различные сценарии тестирования памяти в функциональном режиме, которые управляются и настраиваются микропроцессором.

Ключевые слова: встроенная система самотестирования, тестирование памяти, тестирование памяти в функциональном режиме, автомобильные системы.