ISSN 0002-306X. Proc. of the RA NAS and NPUA Ser. of tech. sc. 2019. V. LXXII, N2.

UDC 004.08:621.382.3 **MICROELECTRONICS**

V.SH. MELIKYAN, S.A. HARUTYUNYAN, K.H. SAFARYAN, M.V. BAZIKYAN

IMPLEMENTATION OF D FLIP-FLOP FOR ULTRA-LOW POWER SYSTEMS

In this article a new circuit technique to reduce the dynamic mode power of the D Flip-Flop is proposed. An enhancement over well-known Flip-Flop circuit is presented to reduce the number of transistors and hence to reduce the power consumption. The circuit is implemented and tested in SAED32nm library. An example of the circuit usage and method efficiency is provided in this paper.

Keywords: low power; dynamic power; d flip-flop; pipelining.

Introduction. Modern IC circuits require both Low-power and at the same time high-speed solutions. The performance of the circuit is always determined by timing elements such as latches and flip-flops, thus even a small improvement in the flip-flop design may have a huge impact on the design. Timing constraints and power usage are the main concerns that IC design faces nowadays. Due to the robustness and tolerance under the deterioration of operating conditions, the conventional D flip-flop (CDFF) [1] is widely used as a digital standard cell, notwithstanding the more power dissipation.

Many efforts have been made to enhance the DFF performance. A sense-amplifier based flip-flop (SAFF), which can employ reduced clock-swing techniques, is proposed for low power achievement [1]. Based on the conventional SAFF, many improved schemes have been presented in [2-6].

It is also well-known that the DFF design proposes [3] an N-C2MOS output latch to reduce the transition delay. And New SAFF is reported in [5] with better power-delay-product (PDP) performance than that of other published SAFFs, but it will cost much more.

A semi - dynamic flip-flop (SDFF) and hybrid latch flip-flop (HLFF) are known as fast flip-flops, and yet more power dissipation is induced because of the redundant node transitions [7].

Low swing clock double-edge triggered flip-flop [8] and ultra-low power flip-flops for MTCMOS circuits [9] suffer from higher process cost which limited their applications.

In this paper, a master-slave flip-flop which achieves lower power and higher speed by reducing the clock capacitance load and discharge time is proposed.

Traditional D Flip-Flop and its uses. D flip-flop (Delay/Data flip-flop) is one of the basic elements for storing information. It can store one-bit data. Flip-flops, on the other hand, have their content change only either at the rising or falling edge of the enable signal. This enable signal is usually the clock signal itself. It is used in all digital applications where it is required to hold certain data. The basic circuit of D Flip-Flop is presented in Fig 1.

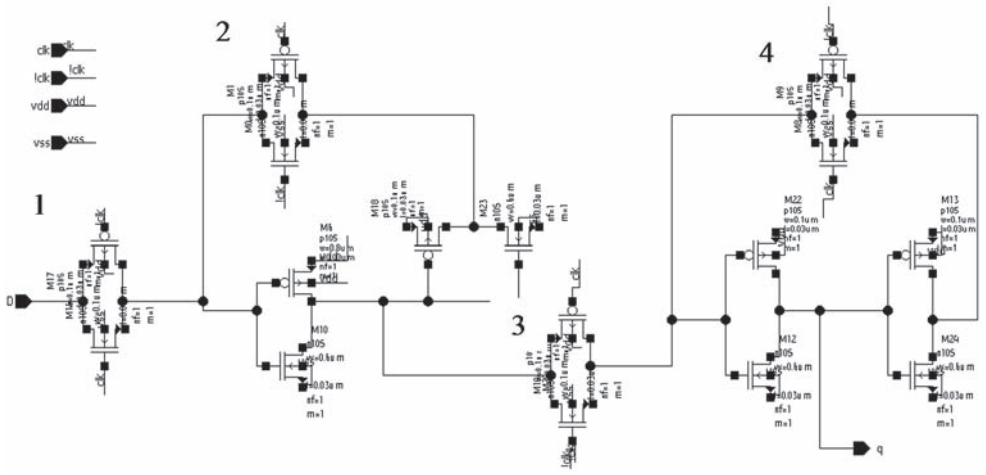

Fig. 1. Traditional CMOS DFF

The circuit has 4 Transmission Gates and 4 Inverters. Transmission Gates are required to make the master slave logic possible. They operate in a way that the entire logic of the circuit is divided into two parts and one of them is always “closed”. Two stages are Sample and Hold.

In Fig 1, TG gates 1 and 3 operate with the same clock edges while 2 and 4 operate with an opposite edge. Let’s assume that the clock signal has logic 1, in that case TG gates 1 and 3 are open and data are pulled into the circuit. When the clock triggers, TG gates also Trigger, resulting in closing the TG 1 and 3 and opening the 2 and 4 TGs. This kind of architecture is used to the prevent the metastable value from passing through the flop to the output of the circuit. This is a traditional CMOS trigger circuit. The circuit also provides the inverse of the actual output signal named QN, but in some applications it is not used remaining as a floating port. That is the exploit that the proposed circuit is taking advantage of.

Two inverters inside the single stage of DFF are used as a memory cell. It is also used to provide both straight and inversed outputs in the output stage. But as mentioned above, output is not always used. The inverter uses both PMOS and NMOS transistors to make sure that the output swing is the biggest possible. Sometimes that is not required.

The proposed circuit is built, considering that internal signals may have a lower voltage than outputs. NMOS transistors of the 2nd inverters have been removed in the proposed circuit. That does not have an impact on the cell functionality. Doing this has a disadvantage that the inversed output of the circuit losses in full swing and has a swing of V_{dd} to V_{dd}-V_{th}. In the path of those signals there are full inverters which fix the swing decrement issue. Hence, it does not affect the circuit functionality. The proposed circuit is shown in Fig 2.

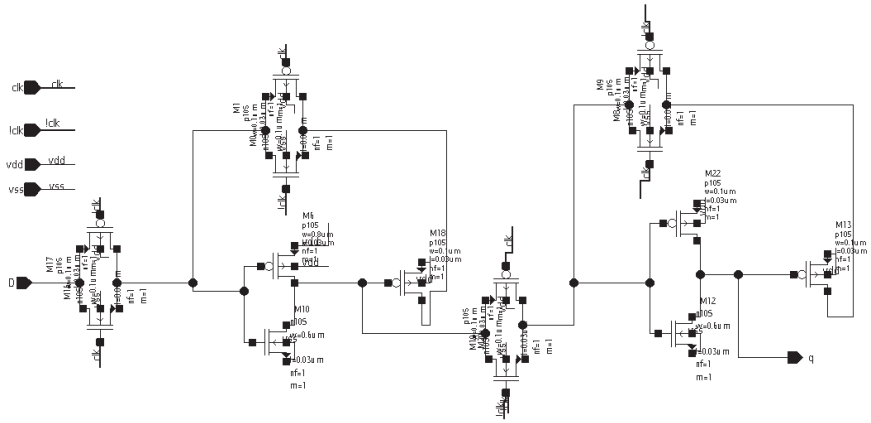

Fig. 2. Proposed DFF circuit

The digital design is carried out by Electronic design automation (EDA) tools. Hence there is no control over what kind of cells the tools will use to create the logic, that is why, libraries include many cells of the same cell. DFF has many variations, including DFFs with only a straight output. The proposed circuit may be used as a low power version of such a cell.

Another application that single output DFFs are used in is Pipelining. Pipelining is a well-known method to fix timing violations. The idea of Pipelining is to split the combo logic into two parts. Put off the correct output by one cycle but make the circuit operate at a higher frequency. Fig. 3 illustrates the idea of Pipelining.

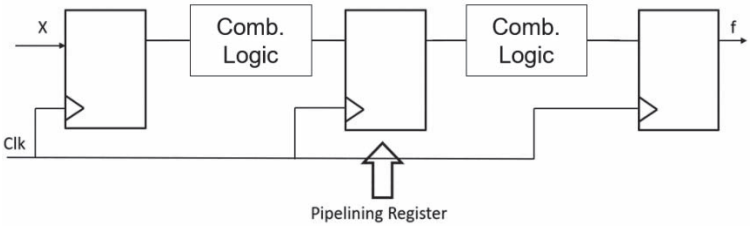

Fig. 3. Pipelining picture

Measurement Results. The DFF circuit has been simulated with SAED 32 nm technology using Hspice[11]. The results of the simulation for traditional and proposed DFFs are illustrated in Fig. 4 and Fig. 5.

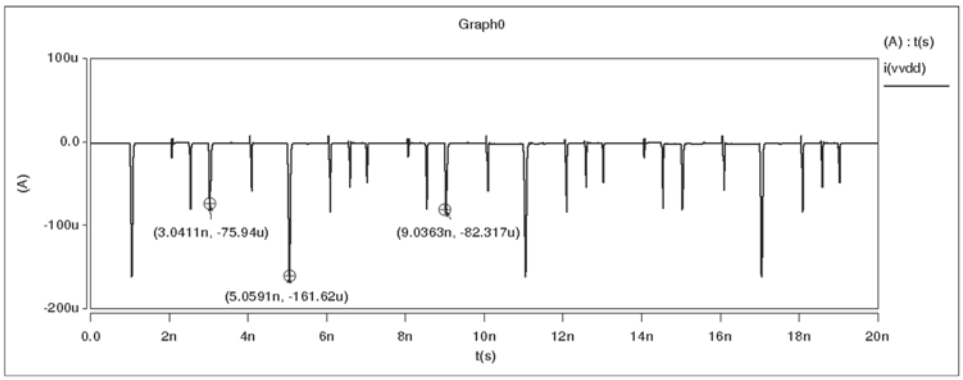

Fig. 4. Simulation Results of the Traditional DFF

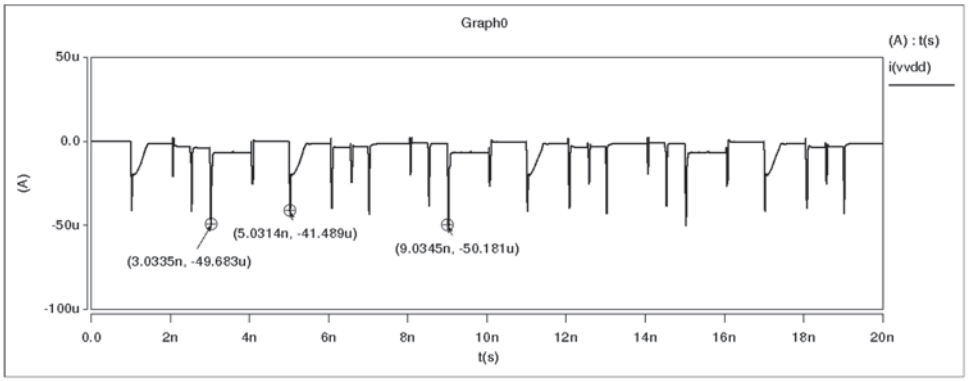

Fig. 5. Simulation Results of Proposed DFF

To test the circuit efficiency in Pipelining, an 8-bit logic has been designed. Although there are no cells between the flops, this illustrates the real pipelining technique that is used in production. It is shown in Fig. 6.

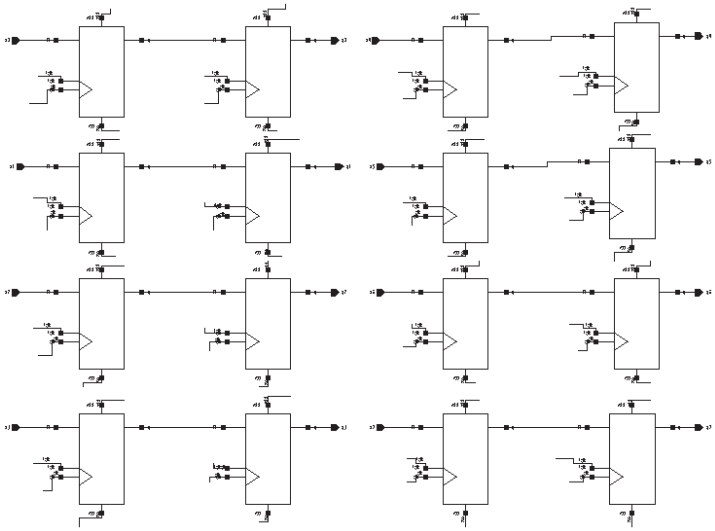

Fig. 6. 8-bit Register Pipelined by 1 stage

The simulation result for the Pipeline circuit with Traditional DFF and the Proposed one are shown in Fig. 7 and Fig. 8.

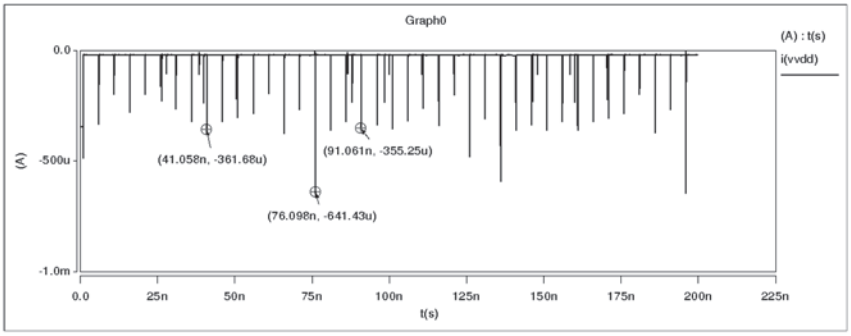

Fig. 7. Simulation Results of the Pipeline circuit with the Traditional DFF

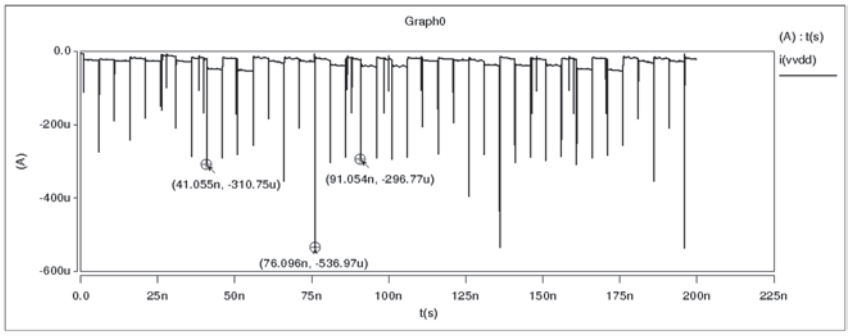

Fig. 8. Simulation Results of the Pipeline circuit with the Proposed DFF

A final comparison has been made between the proposed circuit and the traditional DFF in the face of the area and power parameters. It is shown in the table.

Table

Comparison of the Proposed circuit and the traditional DFF

	Traditional (*uW*)	Proposed (*uW*)
D flip Flop	161,62	41,489
8-bit bus Pipelined 1 stage	641,43	489,79

Conclusion. An improved DFF circuit has been presented. The number of components in the circuit is decreased, resulting in lower power consumption. The circuit has been tested separately both in a real-world application and in cases of the proposed circuit. The proposed circuit had an advantage in power consumption. The disadvantage of the design is that it limits the cells' functionality to only single output type, or the implementer should take care of fixing the voltage value of the Inversed output before usage. As a result of such implementation, power consumption has been reduced by up to 20%. This circuit may be used in other DFF heavy applications.

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National Polytechnic University of Armenia. Material is received 11.04.2019.

Վ.Շ. ՄԵԼԻՔՅԱՆ, Ս.Ա. ՀԱՐՈՒԹՅՈՒՆՅԱՆ, Կ.Հ. ՍԱՖԱՐՅԱՆ, Մ.Վ. ԲԱԶԻԿՅԱՆ

ԳԵՐՑԱԾՐ ՀԶՈՐՈՒԹՅԱՄԲ ՀԱՄԱԿԱՐԳԵՐՈՒՄ D ՏՐԻԳԵՐԻ ՄՇԱԿՈՒՄԸ

Առաջարկվում է նոր սխեմատիկ մեթոդ՝ D տրիգերի դինամիկ ռեժիմում ծախսած հզորության նվազարկման համար։ Հայտնի D տրիգերի սխեմայի բարելավումը թույլ է տալիս նվազեցնել տրանզիստրների քանակը, արդյունքում՝ նաև հզորության ծախսը։ Սխեման մշակված և ստուգված է ՍԱՈՒԴ 32 *նմ* տեխնոլոգիայով։ Հոդվածում ներկայացված է նաև սխեմայի կիրառման և մեթոդի արդյունավետության օրինակ։

Առանցքային բառեր. ցածր էներգասպառում, դինամիկ հզորություն, D տրիգեր, կոնվեյեր։

В.Ш. МЕЛИКЯН, С.А. АРУТЮНЯН, К.Г. САФАРЯН, М.В. БАЗИКЯН

РАЗРАБОТКА Д ТРИГГЕРА ДЛЯ СИСТЕМ СО СВЕРХНИЗКИМ ЭНЕРГОПОТРЕБЛЕНИЕМ

Предложена новая схема для снижения мощности динамического режима D триггера. Улучшение известной схемы D триггера позволяет сократить количество транзисторов и, следовательно, снизить используемую мощность. Схема реализована и протестирована с использованием библиотеки SAED 32 *нм*. В статье также представлен пример использования схемы и показана эффективность метода.

Ключевые слова: низкая мощность, динамическая мощность, D триггер, конвейеризация.