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THE OUTPUT NOISE REDUCTION OF A FLASH ANALOG-DIGITAL CONVERTER

A new approach to reducing output noises in the Flash analog-digital converter (ADC) is presented. A type of ADC with the least amount of noise is Flash ADC, but it also needs to have noises as less as possible. By using this method in 32nm technology, the area of the circuit increases by 72% and the noise error decreases by 63%. This method is very preferable to use for high bit Flesh ADC circuits, as the latter have many logic cells in the Encoder. Switching inputs of those cells leads to high noises in the output.

Keywords: ADC, comparator, encoder, current mirror.

Introduction. ADC is a system that converts an analog signal, such as a sound picked up by a microphone or light entering a digital camera, into a digital signal. Typically, the digital output is a two complement binary number that is proportional to the input. The performance of an ADC is primarily characterized by its bandwidth and signal-to-noise ratio (SNR). The bandwidth of an ADC is characterized primarily by its sampling rate. Analog to digital conversion is shown in Fig.1.

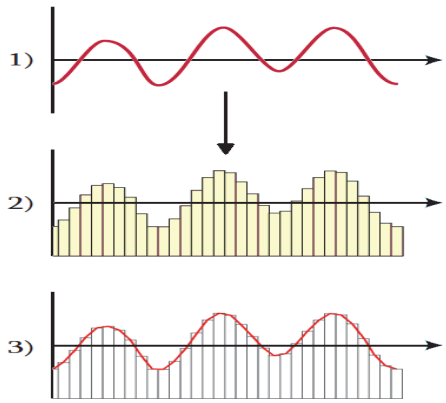

Fig.1. Conversion of analog signal to digital (1 - analog signal, 2 - digital signal, 3 - combination of analog and digital signals)

While analogue signals can be continuous and provide an infinite number of different voltage values, digital circuits on the other hand, work with a binary signal

which has only two discrete states, a logic “1” (HIGH) or a logic “0” (LOW). So it is necessary to have an electronic circuit which can convert between the two different domains of continuously changing analogue signals and discrete digital signals, and this is where Analogue-to-Digital Converters (A/D) come in.

Literature review. There are several methods for reducing noises in the output of ADC. There are global methods and also methods for specific ADC circuits. For example, in [1] the presented method reduces the input noises by digital averaging. It is done using two measurements or even 16, as soon as enough noise is added to the input signal. The more noise present at the input, the more averaging is required to achieve the same result.

In [2], a method bringing out the contributing factors to noise is used. It suggests techniques to minimize the noise in an ADC circuit and presents the salient parameters of a working high speed ADC circuit incorporating techniques. For a given ADC, theoretically, a given signal to the noise ratio (SNR) and the dynamic range can be realised.

In [3], three types of noise filtering are presented. They are analog, digital and both. White noise underneath a strong enough signal can be averaged out by oversampling, moving averages or other techniques, while taking advantage of statistical randomness. Spurious signals in the bandwidth of the signal of interest need to be resolved close to their source; otherwise, an A/D converter just digitizes and mixes them with the signal of interest. Harmonics can be dampened by filtering an A/D converter, undoing some of the effects of nonlinearity.

In [4], advantages and disadvantages of noise filtering are presented. Converting analog sensor signals to the digital domain is a standard practice with wearable patient monitoring equipment. However, designers must be aware that these applications depend on a system that produces reliable, repeatable results, albeit in their noisy environments. Noise filtering techniques are a critical portion of the solution circuit.

In [5], a noise reducing device that includes an acoustic-to-electric conversion section for collecting noise and outputting an analog noise signal; an analog-to-digital conversion section for converting the analog noise signal into a digital noise signal; a digital processing section for generating a digital noise reducing signal on a basis of the digital noise signal and a desired parameter is presented.

In [6], an effective way to remove noise is by using a low-pass (anti-aliasing) filter prior to the ADC is introduced. Including by-pass capacitors and using a ground plane will also eliminate this type of noise. A third source of noise is the radiated noise. The major sources of this type of noise are Electromagnetic Interference (EMI) or capacitive coupling of signals from trace-to-trace.

In [7], three types of noise reduction in ADC are presented. The first is a lower-noise reference. One of the most obvious ways to reduce the level of reference noise entering a system is to choose a voltage reference with less noise. The second is increasing the reference voltage. Another method to potentially reduce the effects of reference noise is to increase the reference voltage, as this affects the change in the percent of utilization. For example, doubling the reference voltage decreases the percent of utilization by a factor of 2. The third is reducing the system ENBW. The third option to reduce the amount of reference noise passed into the system is to limit the overall ENBW. One way to limit ENBW is by reducing the antialiasing, or the reference filter cutoff frequencies.

The proposed Flash-ADC. Flash ADC is the simplest type of ADCs and it has the lowest noises compared with other ADCs, but the more inputs and outputs it has, the bigger noises it has got in the outputs, because there are many switching cells in the circuit with an input voltage change. For example, in a *256-bit* Flash ADC, the output noises can be very big, because at the main input voltage change, there are many cells, whose inputs will be changed at the same time and it will lead to big noises in the output. So, here, a new of optimized Flash ADC is developed, which will have small noises at the output in case of any high bit circuit. Experiments are carried out on a *2-bit* Flash ADC. The primary circuit of the Flash ADC is shown in Fig.2.

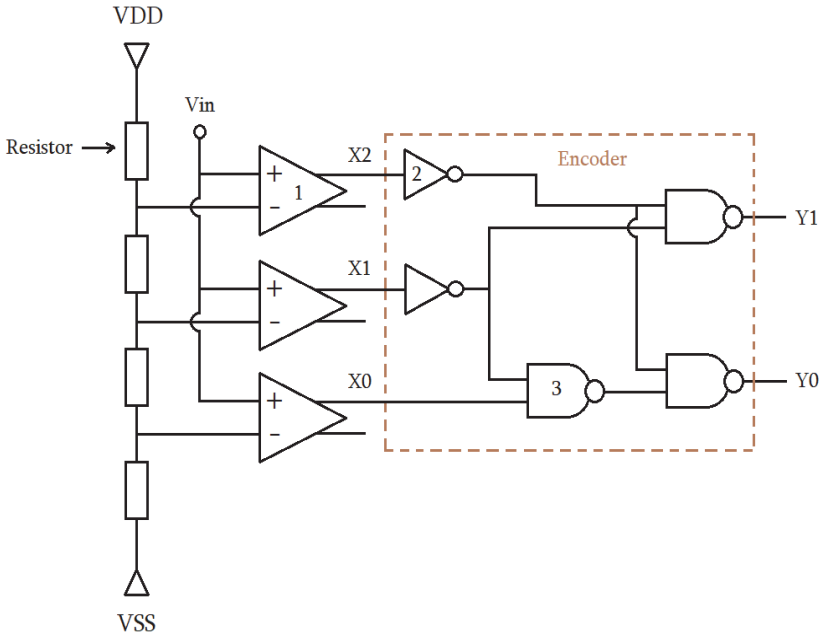

Fig.2. Primary Flash ADC (1 - comparator, 2 - invertor, 3 - NAND)

In the primary circuit, the table of X0, X1, X2, Y0 and Y1 nodes have the form like that in Table 1.

Table 1

The dependency of Y1 and Y2 outputs from X0, X1 and X2

X0	X1	X2	Y0	Y1
0	0	0	0	0
1	0	0	1	0
X	1	0	0	1
X	x	1	1	1

So, the node from X0, X1 and X2 nodes is the last node with high voltage, it will determine the voltages of Y0 and Y1 output nodes.

When Vin increases the table of X0, X1, X2, Y0 and Y1 nodes have the form like that in Table 2.

Table 2

The voltage values of Y1 and Y2 outputs and X0, X1, X2 nodes when Vin increases from 0 to VDD in the primary Flash ADC

X0	X1	X2	Y0	Y1
0	0	0	0	0
1	0	0	1	0
1	1	0	0	1
1	1	1	1	1

In case of a very fast increase of Vin (when X0,X1,X2 will at once change from 000 to 111, or from 001 to 110) there will be many switching nodes in the Encoder part of an ADC and it will lead to big noises in the outputs. To solve this problem, we use the fact that the voltage of output nodes depends on the last input node with a high voltage, and we change the circuit so that only that node has a high voltage in case of the same Vin voltage value. For an optimized circuit, the Table for X0, X1, X2, Y0 and Y1 must be like that in Table 3.

Table 3

The voltage values of Y1 and Y2 outputs and X0, X1, X2 nodes when Vin increases from 0 to VDD in an optimized Flash ADC

X0	X1	X2	Y0	Y1
0	0	0	0	0
1	0	0	1	0
0	1	0	0	1
0	0	1	1	1

The Flash ADC that is appropriate to the Table 3 is shown in Fig.3.

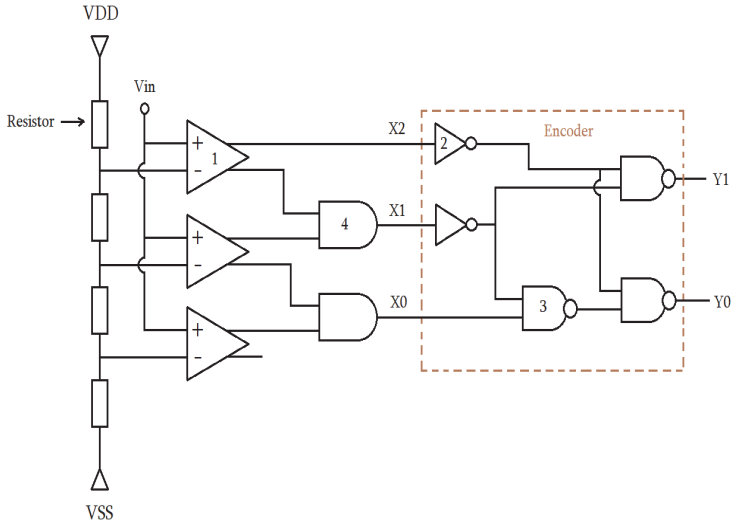

Fig.3. The Flash ADC with much less output noise than the primary circuit (1 - comparator, 2 - invertor, 3 – NAND, 4 - AND)

This is better than the primary Flash ADC, but at every change of the input voltage, one node from X0, X1 and X2, which has a high value, gets 0 value, and one node with 0 voltage gets high voltage. So the encoder in the main cases has two switching inputs which switch at the same time, which also can be dangerous for the accuracy of the outputs. To have the minimum noises in the outputs it is preferable to keep the switch of the node with high voltage a bit later. It means that when one of the nodes changes to 1 from 0, the node that had 1 value before that must change to 0 a bit later (Fig.4).

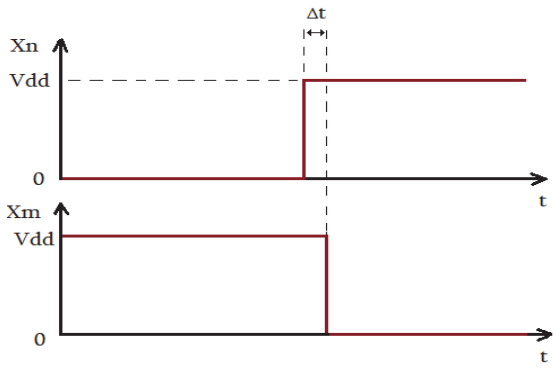

Fig.4. Switching two inputs of the Encoder in an optimized Flash ADC (Δt – is a very short period of time)

The optimized ADC contains two Flash ADC circuits (only comparator parts, the Encoder is general). The input of one Flash ADC is the general input of the circuit, and the input of the second Flash ADC is connected with the first input by transmission gate. When Vin changes very fast and with a high range, the transmission gate will keep the primary value of Vin for the second Flash ADC and it will also keep the high value of one of the Encoders input nodes in the period of the Vin change. It is the same node that has a high value before the Vin change. When another input of the Encoder also gets a high value, two inputs with high voltages will make the transmission gate to become opened. Then the old input node with a high value will become 0, and the input node that gets higher by the change of Vin will keep its value until the next Vin change.

The second transmission gate that is connected in parallel to the first is used in case when Vin changes from 0 to a higher voltage, or from higher voltage to 0. When Vin is 0, the second transmission gate is opened and the input of the second Flash ADC follows the first input until the first input of the Encoder changes to 1.

The optimized Flash ADC is shown in Fig.5.

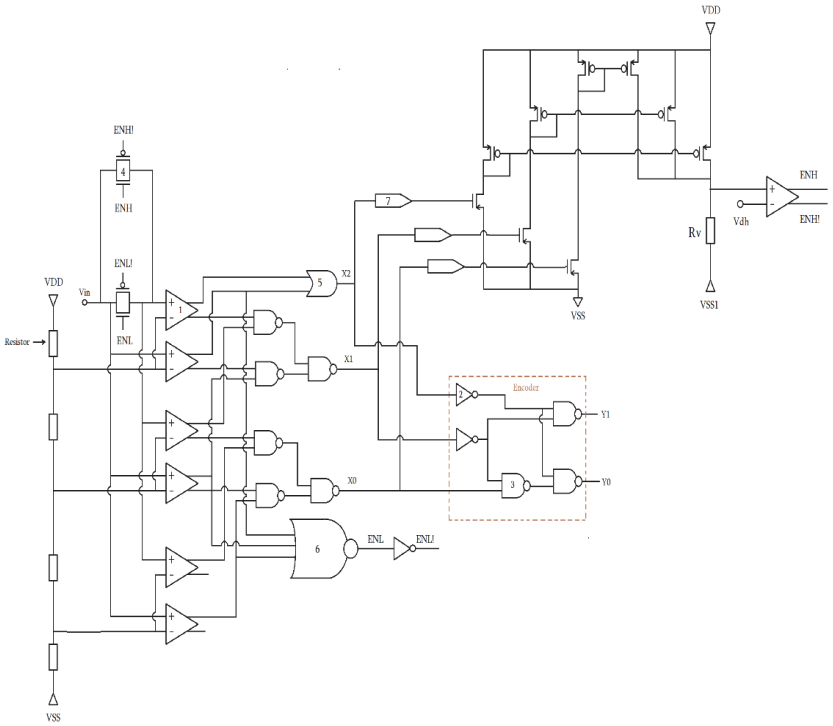

Fig.5. The circuit of the optimized Flash ADC (1 – comparator, 2 – invertor, 3 – NAND, 4 – transmission gate, 5 – OR, 6 – NOR, 7 – Level shifter)

When only one input of the Encoder has 1 value, the voltage on Rv resistor that formed with current mirrors is not so high to keep high voltage on the ENH output of the comparator. So, the first transmission gate is off. When Vin changes, the first transmission gate that is off, keeps the old value of the general input on the input of the second Flash ADC, which keeps the value of the input of Encoder which has a high voltage at that moment.

When two inputs of the Encoder have 1 value, the voltage on Rv becomes so high that the voltage of the ENH output node becomes high and the first transmission gate is on and the input of the second Flesh ADC follows the first.

The inputs of Encoders are connected to the level shifters which change the VDD voltage of the node to a bit lower voltage. This is used not to have a big current in the current mirrors.

The second transmission gate is connected to a NOR whose inputs are the outputs of the comparators of the first Flash ADC. When all outputs of comparators are 0, the transmission gate is on. This is in the case when the voltage of the general input is very low.

The disadvantage of this approach is making the area of the circuit much bigger, but for very high bit Flash ADCs this method is very useful to avoid output noises, because in the case of a fast input change with a high voltage range, the switching nodes in the Encoder will be as low as possible.

Simulation results. The main block of a Flash ADC is designed. Simulations are performed using the HSPICE simulator (described in [8]) for a number of PVT corners including 3 main conditions (TT, FF and SS processes with respective voltage and temperature values). Here the results of the TT typical corner are presented. The circuit is designed and simulation is performed in the 32 *nm* technology. The simulation results of the primary Flash ADC are shown in Fig.6 with input and output characteristics. Supply voltage is $2.5V$ and Vin changes from $1V$ to $2V$. Y0 is $2.5V$, and in the change period of Vin, it gets noises, and Y1 changes from 0 to 2.5V.

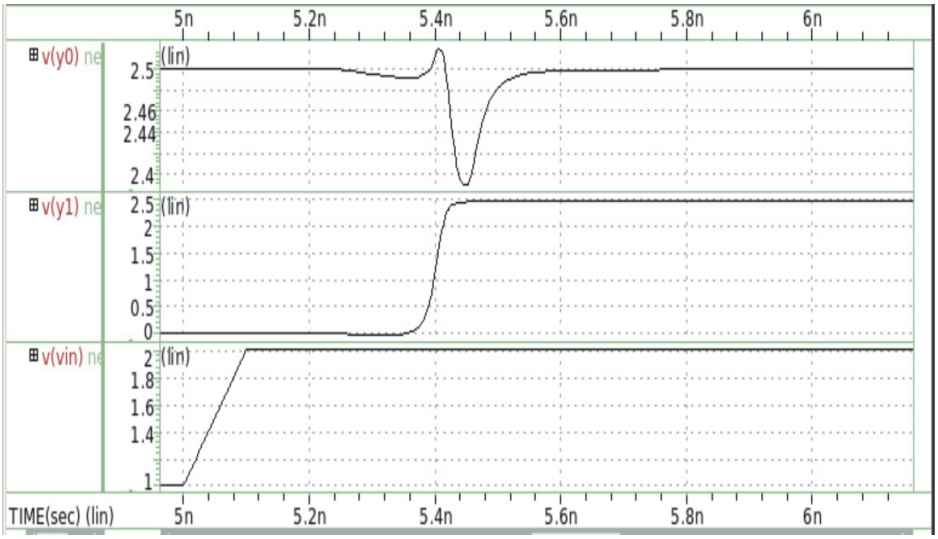

Fig.6. Simulation results of the primary Flash ADC (Vin – input, Y0 and Y1 outputs)

Simulation results of the optimized Flash ADC are shown in Fig.7. In the picture we can see that the voltage noise range of the Y0 output became lower by 63% than in the primary Flash ADC.

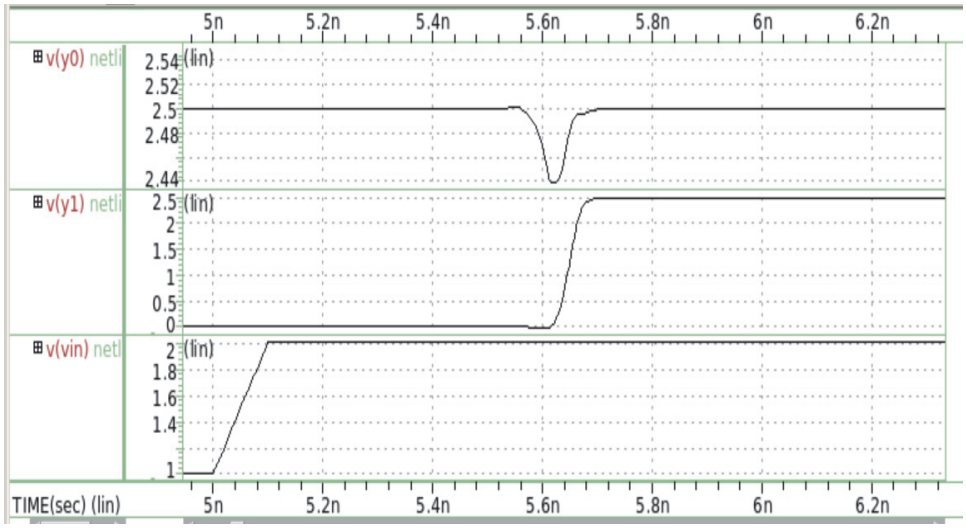

Fig.7. Simulation results of the optimized Flash ADC

The circuit of the primary Flash ADC designed in 32 *nm* technology is shown in Fig.8.

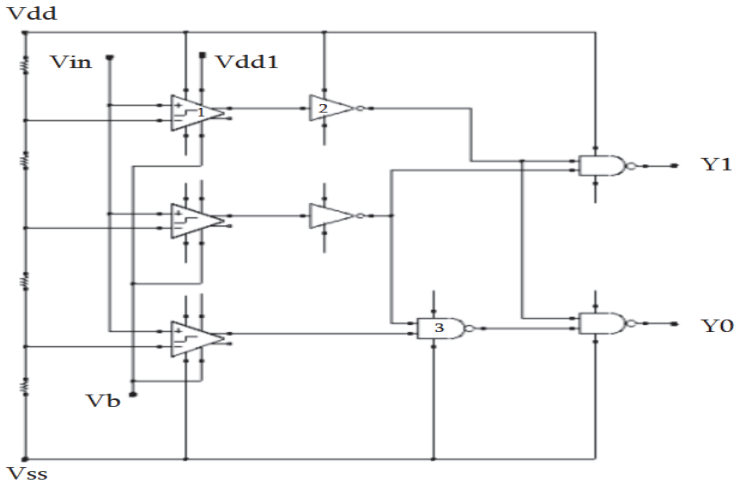

Fig.8. The circuit of the primary Flash ADC designed in the 32 nm technology (1 – comparator, 2 – invertor, 3 – NAND)

The circuit of the optimized Flash ADC designed in the 32 *nm* technology is shown in Fig.9.

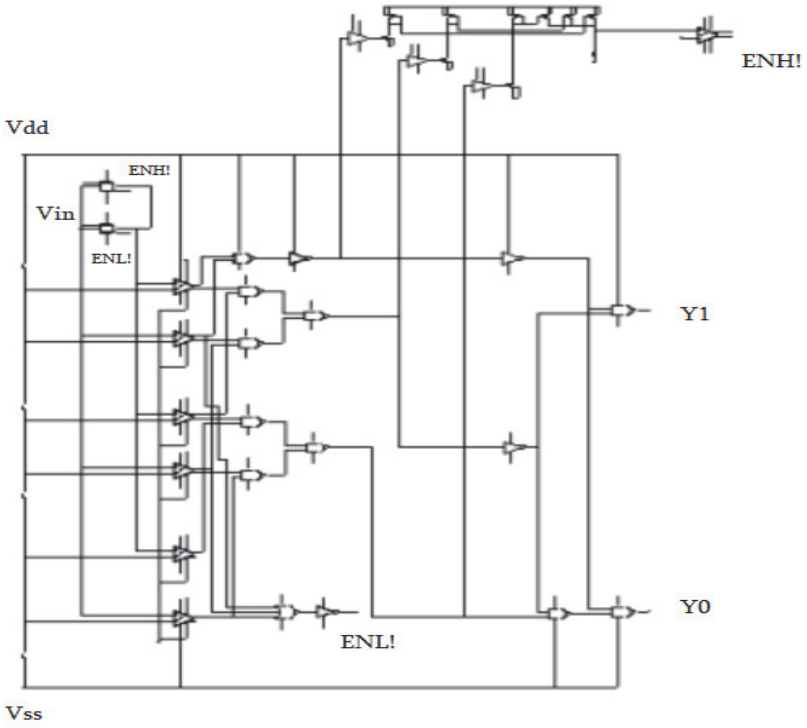

Fig.9. The circuit of the optimized Flash ADC designed in the 32 nm technology

Conclusion. A new method for noise reduction of the Flash ADC is presented. The ADC circuit which has the least noises in the outputs from all types of ADC circuits is the Flash ADC, but in case of high bit circuits, it also has big noises in the outputs. This new method requires an increase in the area, but the higher the bit of the Flash ADC, the method will be more useful for the accuracy of the output signals. In case of a high bit Flash ADCs, by using this method, the percent of the area increase will be less and the accuracy of the output signals will become much higher. In the *2-bit* Flash ADC designed in the 32 *nm* technology, the area of the circuit is increased by 72%, and the noises in the output decreased by 63%. For the design of the new circuit, other comparators, level shifters, current mirrors and transmission gates are used. As we see, even, in case of a *2-bit* Flash ADC, the method works effectively.

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National Polytechnic University of Armenia. The material is received on 11.07.2022.

Հ.Ա. ԲԱԲԱՋԱՆՅԱՆ

ԵԼՔԱՅԻՆ ԱՂՄՈՒԿՆԵՐԻ ՆՎԱԶԵՑՈՒՄԸ ՈՒՂԻՂ ՓՈԽԱՐԿՄԱՆ ԱՆԱԼՈԳԱԹՎԱՅԻՆ ՓՈԽԱՐԿԻՉՈՒՄ

Ներկայացված է ուղիղ փոխարկման անալոգային-թվային փոխարկիչում (ԱԹՓ) ելքային աղմուկների նվազեցման նոր մոտեցում: Ամենաքիչ ելքային աղմուկներ ունեցող ԱԹՓ-ի տեսակը ուղիղ փոխարկման ԱԹՓ-ն է, բայց այն նույնպես կարիք ունի՝ ունենալու հնարավորինս քիչ ելքային աղմուկներ: Օգտագործելով այս մեթոդը 32 նանոմետր տեխնոլոգիայում, սխեմայի մակերեսը մեծանում է 72%-ով, իսկ ելքային աղմուկները նվազում են 63%-ով: Այս մեթոդը շատ նախընտրելի է օգտագործել բարձր բիթային ուղիղ փոխարկման ԱԹՓ-ներում, քանի որ դրանք ունեն մեծ քանակով տրամաբանական բջիջներ կոդավորիչի սխեմայում: Այդ բջիջների փոխանջատվող մուտքերը հանգեցնում են ելքային բարձր աղմուկների:

Առանցքային բառեր. անալոգաթվային փոխակերպիչ, կոմպարատոր, կոդավորիչ, հոսանքի հայելի:

А.А. БАБАДЖАНЯН

МИНИМИЗАЦИЯ ВЫХОДНЫХ ШУМОВ АНАЛОГО-ЦИФРОВОГО ПРЕОБРАЗОВАТЕЛЯ ПРЯМОГО ПРЕОБРАЗОВАНИЯ

Представлен новый метод уменьшения выходных шумов аналого-цифрового преобразователя (АЦП) прямого преобразования. Типом АЦП, имеющего наименьшую величину выходных шумов, является АЦП прямого преобразования, но выходные шумы у него тоже должны быть как можно меньше. Используя метод в 32 *нм* технологии, площадь схемы повышается на 72%, а выходные шумы уменьшаются на 63%. Метод предпочтительнее использовать в высокобитных АЦП прямого преобразования, поскольку они имеют в энкодере логические ячейки в больших количествах. Переключающиеся входы этих ячеек приводят к большим выходным шумам.

Ключевые слова: аналого-цифровой преобразователь, компаратор, энкодер, зеркало тока.