

Z.M. AVETISYAN

MEASUREMENT, CALCULATION AND ANALYSIS OF MTBF FOR
SINGLE-STAGE SYNCHRONIZERS USING AN AUTOMATED SYSTEM

Nowadays, in the systems with very large scale of integration (VLSI), multi-clock domains are widely used to provide high correspondence of cooperation for different blocks in the systems on chip (SoC). Synchronization of the data relationship of the mentioned blocks is necessary while using multi-clock domains. To solve this synchronization problem, special circuits, called synchronizers, are used. As the data arrival time cannot be predictable between different clock domains, there is a probability of having metastable states in synchronizers. Metastability can bring a failure of consequent circuits which can bring to a failure of the whole system. Therefore, during the design and verification of an integrated circuit (IC), it is very important to estimate the probability of failures (the mean time between the failures).

In the scope of this paper, measurement of the metastability parameters and calculation systems of MTBF are researched. To reduce the design verification resources, an automated system is proposed which measures and calculates the mentioned parameters and gives a chance to analyze the circuit.

Keywords: mean time between the failures, multi-clock SoC, synchronizer, timing parameters, measurement, automated system.

Introduction. The necessity of synchronizers arises in multi-clock domain systems on chip (SoC). A simple example of a synchronizer is two series connected D flip-flops [1]. Since separate blocks in SoC work independently of each other, it is impossible to predict the arrival time of the data coming from another clock domain block. Therefore, data can be changed parallel to the synchronization clock in the synchronizer (placed in the data receiving block), which can bring a metastability in synchronizers (Fig.1).

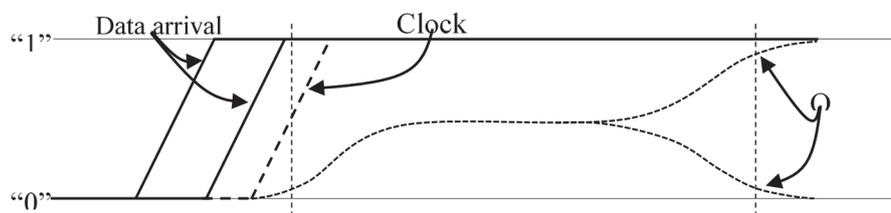


Fig.1. Metastability in a D flip-flop

If the data and the clock rising edges are close enough, it may bring to a metastability issue (Fig.1). During the metastable state output, signal Q stays between the logical levels “0” and “1”.

The process of metastability is a probable phenomenon. The mean time between failures (MTBF) is defined to highlight the synchronizer’s performance. It is based on mathematical equations, using some technology and semitechnical parameters, which are described in the next the sections.

Measurement of Setup and Hold timing parameters. To ensure the normal operation of a flip-flop without failures it is necessary to meet the setup/hold timing constraints. If that constraints are not met, the flip-flop can enter the metastable state or transfer wrong data.

To write data into the D flip-flop, the circuit needs some time before the active edge of the synchronization clock for settling (setup). This timing constraint is called setup time [2] (Fig.2). To measure the setup time, the data signal should be swept towards the clock signal up to the output distortion.

Another important question should be considered as well: how long does the input data signal need to be held unchanged after the active edge of the clock signal to ensure the data transmission without failures. That timing constraint is called hold time [2] and is defined as a minimum time which must be held after the clock active edge until the data input signal changes (Fig.2).

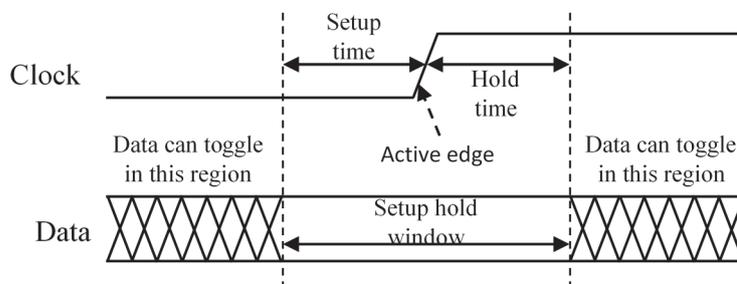


Fig.2. Setup/hold time

Measurement of the timing the constant (tau) parameter. One of the important parameters of metastability is the timing constant (tau, τ) of the metastability curve. τ depends on the physical parameters of the device, which describes how fast a device exits from the metastable state. τ is determined by equation (1) [3] (Fig.3):

$$\tau = (t_2 - t_1) / \ln \left(\frac{\Delta V_2}{\Delta V_1} \right) \quad (1)$$

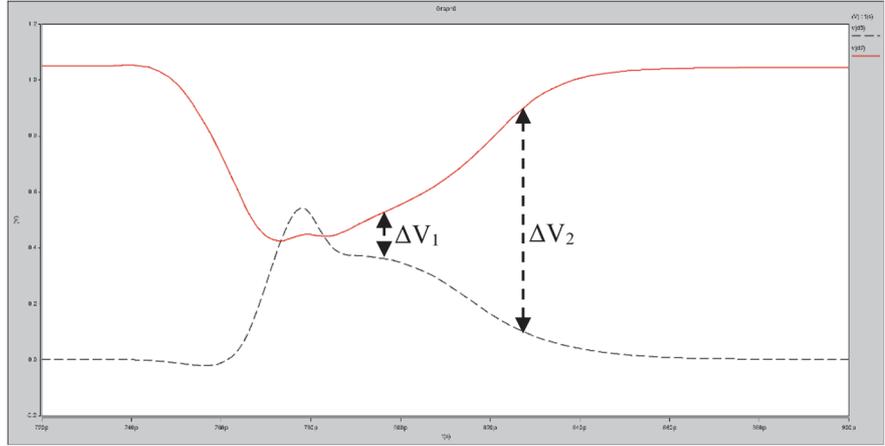


Fig.3. Modeling of the τ calculation

Calculation of the mean time between the failures. Several methods of failure probability calculation for synchronizers are presented in literature [4-6]. The mentioned probability can be calculated as [6]:

$$P_F = \frac{T_w e^{-T_s/\tau}}{T_C} , \quad (2)$$

where T_w is the time window constant, T_s is the settling time, T_C is the clock period of the synchronizer. The settling time and timing window constant can be calculated as (equations (3) and (4) respectively):

$$T_s = T_{CLK} - T_{C2Q} - T_{SU} , \quad (3)$$

$$T_w = T_{SU} + T_{HO} . \quad (4)$$

If the input data of the synchronizer toggles by a T_D period, the probability of the synchronizer failure can be calculated as

$$P_{F/sec} = \frac{T_w e^{-T_s/\tau}}{T_C T_D} . \quad (5)$$

The MTBF can be calculated from (5):

$$MTBF = \frac{T_C T_D e^{T_s/\tau}}{T_w} . \quad (6)$$

Equation (6) represents the mean time between the failures for a single latch.

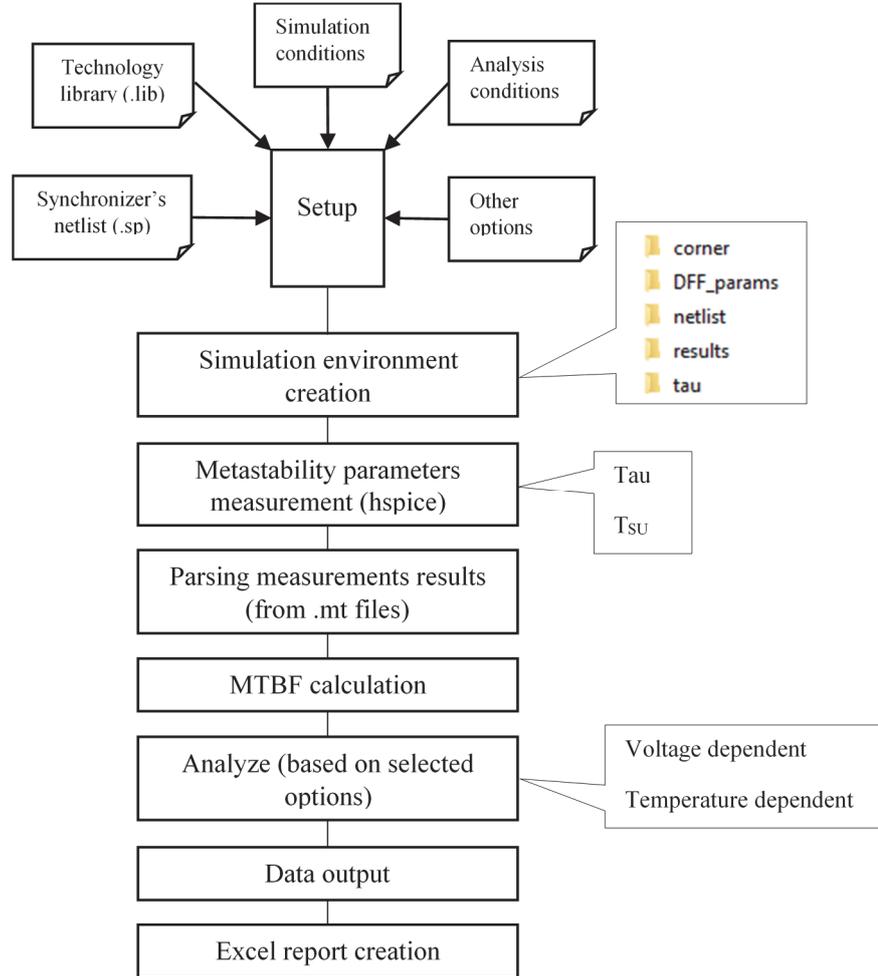


Fig.5. The block-diagram of the proposed automation system

As the minimum MTBF value is often mentioned in the design specification, which must be met during the IC design. The proposed system calculates the minimum count of latches, which are required to meet the design specification. MTBF for cascaded latches can be calculated as [6]:

$$MTBF \approx T_C T_D \left(\prod_{j=1}^{n-1} \frac{\tau_j e^{\sum_{i=1}^n T_i^S / \tau_i}}{T_j^W} \right) \left(\frac{e^{\sum_{i=1}^n T_i^S / \tau_i}}{T_n^W} \right), \quad (7)$$

where N is the number of latches.

N, calculated from equation (7), is the desirable count of latches. As the system suggests the number of latches based on a single latch character, all the

latches in the proposed circuit will have the same parameters (τ , T_s , T_w). Therefore (7) can be modified as follows:

$$\begin{aligned} \text{MTBF} &\approx T_C T_D \left(\frac{\tau e^{NT_s/\tau}}{T_w} \right)^{N-1} \frac{e^{NT_s/\tau}}{T_w} = \\ &= T_C T_D \tau^{N-1} \left(\frac{e^{NT_s/\tau}}{T_w} \right)^{N-1} \frac{e^{NT_s/\tau}}{T_w} = \frac{T_C T_D}{\tau} \tau^N \left(\frac{e^{NT_s/\tau}}{T_w} \right)^N = \frac{T_C T_D}{\tau} \left(\frac{\tau e^{NT_s/\tau}}{T_w} \right)^N, \end{aligned} \quad (8)$$

$$\left(\frac{\tau e^{NT_s/\tau}}{T_w} \right)^N = \frac{\text{MTBF} \cdot \tau}{T_C T_D}. \quad (9)$$

To determine N , equation (9) needs a series of modifications:

$$\begin{aligned} N \cdot \ln \left(\frac{\tau e^{NT_s/\tau}}{T_w} \right) &= \ln \frac{\text{MTBF} \cdot \tau}{T_C T_D}, \\ N \left(N \cdot \ln(e^{T_s/\tau}) + \ln \left(\frac{\tau}{T_w} \right) \right) &= \ln \frac{\text{MTBF} \cdot \tau}{T_C T_D}, \\ \frac{T_s}{\tau} N^2 + \ln \left(\frac{\tau}{T_w} \right) N - \ln \frac{\text{MTBF} \cdot \tau}{T_C T_D} &= 0. \end{aligned} \quad (10)$$

It can be seen, that to determinate the number N , equation (9) was modified to quadratic equation (10), where N is an unknown variable. (11) presents the roots of the quadratic equation (10).

$$N = \frac{-\ln \left(\frac{\tau}{T_w} \right) \pm \sqrt{\ln^2 \left(\frac{\tau}{T_w} \right) + 4 \frac{T_s}{\tau} \ln \frac{\text{MTBF} \cdot \tau}{T_C T_D}}}{2 T_s / \tau}. \quad (11)$$

It can be easily shown that one of the roots always has a negative value (by putting approximate powers of parameters into (11)). The final equation for the proposed latches will be:

$$N = \frac{-\ln \left(\frac{\tau}{T_w} \right) + \sqrt{\ln^2 \left(\frac{\tau}{T_w} \right) + 4 \frac{T_s}{\tau} \ln \frac{\text{MTBF} \cdot \tau}{T_C T_D}}}{2 T_s / \tau}. \quad (12)$$

A graphical environment for the proposed automated system. A graphical environment is developed for the proposed automated system (Fig.6).

This environment helps to measure, calculate and analyze the synchronizer's parameters more easily.

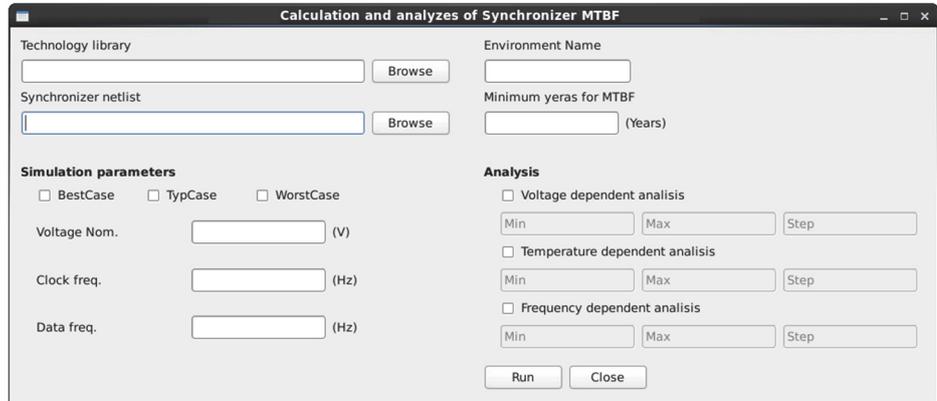


Fig.6. The main window of the graphical environment

In “Simulation parameters” the field designer sets up the simulation nominal voltage, data and clock frequencies, process/voltage/temperature (PVT) corners: “BestCase” ($ff/+10\%V/125^{\circ}C$), “TypCase” ($tt/nom.voltage/25^{\circ}C$), “WorstCase” ($ss/-10\%V/-40^{\circ}C$).

The number of latches is proposed by the system, corresponding to the value of MTBF defined in the field “Minimum years for MTBF”.

Some parameters can be chosen and analyzed, using the “Analysis” field.

When the analysis is complete and all the measurements are carried out, the automated system displays the results in a new window (Fig.7). All the results are saved in an Excel spreadsheet, which may have different sheets based on the setup.

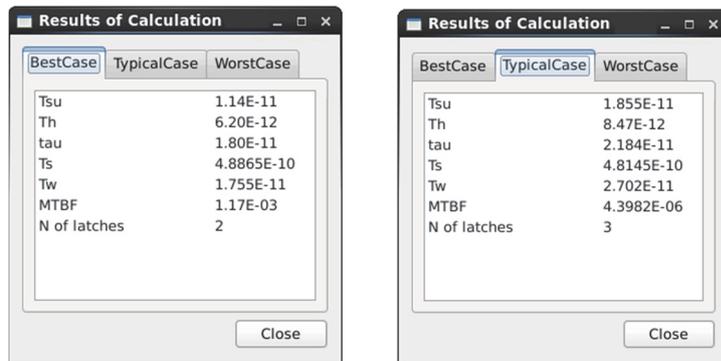


Fig.7. The output window of the graphical environment

In “BestCase”, “TypCase” and “WorstCase” sheets’ measurement and calculation, the results are presented in Fig.8.

Td	1.00E-09
Tc	1.00E-09
Tsu	1.14E-11
Th	6.20E-12
tau	1.80E-11
Ts	4.89E-10
Tw	1.76E-11
MTBF	3.68E+04 sec
	1.02E+01 hour
	1.17E-03 years
MTBF spec	2.00E+20 years
Number of latches	2

BestCase TypCase WorstCase Analysis_Charts Analysis_Results

Fig.8. The view of a single sheet of an Excel spreadsheet

The results of the selected analysis are reported in the “Analysis_Charts” and “Analysis_Results” sheets. Based on the values of the “Analysis_Results” (Fig.9), some diagrams are generated (Fig.10) which are saved in the “Analysis_Charts” sheet.

Voltage	0.8	Voltage	0.87	Voltage	0.94	Volts
Td	1.00E-09	Td	1.00E-09	Td	1.00E-09	Td
Tc	1.00E-09	Tc	1.00E-09	Tc	1.00E-09	Tc
Tsu	1.75E-11	Tsu	1.56E-11	Tsu	1.43E-11	Tsu
Th	8.20E-12	Th	8.10E-12	Th	7.90E-12	Th
tau	1.97E-11	tau	1.92E-11	tau	1.87E-11	tau
Ts	4.825E-10	Ts	4.84E-10	Ts	4.86E-10	Ts
Tw	2.566E-11	Tw	2.37E-11	Tw	2.22E-11	Tw
MTBFn	1.65E+03 sec	MTBFn	3.71E+03 sec	MTBFn	8.60E+03 sec	MTB
	4.59E-01 hour		1.03E+00 hour		2.39E+00 hour	
	5.24E-05 year		1.18E-04 year		2.73E-04 year	
Temperature	-40	Temperature	-20	Temperature	0	Tem
Td	1.00E-09	Td	1.00E-09	Td	1.00E-09	Td
Tc	1.00E-09	Tc	1.00E-09	Tc	1.00E-09	Tc
Tsu	1.20E-11	Tsu	1.18E-11	Tsu	1.18E-11	Tsu
Th	7.30E-12	Th	7.00E-12	Th	7.00E-12	Th
tau	1.93E-11	tau	1.92E-11	tau	1.92E-11	tau
Ts	4.881E-10	Ts	4.88E-10	Ts	4.88E-10	Ts
Tw	1.925E-11	Tw	1.88E-11	Tw	1.88E-11	Tw
MTBFn	4.99E+03 sec	MTBFn	5.86E+03 sec	MTBFn	5.90E+03 sec	MTB
	1.39E+00 hour		1.63E+00 hour		1.64E+00 hour	
	1.58E-04 year		1.86E-04 year		1.87E-04 year	
Frequency	100 meg	Frequency	200 meg	Frequency	500 meg	Freq
Td	1.00E-09	Td	1.00E-09	Td	1.00E-09	Td
Tc	1.00E-08	Tc	5.00E-09	Tc	2.00E-09	Tc
Tsu	1.14E-11	Tsu	1.14E-11	Tsu	1.14E-11	Tsu
Th	6.20E-12	Th	6.20E-12	Th	6.20E-12	Th
tau	1.80E-11	tau	1.80E-11	tau	1.80E-11	tau

stCase TypCase WorstCase Analysis_Charts Analysis_Results

Fig.9. The view of the “Analysis_Results” sheet

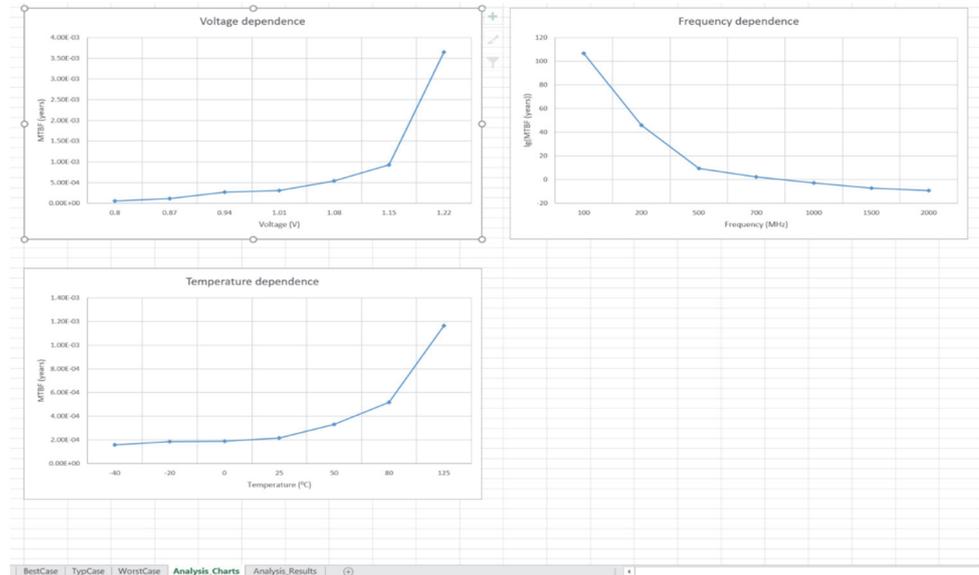


Fig.10. The view of the “Analysis_Charts” sheet

The overall working time of the proposed automated system for all selected options is 1 min. 12 sec.

The results of the proposed method are compared with the manual measurements for the typical corner (Table).

Table

Comparison of the manual and proposed methods

Type of measurement	T _{SU} (ps)	T _H (ps)	τ (ps)	T _S (ps)	T _W (ps)	MTBF (years)
Manual	17.9	9.3	21.3	481	27.2	7.8*10 ⁻⁶
Proposed automated system	18.6	8.4	21.8	481.5	27	4.4*10 ⁻⁶

Conclusion. Metastability parameter measurements, and MTBF calculation methods are researched. A new automated system is developed for measuring the mentioned parameters and MTBF calculation. The system proposes the minimum number of latches to meet the design specification. The proposed automated system analyzes the synchronizer and generates appropriate reports and graphics.

REFERENCES

1. **Melikyan, V., Babayan, E., Khazhaky, T., Manukyan, S.** Analysis of the impact of metastability phenomenon on the latency and power consumption of synchronizer circuits // East-West Design & Test Symposium (EWDTS). – 2016 IEEE. – P. 1-3.
2. **Baker R.J.** CMOS: Circuit Design, Layout, and Simulation. – 2010.

3. **Jones I.W., Yang S., Greenstreet M.** Synchronizer behavior and analysis // Asynchronous Circuits and Systems, 2009. ASYNC'09: 15th IEEE Symposium on. – IEEE, 2009. – P. 117-126.
4. **Chong A.B.** Product Level MTBF Calculation // Intelligent Systems, Modelling and Simulation (ISMS): 2014 5th International Conference on. – IEEE, 2014. – P. 749-754.
5. Variability in multistage synchronizers/ **S. Beer, J. Cox, R. Ginosar, et al** // IEEE Transactions on Very Large Scale Integration (VLSI) Systems. – 2015. – №. 12. – P. 2957-2969.
6. **Mak T.** Truncation error analysis of MTBF computation for multi-latch synchronizers // Microelectron. J. – 2012.-Vol. 43, no. 2. – P. 160-163.
7. **Thote V.S., Khetade V.E.** Modified synchronizer for protection from metastability // Recent Trends in Electronics, Information & Communication Technology (RTEICT): IEEE International Conference. –2016. – P. 1393-1397.

“Synopsys Armenia” CJSC. The material is received 16.10.2018.

Ջ.Ս. ԱՎԵՏԻՍՅԱՆ

ՄԻԱԿԱՍԿԱՂ ՄԻՆՔՐՈՆԱՑՆՈՂ ՍԱՐՔԵՐՈՒՄ ԽԱՓԱՆՈՒՄՆԵՐԻ ՄԻՋԵՎ ԸՆԿԱԾ ԺԱՄԱՆԱԿԱՀԱՏՎԱԾԻ ՉԱՓՈՒՄ, ՀԱՇՎԱՐԿ ԵՎ ՎԵՐԼՈՒԾՈՒԹՅՈՒՆ՝ ԱՎՏՈՄԱՏԱՑՎԱԾ ՀԱՄԱԿԱՐԳԻ ԿԻՐԱՌՄԱՍԲ

Բյուրեղի վրայի համակարգերում տարբեր սինքրոնազանչանային տիրույթներում աշխատող հանգույցներն անհրաժեշտ է սինքրոնացնել: Դրա համար գոյություն ունեն հատուկ սխեմաներ՝ սինքրոնացնող սխեմաներ: Քանի որ հնարավոր չէ կանխատեսել մեկ այլ սինքրոնազանչանային տիրույթում գեներացված ազդանշանի ժամանման պահը, սինքրոնացնող սխեմաներում կարող են առաջանալ մետակայուն վիճակներ: Մետակայունությունը կարող է հանգեցնել հաջորդ սխեմաների խափանմանը, որն իր հերթին կարող է հանգեցնել ամբողջ համակարգի ոչ ճիշտ աշխատանքին: Հետևաբար, շատ կարևոր է ինտեգրալ սխեմայի նախագծման և ստուգման փուլում գնահատել խափանումների հավանականությունը (խափանումների միջև ընկած ժամանակահատվածը՝ ԽՄԸԺ):

Ուսումնասիրվել են մետակայուն վիճակի պարամետրերի չափման և ԽՄԸԺ-ի հաշվարկի մեթոդները: Նախագծի ստուգման ռեսուրսները խնայելու համար առաջարկվել է ավտոմատացված համակարգ, որը չափում և հաշվում է վերոնշյալ պարամետրերը, կատարում է սինքրոնացնող սխեմայի պարամետրերի վերլուծություն:

Առանցքային բառեր. խափանումների միջև ընկած ժամանակահատված, բազմա-սինքրոնազանչանային բյուրեղի վրայի համակարգ, սինքրոնացնող սխեմա, ժամանակային պարամետրեր, չափում, ավտոմատացված համակարգ:

З.М. АВETИСЯН

**ИЗМЕРЕНИЕ, РАСЧЕТ И АНАЛИЗ ВЕЛИЧИНЫ НАРАБОТКИ НА ОТКАЗ В
ОДНОКАСКАДНЫХ СИНХРОНИЗАТОРАХ С ИСПОЛЬЗОВАНИЕМ
АВТОМАТИЗИРОВАННОЙ СИСТЕМЫ**

В системах на кристалле узлы, работающие в различных синхросигнальных областях, нуждаются в синхронизации. Для этого существуют специальные схемы, называемые синхронизаторами. Так как время прибытия сигнала даты, генерированного в другой синхросигнальной области, невозможно предвидеть, в синхронизаторах могут возникнуть метастабильные состояния. Метастабильность может привести к сбоям в последующих схемах и, как следствие, к сбою общей системы. Следовательно, на этапе проектирования и верификации интегральной схемы очень важно оценить вероятность сбоев (наработок на отказ - ННО).

В рамках статьи исследованы методы измерения параметров метастабильного состояния и расчета ННО. Для сбережения ресурсов верификации проекта предложена автоматизированная система, которая измеряет и вычисляет вышеупомянутые параметры, анализирует параметры синхронизатора.

Ключевые слова: наработка на отказ, многосинхросигнальная система на кристалле, синхронизатор, временные параметры, измерение, автоматизированная система.