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MODELING OF ELECTROSTATICS AND DRAIN CURRENT SOI FinFET

An analytical expression is obtained for 2D electrostatic potential in Tri-Gate SOI FinFET in weak and moderate inversion regimes. The obtained solution allows to calculate the threshold voltage with great accuracy. Further, a simple model is proposed to calculate the drain current. The calculations are performed considering silicon thicknesses from 10 *nm* to 60 *nm* and channel length down to 25 *nm*. The model is validated with numerical simulations, and good accuracy is obtained.

Keywords: SOI FinFET, MOSFET, undoped body, Tri-gate FET, threshold voltage, potential model.

Introduction. Multi-gate devices such as Double Gate (DG) or Tri-Gate (TG) MOSFETs are attractive alternatives of planar MOSFETs. The multi-gate control of the channel highly suppressed the short channel effects [1-4]. Another example of the DG structure is the thin film in-plane gate FETs, where the electrostatics of two-dimensional system dominate. Such electrostatic problems in 2D systems are well interpreted in [5]. Besides, the Fin-shaped Field Effect Transistors (FinFET) have excellent compatibility with existing CMOS fabrication technology [2-4]. The experimental and simulation results show that the TG FinFET dimensions are more flexible and relaxed compared to single-gate or DG devices. To avoid the doping challenges and the implied threshold voltage variations, the undoped body is the proper choice for these structures [6-9]. Analytical models of the electrostatics are extremely important in guiding the device design and in providing physical insights of the device behaviour. There are already several published analytical works on TG FETs [10-13]. However, the accurate analytical modeling of TG FinFETs is rather challenging. A. Kloes et al have developed an analytical, structure oriented model for the potential barrier in undoped TG FinFETs, which inherently includes short channel and corner effects [10]. However they neglect mobile charge term in sub-threshold regime, and this makes the potential solution less accurate, since the mobile charge will affect the electrostatic performance in near-threshold regime whereas the corner effects are not essential for undoped body [7-9]. The mobile charge term in weak inversion was neglected also in [11]. The mobile charge was accounted in the model suggested by El Hamid et al [12] but they simply assume the parabolic decay for the potential along the vertical direction (from top gate to bottom), and by defining the parameters from boundary conditions expand the solution of DG FET to TG.

An analytical compact model for the threshold voltage of TG FinFETs is presented in [13], however the dependence on top oxide thickness is not included in the model. The generalized threshold analyses is provided in [6] valid only for an ultra-thin body.

In this paper, we present a potential-based semi-analytical model for TG SOI FinFET which is valid for large range of structural parameters. The presented model can be considered also as the generalisation of DG MOSFET model [14]. The 2D Poisson equation is solved in weak inversion including the mobile charge term. The model is derived for long channel TG SOI FinFET, however it can be easily be extended to short channel devices based on [15]. The silicon body thickness and height are considered to be greater than thermal de Broglie wave length (which is about 8 *nm* for Si [16]), thus the quantum effects can be neglected. The extensive validation of analytical model with numerical simulations shows the accuracy of the proposed model.

The paper is organized as follows. Section I presents the analytical model for the electrostatic potential in sub-threshold and moderate inversion. The modeling of TG FET in strong inversion is presented in Section II. Section III presents the comparisons with numerical simulations and discussions.

Methodology: Analytical model

1. **Weak and moderate inversion**. Fig. 1 shows the cross section of the FinFET structure considered. The silicon fin is of height H, width W, the side oxides are of thickness t_{ox_side}, the top oxide is of thickness t_{ox_top}.

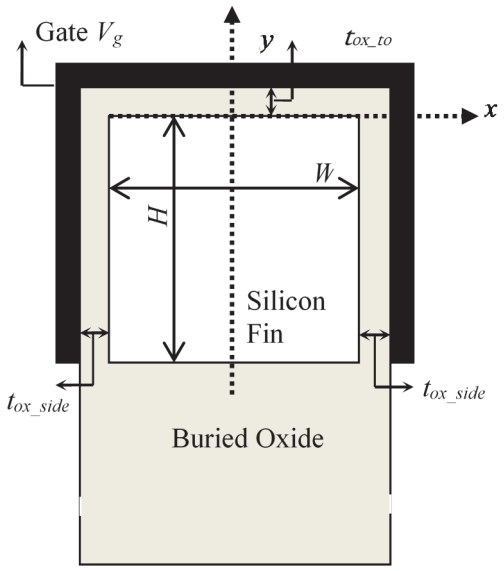


Fig. 1. Cross section of the TG FinFET structure

For long channel devices, the impact of the drain voltage in the formation of sub-threshold current is negligible, thus, for simplicity, in this stage of development we assume that the source and drain are grounded. All energies are referred to the Fermi energy of the channel. Top and side gates are at the same voltage (V_g).

We can write the Poisson equation in the silicon fin considering only the mobile electrondensity:

$$\frac{\partial^2 \varphi(x,y)}{\partial x^2} + \frac{\partial^2 \varphi(x,y)}{\partial y^2} = \frac{q}{\varepsilon_{si}} n_i e^{\frac{\varphi(x,y)}{V_T}}, \tag{1}$$

where q is the electron charge, ε_{si} -the silicon permittivity, n_i - the silicon intrinsic carrier density, and V_T- the thermal voltage. For symmetry considerations, (1) can be solved only for $x \geq 0$, with the following boundary conditions (BCs),

$$\left(\frac{\partial\, \varphi(x,y)}{\partial x}\right)_{x=0} = 0, \tag{2}$$

for the top gate, and for $-W/2 \leq x \leq W/2$, we have:

$$C_{ox\_Top}\left(V_g^* - \varphi(x,0)\right) = \varepsilon_{si}\left(\frac{\partial \varphi(x,y)}{\partial y}\right)_{y=0,}, \tag{3}$$

where as for the side gate, for $-H \leq y \leq 0$,

$$C_{ox\_Sd}\left(V_g^* - \varphi(W/2,y)\right) = \varepsilon_{si}\left(\frac{\partial \varphi(x,y)}{\partial x}\right)_{x=W/2}, \tag{4}$$

where C_{ox_Sd}=$\varepsilon_{ox}/t_{ox\_side}$ and C_{ox_Top}=$\varepsilon_{ox}/t_{ox\_top}$ are the capacitances per unit area of the side and top oxides, respectively; V_g^*= V_g– ϕ_{ms} where ϕ_{ms} is the work function difference between the gate electrodes and intrinsic silicon. Thus, when V_g^*=0 the potential is zero everywhere in the silicon fin. We also assume that the buried oxide is thick enough:

$$\left(\frac{\partial \varphi(x,y)}{\partial y}\right)_{y=-H} = 0. \tag{5}$$

Let us at first consider the one-dimensional Poisson equation along the y axis, discarding for a moment the side gates and the dependence on x. Then we have:

$$\frac{\partial^2 \varphi(y)}{\partial y^2} = \frac{q}{\varepsilon_{si}} n_i e^{\frac{\varphi(y)}{V_T}}, \tag{6}$$

$$\frac{\partial \varphi}{\partial y} \Big|_{y=-H} = 0 \, , \varphi(0) = \varphi_s. \tag{7}$$

While considering sub-threshold conditions, the potential mostly follows V_g, and varies little in the silicon cross section. For our convenience, we can introduce $\varphi(y)$ as:

$$\varphi(y) = V_g^* - \varphi^*(y), \tag{8}$$

where $\varphi^*(y)$ is the variation of the potential along the cross section. In sub-threshold $\varphi^*(y)$ is smaller than the thermal voltage. We substitute (8) in (6) and approximate the exponential with the first term of Taylor's expansion:

$$\frac{\partial^2 \varphi*(y)}{\partial y^2} = \frac{q}{\varepsilon_{si}} n_i e^{\frac{V_g^*}{V_T}} \left(1 - \frac{\varphi*(y)}{V_T}\right). \tag{9}$$

The solution of (7) and (9) can be presented in a trigonometric form:

$$\varphi^*(y) = (\varphi_s - C) \operatorname{Cos}\left(\frac{H+y}{b}\right) Sec\left(\frac{H}{b}\right) + C, \tag{10}$$

where $C=V_T$ and

$$b = \sqrt{\frac{C\varepsilon_{si}}{q n_i}} e^{-\frac{V_g^*}{2V_T}}. \tag{11}$$

One can expect that the 2D potential in the Fin cross section of the TG FET has the same profile in the vertical direction as (10) with the only difference that now parameters C and b are functions of x due to side gates. Therefore, we can write:

$$\varphi(x,y) = \left[\varphi_{tp}(x) + C(x)\right] Cosh\left(\frac{H+y}{b(x)}\right) Sech\left(\frac{H}{b(x)}\right) - C(x), \tag{12}$$

where $\varphi_{tp}(x) \equiv \varphi(x,0)$ is the surface potential at the top interface. Equation (12) determines the potential distribution in TG SOI MOSFET in the sub-threshold regime.

Substituting (12) in BC (3), and assuming $H \gg b(x)$ we obtain:

$$b(x) = \frac{\varepsilon_{si}(\varphi_{tp}(x) + C(x))}{C_{ox\_Top}\left[V_g^* - \varphi_{tp}(x)\right]}. \tag{13}$$

It is easy to see that $b(x)$ has the meaning of a screening length along the vertical direction and is proportional to the top oxide thickness. If we substitute

(12) for y=–*H* in (1), (2), and (4), we obtain equations similar to the set of equations for the DG MOSFET [14], since close to the bottom, the first term in potential (12) is very small and the top gate is distant. We have:

$$\varphi(x,-H) \approx -C(x) = \varphi_{DG}(x) = \varphi_{DG}(0) - 2\,V_T ln\left[cos\left(\sqrt{\frac{q^2 n_i}{2\varepsilon_{si} kT}} e^{\frac{\varphi_{DG}(0)}{2V_T}} x\right)\right], \quad (14)$$

where $\varphi_{DG}(0)$ is the central potential of DG MOSFET and can be defined from BC (4) rewritten for the DG structure.

For the top surface potential we can assume the same profile as we have for the side surface potential (see eq.(10)):

$$\varphi_{tp}(x) = \varphi_{tp}(0) + a\,\left[Cosh\left(\frac{x}{\beta}\right) - 1\right], \quad (15)$$

where $\varphi_{tp}(0) = \varphi(0)$ (the potential, at the point s in Fig.1), a and β are the functions of V_g^*, W, H, C_{ox_Sd}, C_{ox_Top}. Parameter a can be obtained from BC (4) as:

$$a = \frac{V_g^* - \varphi_{tp}(0)}{Cosh\left(\frac{W}{2\beta}\right) - 1 + \frac{\varepsilon_{si}}{\beta\, C_{ox\_Sd}} Sinh\left(\frac{W}{2\beta}\right)}. \quad (16)$$

Eq. (5) suggests writing $\varphi_{ST}(0)$ as the surface potential of DG FET for which the potential in the center is equal to $\varphi(0,-H)$:

$$\varphi_{tp}(0) = V_g^* - \frac{1}{C_{ox\_Top}} \sqrt{2\varepsilon_{si} kT n_i} \left(e^{\frac{\varphi_{tp}(0)}{2V_T}} - e^{\frac{\varphi(0,-H)}{2V_T}}\right), \quad (17)$$

where

$$\varphi(0,-H) = \left(\varphi_{tp}(0) - \varphi_{DG}(0)\right) Sech\left(\frac{H}{b(0)}\right) + \varphi_{DG}(0). \quad (18)$$

Substituting (12) and (15) into Poisson eq. (1) and setting $y = 0$, $x=W/2$, we obtain an equation for β:

$$-\psi\left(1 + \frac{\Delta_\varphi}{V_T} + \frac{\Delta_V}{V_T \Delta_\beta}\right) + \frac{\Delta_V}{\beta^2\, \Delta_\beta} + \frac{{\Delta_V}^2 \left(\Delta_\beta - 1\right)^2}{\left(\frac{\varepsilon_{si}}{C_{ox\_Top}}\right)^2 \left({\Delta_\beta}^2 \Delta_\varphi + \Delta_V\, \Delta_\beta\right)} = 0\,, \quad (19)$$

where $\psi \equiv \frac{q}{\varepsilon_{si}} n_i exp\left(\frac{\varphi_{DG}(w/2)}{V_T}\right)$, $\Delta_\varphi \equiv \varphi_{tp}(0) - \varphi_{DG}(w/2)$, $\Delta_V \equiv V_g^* - \varphi_{tp}(0)$, $\Delta_\beta \equiv 1 + \frac{\varepsilon_{si}}{\beta\, C_{ox\_Sd}}$.

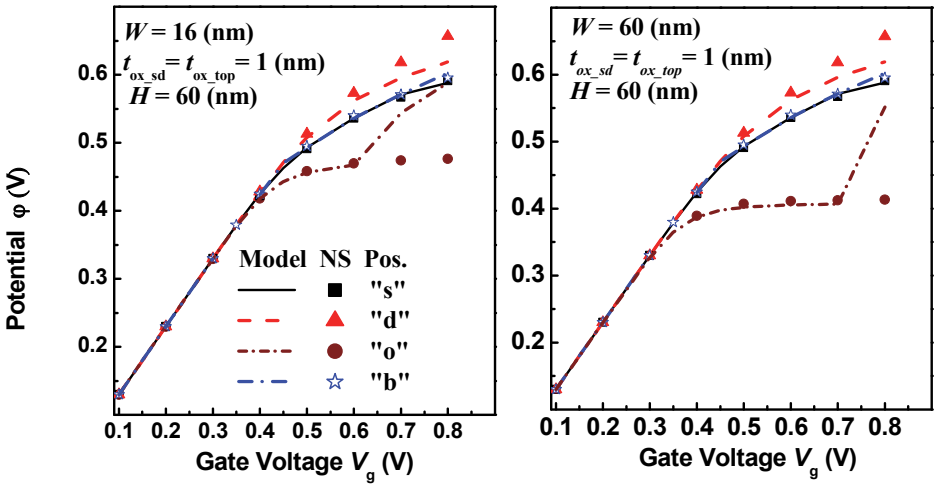
Eq. (19) is a cubic equation with respect to β, only one solution of which has physical meaning. The solution is presented in the Appendix. This procedure to substitute the approximate solution (12) into the Poisson equation (1) to define the parameter β makes the derived potential model more accurate.

Thus according to our TG FinFET model, the 2D potential in sub-threshold and near-threshold regimes is given by (12), with parameters defined from (13) - (19).

2. Strong inversion regime. At strong inversion regime, the screening of the mobile charge is so effective that the total mobile charge of TG FinFET can be computed as the sum of the charge induced on the sides of 2- DG FinFETs: a DG FET with silicon thickness *W* and of width *H* and (i.e., discarding the effect of the top gate), let's call it as "$DG_{\|}$", plus the charge induced under the top gate computed as the half charge of a DG FET of width W and silicon thickness H(i.e., discarding the effect of the side gates), we will call it "$DG_{=}$".

The "2-DG model" will allow to use any of compact charge - based models derived for DG devices, e.g. [15], to compute the output characteristics of TG Fin FET in strong inversion. Due to this "2-DG model" the drain current will be sensitive not only to side oxide variations but also to the top oxide thickness which, in general, can be different from the side oxide thickness.

Results and discussion. To validate the derived model we compare analytical calculations with 2D TCAD simulations [17]. In Fig. 2 we compare the results derived from our potential model presented in Section 2 (let us call it "TG model") with numerical simulations (NS).The potential is plotted as a function of the gate voltage for four different positions (o,s,b,d) in the Fin (indicated in Fig.1), for different values of W(16 nm and 60 nm). It is seen that the proposed potential model well works in sub-shold and in moderate inversion regimes, whereas in the strong inversion regime, the mismatch is evident since the potential in position "o" saturates and therefore (9) is not applicable. The excellent agreement between the model and NS for the potential at point "s" makes evident the accuracy of $DG_{=}$ assumption. As it was expected, in moderate inversion the highest potential is at the corner (point "d") which mainly defines the threshold voltage and is responsible for its divergence from DG case.



a) b)

Fig. 2. Potential versus gate voltage at different points of silicon body for two structures with widths: W=16 nm (a) and W=60 nm (b)

From the TG model it is possible to extract the threshold voltage in a very precise way, for a broad range of H/W ratios and for a different side and top oxide thicknesses, as shown in Fig. 3. As can be seen, the maximal error with respect to threshold voltage calculated in the same way from numerical simulations is about 3 mV. In Fig.4 the charge calculated from these models is compared with numerical simulations for four different structures. As can be seen in Fig. 4, the TG model well predicts the charge in sub-threshold and near-threshold regimes, and therefore is good also for extracting the threshold voltage. In the linear region the drain current is proportional to the charge in the channel, and thus the threshold voltage is defined here as the gate voltage for which the third derivative of the charge as a function of the gate voltage is zero.

Up to this point we have been considering a long channel, however the simple implementation of the 2-DG model allows to use the model developed for ultra scalled DG FinFET [15] and to calculate the drain current in short TG FinFET. Due to implementation of the 2-DG model the drain current is sensitive not only to the side oxides' thickness but also to the top oxides' thickness. In Fig. 5 are illustrated the calculations for TG FinFET with 25 *nm* channel length and 10 *nm* silicon thickness and height. The analytical calculations are compared with 3D TCAD simulations performed in Sentaurus platform. As it is seen, the agreement is quite good.

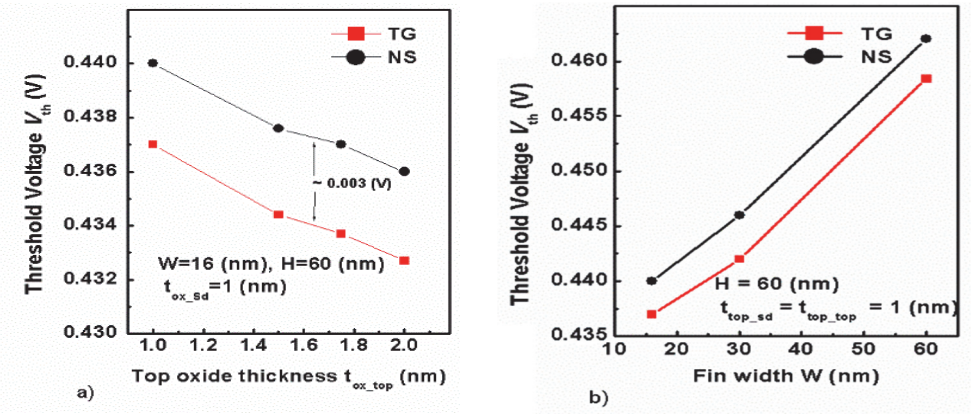


Fig. 3. Threshold voltage data calculated from TG model and numerical simulations (NS) for structures with different top oxide thickness t_{ox_top} (a) and for different silicon width W (b)

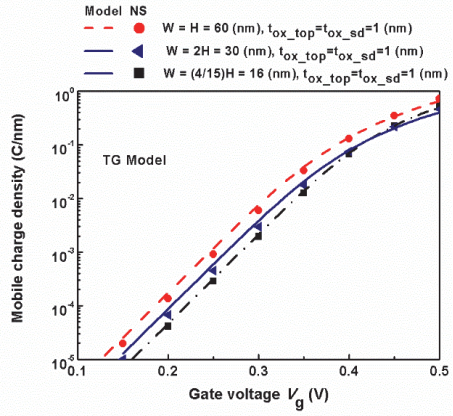


Fig.4. Mobile charge density calculated from TG model in sub-threshold and weak inversion regimes

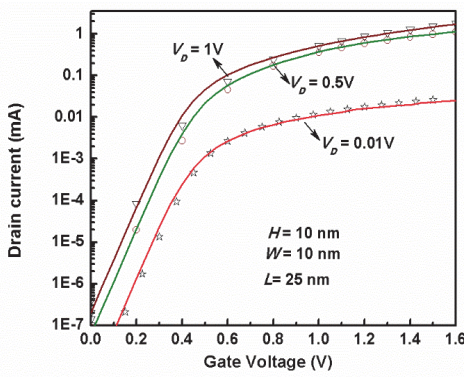


Fig.5. Drain current calculated using 2-DG approach for 25 nm Tri-gate FinFET. Lines: analytical model, symbols: 3D numerical simulations with Sentaurus Synopsys

Conclusion. In this paper an analytical expression of two-dimensional potential in undoped TG FinFET is derived applicable in sub-threshold and in moderate inversion conditions. On the basis of the derived potential model, the threshold voltage of the device is estimated with high precision. Further, to model the charge in strong inversion, a model of 2-DG FinFETs is proposed. The proposed 2-DG model is very sensitive to the device parameters, including the top oxide thickness, and imply to extend the DG drain current model for short channel devices to TG FinFET.

Appendix

Solution of (19)

$$\frac{1}{\beta} = -\frac{B_2}{3B_3} + \frac{2^{1/3}\cdot\left(B_2^{\,2} + 3B_3\cdot B_1\right)}{3B_3\cdot A_{BD}} + \frac{A_{BD}}{2^{1/3}\cdot 3B_3}\ , \text{ where}$$

$$A_{BD} = \left(A_B + \sqrt{-4\left(B_2^{\,2} + 3B_3\cdot B_1\right)^3 + A_B^{\,2}}\right)^{1/3},\quad A_B = -2B_2^{\,3} - 27B_3^{\,2}D_1 - 9B_1B_2B_3\ ,$$

$$D_1 = -\psi\cdot\left(1 + \frac{\triangle\varphi + \triangle \mathrm{V}}{V_T}\right)\cdot(\triangle \mathrm{V} + \triangle\varphi),\quad B_1 = \frac{\varepsilon_{Si}}{C_{ox\_\mathrm{Top}}}\psi\cdot\left(\triangle\varphi\cdot 2\left(1 + \frac{\triangle\varphi}{V_T}\right) + \cdot\triangle \mathrm{V}\left(1 + 2\frac{\triangle\varphi}{V_T}\right)\right),$$

$$B_2 = -\psi\cdot\triangle\varphi\cdot\left(1 + \frac{\triangle\varphi}{V_T}\right)\cdot\left(\frac{\varepsilon_{Si}}{C_{ox\_Sd}}\right)^2 + \triangle \mathrm{V}\cdot\triangle\varphi + \left(\left(\frac{C_{ox\_Top}}{C_{ox\_\mathrm{Sd}}}\right)^2 + 1\right)\triangle \mathrm{V}^2,\quad B_3 = \triangle \mathrm{V}\cdot\triangle\varphi\cdot\frac{\varepsilon_{Si}}{C_{ox\_\mathrm{Top}}}\ .$$

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Ա.Է. ԵՍԱՅԱՆ

ԷԼԵԿՏՐԱՍՏԱՏԻԿԱՅԻ ԵՎ ԵԼՔԱՅԻՆ ՀՈՍԱՆՔԻ ՄՈԴԵԼԱՎՈՐՈՒՄԸ SOI FinFET-ՈՒՄ

Ստացվել է անալիտիկ արտահայտություն երկչափ էլեկտրաստատիկ պոտենցիալի համար եռակի փականով SOI FinFET-ում: Ստացված լուծումը հնարավորություն է տալիս ճշգրտորեն հաշվարկել շեմային լարումը: Առաջարկված է ելքային հոսանքի հաշվարկի պարզ մոդել: Հաշվարկները կատարված են 10-60 *նմ* հաստությամբ և 25 *նմ* երկարությամբ սիլիցիումային ուղետարի համար: Անալիտիկ մոդելը համեմատվել է թվային հաշվարկների հետ, և ցույց է տրվել մոդելի բարձր ճշգրտությունը:

Առանցքային բառեր. SOI FinFET, ՄՕԿ ԴՏ, չլեգիրված ուղետար, եռակի փականով ԴՏ, շեմային լարում, պոտենցիալային մոդել:

А.Э. ЕСАЯН

МОДЕЛИРОВАНИЕ ЭЛЕКТРОСТАТИКИ И ВЫХОДНОГО ТОКА SOI FinFET

Получено аналитическое выражение для двумерного электростатического потенциала в трехзатворном SOI FinFET при слабой и умеренной инверсии. Полученное решение позволяет с высокой точностью вычислить пороговое напряжение. Предлагается простая модель для расчета тока. Расчеты выполнены для каналов толщиной от 10 до 60 *нм* и длиной до 25 *нм*. Аналитическая модель проверена с помощью численного моделирования, и получена хорошая точность.

Ключевые слова: SOI FinFET, MOSFET, нелегированный канал, трехзатворный FET, пороговое напряжение, модель потенциала.