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V.SH. MELIKYAN, K.W. MOVSISYAN

MODELING AND DESIGN OF POWER SUPPLY NETWORK OF AN IC HIGH SPEED I/O INTERFACE

The parasitic inductances of a CMOS integrated circuit (IC) power supply network produce supply rail noises. These noises introduce propagation delay variations and signal jitters which reduce the signal timing budget. This becomes very critical in high speed signaling. In order to compensate the effect of the IC supply system inductances and damp the supply rail noises, an effective approach of the usage of on-die decoupling capacitances is elaborated.

Keywords: integrated circuit, input output system, power supply network, on-die decoupling capacitance.

The IC supply network configuration has direct impact on the operation of I/O buffers and signal distortions. The supply voltage is provided to I/O buffers via Power/Ground I/O cells and internal supply buses. The chip power supply network must be designed in a way not to impact the signal integrity (SI). The main issue is when an output buffer switches it tries to draw current quickly. The parasitic inductances of the power network oppose to the current switching. If the power network inductance is significant it will isolate the voltage source from the buffer during high speed switching. Since the supply network cannot provide needed current, the supply voltage that the buffer has will drop:

$$V_{buf} = V_{DD} - \frac{Ldi}{dt}. \quad (1)$$

The buffer supply voltage noises - drops and peaks - in many cases could be significant, in some cases inadmissible for reliable signal transferring. To reduce the switching noise, the chip I/O interface and the package must be designed and placed on the PCB in a way to minimize the power supply network inductances.

The decoupling capacitance along with power supply network inductance makes up an oscillatory circuit. If the operation frequency is close to the resonance frequency of the supply network there could be large variations of the supply voltage. One of the problems is to damp oscillations. This can be done either by selecting package and decoupling circuit parameters [1] or by including additional circuits into the power supply network, for example, in [2] it is proposed to insert an RLC damping circuit in parallel to the decoupling capacitance.

The schematic diagram of the IC I/O interface is shown in Fig. 1. In order to achieve required SI in high-speed I/O interface the supply I/O cells should be placed

close to the output signal drivers. Depending on the operating frequency and SI requirements the signal I/O to power supply I/O cell ratio can vary in large margin. The examples of the interface with different values of this ratio (8:1; 4:1; 1:1) are shown in Fig. 1. The supply voltage is applied from the on-board power supply through IC package power/ground (VDD/VSS) pins. To manage the required total supply current and SI issues, an I/O interface can have several VDD/VSS pin pairs which are electrically connected in parallel. They are connected to IC substrate VDD/VSS rails. These rails are connected to the VDD/VSS bonding pads of I/O cells via wire bonds. The supply current is provided to the signal I/O cells through the VDD/VSS I/O cells and on die VDD/VSS power buses.

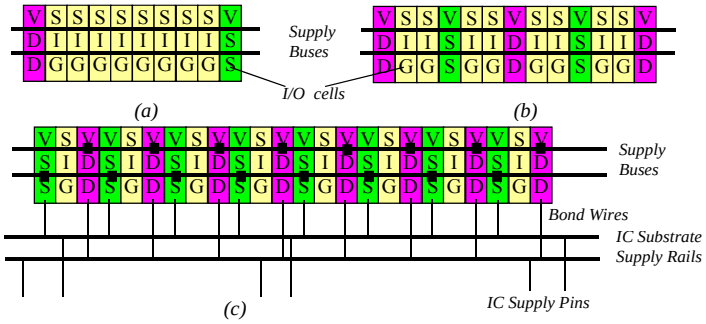


Fig. 1. Signal and power/ground I/O cell arrangement: (a) signal to power cell ratio 8:1; (b) signal to power cell ratio 4:1; (c) signal to power cell ratio 1:1

The VDD or VSS pin-to-substrate inductances are electrically connected in parallel. The equivalent pin inductance is:

$$L_{VDDp2s} = \frac{L_{VDDpin}}{N_{VDD-pin}}, L_{VSSp2s} = \frac{L_{VSSpin}}{N_{VSS-pin}}, \quad (2)$$

where L_{VDDpin} and L_{VSSpin} are IC VDD/VSS supply pin inductances, $N_{VDD\text{-}pin}$ and $N_{VSS\text{-}pin}$ are the numbers of pins, L_{VDDp2s} and L_{VSSp2s} are VDD/VSS pin group equivalent inductances. The minimum number of needed P/G I/O cells is determined from the required total current:

$$N_{VDD-pad-min} = \frac{I_{total}}{I_{pad}}, N_{VSS-pad-min} = \frac{I_{total}}{I_{pad}}, \quad (3)$$

where I_{total} is the IC I/O system total current and I_{pad} is the current of one power or ground I/O cell. The VDD or VSS substrate rail-to-VDD/VSS I/O cell bonding pad inductances can also be considered as connected in parallel:

$$L_{VDDs2b} = \frac{L_{VDDpad}}{N_{VDD-pad}}, L_{VSSs2b} = \frac{L_{VSSpad}}{N_{VSS-pad}}, \quad (4)$$

where L_{VDDpad} and L_{VSSpad} are bonding wire inductances, $N_{VDD\text{-}pad}$ and $N_{VSS\text{-}pad}$ arethe numbers of VDD/VSS I/O cells, L_{VDDpad} and L_{VSSpad} are equivalent inductances of VDD/VSS bonding wires from I/O to IC substrate VDD/VSS rails.

Increasing the number of VDD/VSS I/O cells and pins one can decrease the power network equivalent inductance and hence, reduce the switching noise and improve SI. But this is achieved by die area and package pin overhead. The I/O sub-system area usage efficiency can be estimated by

$$AE = \frac{A_S}{A_T} = \frac{A_S}{A_S + A_P}, \quad (5)$$

where A_S is the area occupied by signal cells, A_P is the area occupied by VDD/VSS cells, A_T is the total I/O system area. For the signal to power ratio of 8:1 the area usage efficiency is 8/10, while for the signal to power ratio of 1:1 the area usage efficiency is only 8/24.

Another efficient approach for noise decreasing is the usage of on-die decoupling capacitances. The decoupling capacitances are charged up to supply voltage and during buffer's switching they discharge supplying needed buffer current. Obviously, the inductance induced noise compensation is as efficient as the decoupling capacitance is large. The large on-die capacitance can be implemented in large area. The available area on the die is strictly limited. The simplified circuit diagram of an IC I/O supply system is shown in Fig. 2. L_{PCB} is the PCB wire inductance from supply voltage source electrodes to chip's VDDsp/VSSsp supply pins.

The on-board decoupling capacitance C_{PCB} is connected between VDDsp/VSSsp pins to compensate L_{PCB}. $L_{VDD\text{-}pin}$, $L_{VSS\text{-}pin}$ are inductances from VDDsp/VSSsp IC pins to the IC substrate supply rails and $L_{VDD\text{-}pad}$, $L_{VSS\text{-}pad}$ are inductances from the IC substrate to on-die VDD/VSS supply I/O cells (pads). The C_d is the total on-die decoupling capacitance basically placed inside the I/O supply cells. This capacitance should compensate the pin and pad inductances. The inductances L_{VDDp2s}, L_{VDDs2b} and L_{VSSp2s}, L_{VSSs2b} can be replaced by following equivalent inductances

. (6)

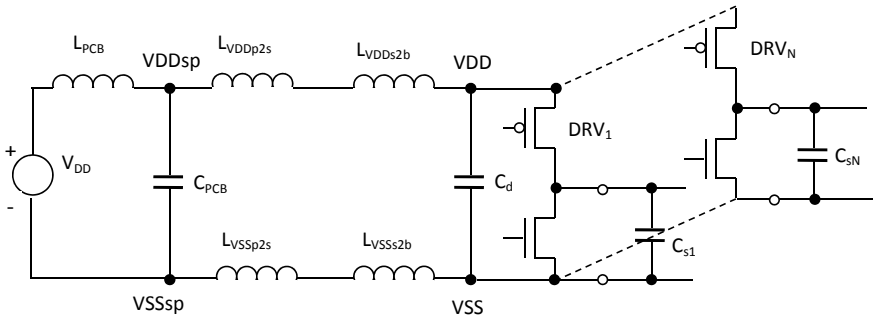


Fig. 2. Simplified circuit diagram of an IC I/O system

The amount of decoupling capacitance should be enough to compensate the supply network inductances. To estimate the needed decoupling capacitance we will assume that the total amount of the current during switching is supplied only by the decoupling capacitance. The decoupling capacitance supplies the load during the buffer switching in a way that the voltage decrease is less than maximum allowed value. The voltage drop can be estimated from charge sharing between decoupling capacitance and the load capacitance. When PMOS buffer conducts, the load capacitance charges from 0 to voltage value V:

$$\Delta V = \frac{C_L}{C_L + C_{IO}} V \quad , \tag{7}$$

where V is the initial nominal voltage across decoupling capacitance C_d. $V=V_{DD}-V_{SS}=$ $=V_{Cd}(t=0)$, $C_L=\Sigma C_{sk}$ is the equivalent load capacitance. In the worst case when all buffers are switched simultaneously, it is the sum of load capacitances of all buffers: $C_L=\Sigma C_{sk}=NC_s$.

The supply voltage drop is restricted by the resulting maximum delay variation which decreases the usable duration (timing budget) of the signal's period in the receiver side

, (8)

where t_{max} is the delay at minimum supply voltage, t_{nom} is the delay at nominal supply voltage.

The formulas allowing estimating the output signal delay variation as function from the supply voltage variation are obtained in [3].

Taking into account the supply network equivalent inductances discussed above, the more realistic simplified circuit diagram can be created, as shown in Fig. 3. This circuit will show up supply voltage oscillations if the signal switching main frequency or its higher harmonics are close to power network resonance frequency.

The magnitude of the voltage oscillations can roughly be estimated as

$$\Delta V = I_s Z(\omega), \tag{9}$$

where I_s is the switching current, Z (ω) is the impedance of the power supply network, ω is the cycle frequency. Since the switching current depends only on the I/O signal loading, a way to get small voltage variations is to keep Z (ω) as small as possible.

The impedance of the supply network is given by the following formula:

$$Z(\omega) = R_{BS} \sqrt{((1 - R_1 d/R_1 s)^2 + \omega^2 (L_1 s/R_1 s + R_1 d\, C_1 d)^2)/((1 - (\omega^2 L_1 s\, C_1 d))^2 + \omega^2 C_1 d^2 (R_1 d + R_1 s)^2)}$$

. (10)

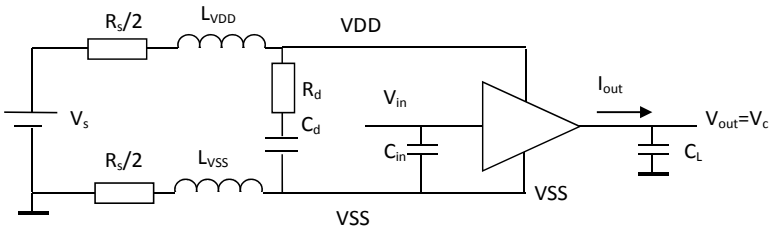
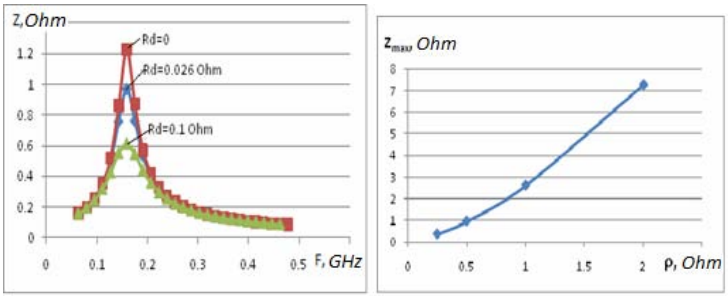


Fig. 3. IC I/O system supply network equivalent circuit

For the simplified case with very large L_s, $Rs=R_d=0$, and $\omega_r<\omega$ one can get $Z\cong 1/\omega C_d$, and the voltage variations can be estimated by (7). It is seen that increasing R_s and/or R_d will decrease the voltage oscillations. However, increasing R_s will increase the DC voltage drop on the power network and the IC will be supplied under reduced supply voltage $V_{DD}=V_S-IR_S$, and delays will increase. The increase of the R_d will also contribute to damping of power rail voltage oscillations. The power network impedance-frequency characteristics for three cases of R_d are shown in Fig. 4a. Increasing R_d can also have a negative impact – will increase the voltage drop on the R_d-C_d series circuit and increase oscillations.

It is obvious that it is preferable to have the resonance frequency below operating frequency range. However, in most cases it will be very costly since a low resonance frequency requires a large decoupling capacitance. A large inductance will reduce the resonance frequency, but will not help to reduce voltage variations and a large decoupling capacitance will be needed to compensate the inductance. In Fig. 4b is shown the supply network peak impedance, Z_{max}, dependence on the network characteristic impedance, $\rho=(L_s/C_d)^{0.5}$, for a constant resonance frequency, $\omega_r=(LsCd)^{-0.5}=1$ ($R_s=0.1$ *Ohm*, $C_d=0.026$*Ohm*). For small voltage variations it is necessary to have small Z_{max}, and hence small ρ. For small values of ρ it is necessary to have small inductance and large capacitance.



(a) *(b)*

Fig. 4. (a) The power network impedance-frequency characteristics: $R_s=0.1$ Ohm, $L_s=0.5$ nH, $C_d=2$ nF; (b) the power network peak impedance, Z_{max}, dependence on the network characteristic impedance, ρ

If the network is well damped, then having the resonance frequency in the operating frequency region could not be an issue. Considering the power supply network as second order network shown in Fig. 3 the supply rail voltage variations can be represented as [1]:

(11)

ΔV is given by (8), ς is the damping factor. For low magnitude oscillations it is beneficial to have large damping factor. As mentioned above the R_s and R_d values cannot be increased significantly. The main means remains as reducing ρ by increasing the decoupling capacitance, C_d, and controlling R_d. The reasonable value of the damping factor could be in the range $0.1 < \varsigma < 0.4$.

The decoupling capacitance on the chip is realized with the gate capacitance of MOS transistors (Fig. 5). The MOS capacitance has drain, source and bulk connected together and is tied to the ground which serves as one of electrodes of the capacitance. The gate of the MOS device serves as the second electrode. The MOS capacitance has also a parasitic resistance R due to nonzero channel resistance of the MOS device.

In [4] the NMOS capacitance is considered as distributed RC line and derived the input impedance as follows.

$$Z_{dist}(s) = 1/(sC_{ch}) + R_{ch}/12 \quad . \tag{12}$$

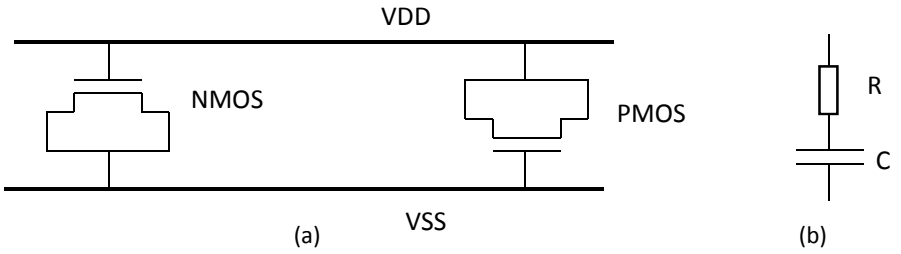


Fig. 5. MOS transistor used as a capacitor: (a) usage in a circuit; (b) equivalent circuit

Comparing with the impedance of a lumped resistor in series with a capacitor (Fig. 6b) one can find:

$$Z_{lumped}(s) = 1/sC + R \quad . \tag{13}$$

It can be seen that

$$C = C_{ch}$$
$$R = \frac{R_{ch}}{12} \quad . \tag{14}$$

The decoupling capacitors consist of parallel connection of many cells. The capacitance of a cell is determined as

$$C_{cell} = c_{ox}A_{cell} = c_{ox}WL \quad , \tag{15}$$

where A_{cell} is the cell gate area, $A_{cell}=WL$, c_{ox} is the gate oxide capacitance [5], $c_{ox}=\varepsilon\varepsilon_0/T_{ox}$, ε is the gate oxide dialectical permeability, ε_0 is the electrical constant, T_{ox} is the gate oxide thickness.The required decoupling capacitance is composed by parallel connection of N cells:

$$C_d = NC_{cell} = Nc_{ox}WL \quad . \tag{16}$$

Respectively, the decoupling capacitance area is determined as:

$$A_d = NA_{cell} \, . \tag{17}$$

The effective area occupied by the decoupling capacitance is larger than given by (17) since there is an area overhead due to the spacing between cells according to design rules.

To estimate the series resistance of a decoupling capacitor cell, we have to determine the channel resistance R_{ch} of the cell. In the capacitor configuration of the MOS there is a symmetrical conducting channel between the source and drain with $V_{ds}=0$. The simplified current-voltage characteristic of MOS device in the linear mode (not saturated mode) is represented in [5]

$$I_{ds} = \frac{\left(\frac{W}{L}\right)k_p\left(V_{gs} - V_t - V_{ds}\right)V_{ds}}{2} \, . \tag{18}$$

The resistance of the channel can be derived as

$$R_{ch} = \left(\frac{\delta I_{ds}}{\delta V_{ds}}\right)^{-1}\Big|_{V_{ds}=0} = \frac{\frac{L}{W}}{k_p\left(V_{gs} - V_t\right)} = \left(\frac{L}{W}\right)R_{proc} \quad , \tag{19}$$

where R_{proc} is the process resistance; depends only on the process and supply voltage ($V_{gs}=V_{DD}$ in this configuration (Fig. 5a)):

$$R_{proc} = \frac{1}{k_p\left(V_{DD} - V_t\right)} \, . \tag{20}$$

For a required decoupling capacitance the equivalent series resistance is determined as:

$$R_d = \frac{R}{N} = \frac{R_{ch}}{12N} = \frac{\left(\frac{L}{W}\right)R_{proc}}{12N} \, . \tag{21}$$

It is seen that with a given area (WL) the resistance depends on the MOS device aspect ratio (W/L). So, the aspect ratio can be determined from required equivalent series resistance, R_d.

Taking into account $N=C_d/C_{cell}=C_d/(c_{ox}WL)$, from (21) is derived:

$$R_d = \frac{L^2 c_{ox} R_{proc}}{12C_d} \, . \tag{22}$$

Or

$$L = \sqrt{\frac{12R_d C_d}{c_{ox} R_{proc}}} \quad (23)$$

As a design example, let's consider an IC I/O system that includes a 16-bit interface with a signal-to-power ratio of 1:1 (similar to the one shown in Fig. 1c); N_{sg}=16, N_{pg}=16. From the IC packaging it is given $N_{VDD\text{-}pin}$=$N_{VDD\text{-}pad}$=$N_{VSS\text{-}pin}$=$N_{VSS\text{-}pad}$=N_{pg}; the pin inductance and resistance, L_{pin}=3 *nH*, R_{pin}=0.6 *Ohm*; the bonding wire inductance and resistance, L_{pad}=1 *nH*, R_{pad}=0.2 *Ohm*. The equivalent inductance and resistance of the IC I/O system VDD/VSS rails, L_{VDD}=L_{VSS}=(L_{pin}+L_{pad})/N_{pg}=(3+1)/16 ==0.25 *nH*, R_{VDD}= R_{VSS} = =(R_{pin}+R_{pad})/N_{pg}=(0.6+0.2)/16 =0.05 *Ohm*. The equivalent inductance and resistance of the I/O power network, Ls=L_{VDD}+L_{VSS}=0.5 *nH*, Rs=R_{VDD}+R_{VSS}=0.1 *Ohm*. The I/O operation frequency is in the range of 100 *MHz* to 800 *MHz*, the supply voltage is V_s=1.8 *V*, the driver's signal output pad capacitive loading, C_s=5 *pF*. The main SI objectives are to keep supply rail voltage and driver delay variations within 10%.

The rough estimate of the needed decoupling capacitance is determined from (7) and (11):

$$\Delta V = V_{1s}\ C_1 L/(C_1 L + C_1 d)\,(1 + \exp(-\pi\zeta/\sqrt{(1-\zeta^2}\,)) \quad (24)$$

Restricting the voltage variation, ΔV at 10% level from the supply voltage of 1.8 *V* and taking into account that C_L=$N_{sg}C_s$=16·5=80 *pF*, and assuming the damping factor ζ=0.1, we get

$$1.8\frac{80}{80+C_d}\left(1+\exp\left(-0.\frac{1\pi}{\sqrt{1-0.1^2}}\right)\right) < 0.18$$

and C_d>1520 *pF*. We will take C_d=2000 *pF*. The buffer's delay variations and the VDD supply rail's voltage variations as functions from C_d obtained by Spice simulations are shown in Fig. 6a.

The voltage and delay variations depend basically on the decoupling capacitance. The damping factor, and hence voltage variations, also depend on the R_d. The optimum value of R_d can be determined by simulations. The VDD supply rail voltage variations as function from R_d when Cd=2 *nF* are shown in Fig. 6b. The minimum variations correspond to R_d=0.052 *Ohm*. To design a MOS decoupling capacitance with C_d=2 *nF* and R_d=0.052 *Ohm* the following technology and layout parameters are used: A_{cell}=10 μm^2, c_{ox}=6 $fF/\mu m^2$, k_p=2.132·10^{-4} A/V^2, V_t=0.566 *V*, V_{DD}=1.8 *V*.

The goal of the design is to determine L, W and N. Using formulas (20) and (23) the following calculations are performed: R_{proc}= (2.132·10^{-4}(1.8-0.566))$^{-1}$ =3.78 *kOhm*;

$L= (12\cdot0.052\cdot2\cdot10^{-9}/ (6\cdot10^{-15}\cdot3.78\cdot10^{3}))^{0.5} \cong 7$ *μm*; $W=A_{cell}/L=10/7\cong1.5$ *μm*; $C_{cell}=A_{cell}\cdot c_{ox}= =10\cdot6= 60$ *fF*; $N=C_d/C_{cell}=33000$; $A_d=NA_{cell}=0.33$ mm^2.

The calculated values of W and L must be consistent with technology design rules.

The characteristic impedance of the supply network, $\rho= \sqrt{L_s/C_d}=0.5$ *Ohm*. The corresponding damping factor is $\varsigma=(R_s+R_d)/2\rho=0.152$. As it can be seen the power network resonance frequency $F_r=(2\pi\sqrt{L_sC_d})^{-1}=159.2$ *MHz* is within the I/O operation frequency range.

The output buffer's input, output signals and supply rail voltage waveforms when all 16 output drivers are switched simultaneously are shown in Fig.7. The dependence of the supply rail voltage oscillation's magnitude on the operating frequency when $F_r=159.2$ *MHz*, VDD=1.8 *V* is shown in Fig. 8a. It can be seen that though the network resonance frequency is located within the operating frequency range, the voltage oscillation magnitude is within 10% margin ($\Delta V_{max}=0.1776$ *V*). The output buffer delay dependence on the operating frequency is shown in Fig. 8b; the delay variations are less than 6% (7 *ps*).

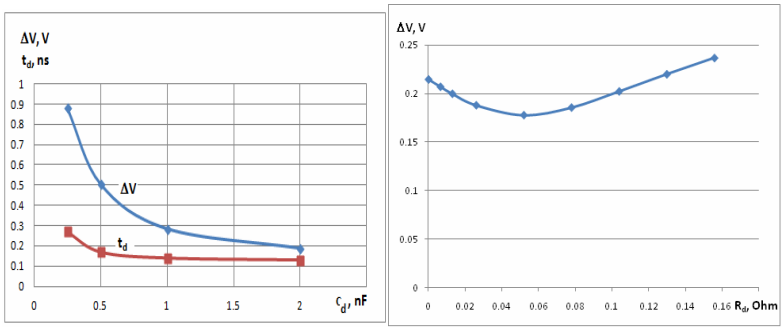


Fig. 6. (a) the buffer delay (t_d) and supply rail voltage (ΔV) variations from C_d, (b) the supply rail voltage variations from R_d

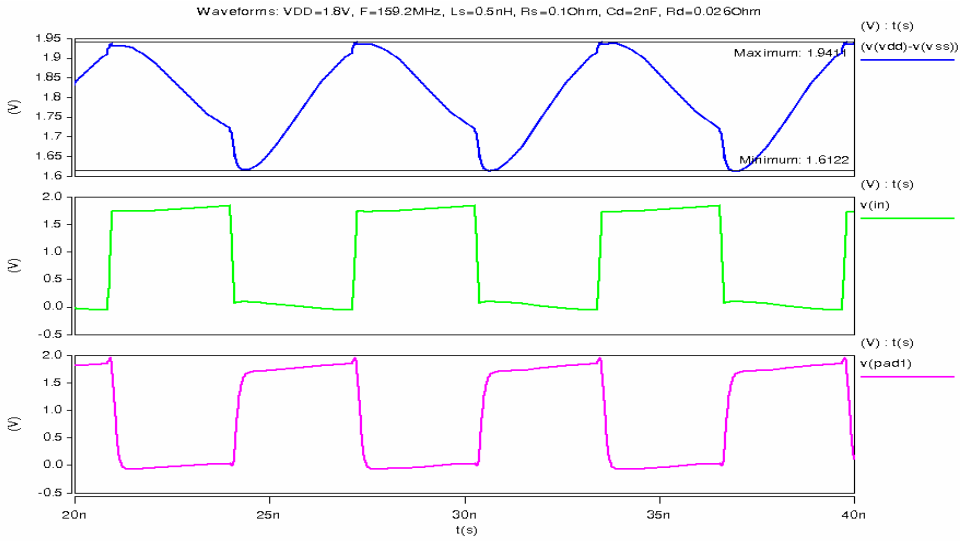


Fig. 7. Theoutput buffer's input, output signals and supply rail voltage waveforms

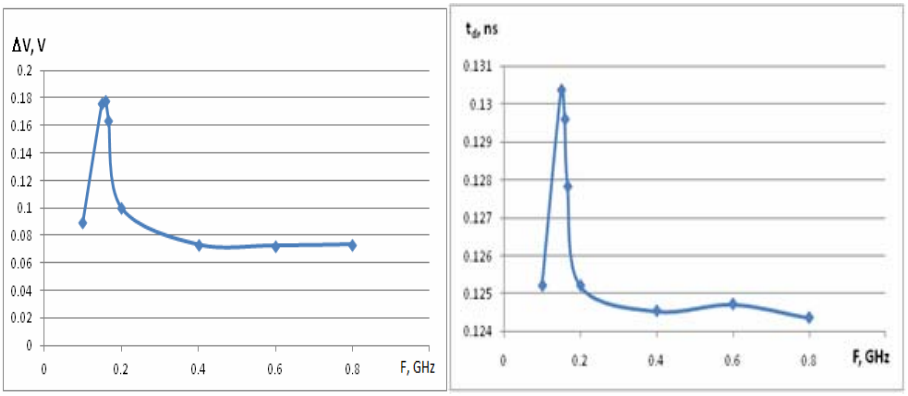


Fig. 8. The supply rail voltage (a) and the driver delay (b) variations from operating frequency

Summary. The output driver delay variations impact the data transfer system timing budget. The delay variations are a result of supply voltage variations due to the driver switching current. These variations can be reduced by using an on-die decoupling capacitances and by using multiple power/ground IO cells and package pins to reduce package inductances. It is shown also that the voltage and delay variations depend on the supply network damping factor which can be controlled by adjusting the network characteristic impedance and the MOS capacitor aspect ratio. The performed simulations confirm the basic concepts of this work.

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Վ.Շ. ՄԵԼԻՔՅԱՆ, Կ.Վ. ՄՈՎՍԻՍՅԱՆ

ԻՍ-ԵՐԻ ԱՐԱԳԱԳՈՐԾ ՄՈՒՏՔ-ԵԼՔ ԻՆՏԵՐՖԵՅՍԻ ՄՆՄԱՆ ՑԱՆՑԻ ՄՈԴԵԼԱՎՈՐՈՒՄ ԵՎ ՆԱԽԱԳԾՈՒՄ

ԿՄՕԿ ինտեգրալ սխեմաների (ԻՍ) սնման ցանցի մակաբույծ ինդուկտիվությունները սնման դողերում ստեղծում են աղմուկներ: Դրանք պատճառ են դառնում ազդանշանի տարածման հապաղման փոփխությունների և ջիտերի, որոնք փոքրացնում են ազդանշանի ժամանակային բյուջեն: Սա դառնում է կրիտիկական խնդիր հատկապես բարձրար ազդություններով ազդանշանների փոխանցման համակարգերում: Սնման ցանցի ինդուկտիվությունների ազդեցությունների փոխհատուցման և աղմուկների ճնշման համար մշակվել է ԻՍ-ի բյուրեղի վրա տեղադրված կապազերծող ունակությունների օգտագործման արդյունավետ եղանակ:

Առանցքային բառեր. ինտեգրալ սխեմա, մուտք-ելք համակարգ, էլեկտրասնուցման ցանց, ԻՍ-իվրակապազերծող ունակություն:

В.Ш. МЕЛИКЯН, К.В. МОВСИСЯН

МОДЕЛИРОВАНИЕ И ПРОЕКТИРОВАНИЕ СЕТИ ПИТАНИЯ ВЫСОКОСКОРОСТНОГО ИНТЕРФЕЙСА ВВОДА/ВЫВОДА ИС

Паразитные индуктивности сети питания КМОП интегральных схем (ИС) создают помехи в шинах питания. Они создают джиттер и изменяют задержки распространениясигнала, которые сокращают временной бюджет сигнала. Это становится критической проблемой, особенно в системах с высокой скоростью передачи данных. Разработанэффективный способ применения развязывающих емкостей, размещенных на кристалле ИС для компенсации влияния индуктивностей сети питания и подавления помех.

Ключевые слова: интегральная схема, система ввода-вывода, сеть электропитания, развязывающая емкость на ИС.