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ON-DIE CMOS TERMINATION RESISTOR FOR USB TRANSMITTER

Nowadays moving termination resistor from outside onto die is very beneficial from view of minimizing noises and saving cost. In this work new voltage-controlled CMOS active resistor aimed at on-chip termination is proposed. With current–voltage and resistance-voltage characteristics showing that this on-chip active termination resistor has good linearity across a wide range, and being suitable for analog impedance control technique using a feedback loop it is proven that it could be applied for USB transmitter. It is obtained that compared to other MOS only on-chip active resistors the proposed new resistor ensures about 20% of better linearity.

Keywords:universal serial bus, termination resistor, transmitter, on-die termination, linearity.

Introduction. Unlike low speed systems, in Universal Serial Bus(USB) [1] and other high-speed microelectronic applications, passive circuit elements (interconnect wires, cables, etc) can significantly affect the output signal (representing data, instructions, control information, etc) quality. The influences on signal integrity caused by the signal reflections and induced crosstalk voltage in these passive elements could be reduced by proper termination of transmission line [2]. Typically, a termination device is implemented as a resistor that is coupled between a signal line and a power supply node or ground and is co-located externally on the printed circuit board (PCB) [3]. Although external resistor provides a well matched termination, this approach has important disadvantages. The discrete external resistors consume valuable area on the board they are located, besides they are unable to prevent reflections resulting from the interconnect stub lines to which the buffer is connected. If the parasitic bonding inductance is represented as L_{bond} through which transmitter passes the current, then $\Delta V = L_{bond} \cdot di/dt$ voltage will be induced. The transmitted signal will be distorted and affected by the effect of bonding wire[4]. Instead of having the off-chip resistive termination, the termination located inside the semiconductor chips – On-Die Termination (ODT) helps to overcome these challenges, because ODT resistors have better performance on frequency response, also in case of off-chip resistors output signal has peaking on certain frequency caused by bonding wire which is absent for ODT[5]. There are different ways to construct resistors on a CMOS Integrated circuits(IC). Large variation in resistance (about 30%) prevents the use of passive on-chip (such as poly-silicon) resistors[6].On-chip laser

trimmed resistors are good but for trimming them it would be very time consuming and costly[7]. Another approach is to combine specifics of MOS transistors and polyresistor within one active resistor [8]. As mentioned the resistance of the voltage-controlled element can vary on process and temperature variations. In order to balance the obvious variations of processes and temperature, the digital control logic of impedance is widely used[9]. One of the disadvantages for this method is the step-like iterative adjustment. It can cause noise on the power buses if a large number of nodes are simultaneouslyswitched. It could also affect on data sending and reception. Another disadvantage is that the correctness of the digital on-chip resistor depends on the number of legs(resistors) used.

Forming on-chip resistors with only MOS transistors and analog techniques for their control is more beneficial because usage of only MOS components makes the design and implementation easier and cheaper, while the analog control technique helps to adjust impedance autonomously without causing extra noises on the busses. In [10,11] floating-gate CMOS resistors are proposed, but the usage of floating gate transistors and the fact that provided resistance could be very high(achieving several hundred $k\Omega$s) even in low voltage modes, make them not suitable for basic USB CMOS transmitter. In [12] an active resistor based on all pMOS structures is given, but in case of low voltages until about $0.6V$ it does not show good linearity[8] for USB target 45Ω termination impedance. Another disadvantage of this proposal is the absence of resistance adaptive control during circuit work time.

In this paper a new approach to form controllable termination resistors using MOS transistors located on the die aimed at USB and other high-speed systems as well is proposed. The novel schemes of both termination resistors and its analog control are presented. The resistor is made of MOS transistors with different input voltages. The termination resistor control scheme is based on usage of negative loop to adaptively control the transmitter impendence that is strong advantage compared to ways when the adjustment is performed iteratively step by step causing extra noises on supply and ground buses.

Proposed on-die resistor scheme. There are various ways of USB transmitter design. In [13] one separate single-endedtransmitter for each data line is proposed. Another approach is to use a transmitter based on differential pair with two outputs. But according to [1] 45Ω termination resistor should be placed at the end of each transmission line to ensure proper termination and prevent ringing.

The proposed new scheme of the ODT resistor is shown in Fig. 1. The impedance is made of n-type MOS transistors controlled by separate gate voltages.

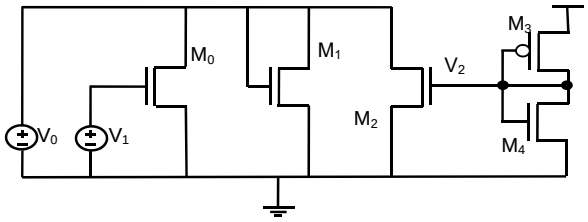

Fig. 1.ProposedMOS only active resistor

By changing the values of these input voltages correctly the necessary impedance value can be achieved.In case of V_1= 0, M_0 is closed. Thus, the overall current is formed by ones passing through M_1 and M_2. Because gate and drain of M_1 are shortened, $V_{GS1} = V_{DS}$ and if $V_{GS1}(V_{DS}) \geq V_{Thr}$ then it will operate in saturation region [6,14]. Otherwise if $V_{GS1}(V_{DS}) < V_{Thr}$ $I_1 = I_{DS1} = 0$. But when $V_{DS} < V_{GS2} - V_{Thr}$, M_2 operate in linear region[6,14]. Note, if$V_{GS2} >> V_{Thr}$, so $(V_{GS2} - V_{Thr})V_{DS} >> \frac{1}{2}V_{DS}^2$ approximation can be taken into account for linear region. And finally, for $V_{DS} < V_{Thr}$, the total current will be obtained as follows:

$$I = I_1 + I_2 = \mu_n C_{ox} \frac{W_2}{L_2}\left[(V_{GS2} - V_{Thr})V_{DS}\right]. \quad (1)$$

Hence the entire current is a linear function of V_{DS}. When $V_{Thr} < V_{DS} < V_{GS2} - V_{Thr}$ I_1 and I_2 are determined by equations characterizing saturation and linear regions of transistor correspondingly. And selecting the proper ratio of M_1 and M_2, the V_{DS}^2 member can be omitted for total I. So it can be assumed as a linear function from V_{DS} too.

In case of $V_{DS} \geq V_{GS2} - V_{Thr}$ M_2 is in deep saturation with some approximation $I_2 = \text{constant}$. From simulation results it is assumed that with V_{DS} rise, I_1 increases almost linearly. So the sum of these two currents behaves linearly depending on V_0 as well.

Termination resistor control scheme. The on-chip transmitter termination scheme is shown in Fig. 2. It uses a negative feedback loop of the two-stage differential amplifier to adaptively control the transmitter impedance R_1, R_2 through an identical MOS-only reference resistor R_{ref}.

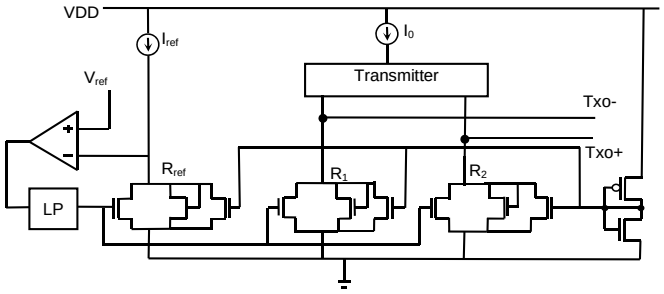

Fig. 2.Terminate resistor control scheme

Using I_{ref}, fixed current the value of the resistance can be determined by the voltage drop on R_{ref}. This voltage drop is compared with V_{ref}. With the help of the comparator using negative feedback loop, the output impedance of the transmitter will be changedto the value given in (2):

$$R = R_1 = R_2 = R_{ref} = \frac{V_{ref}}{I_{ref}}. \tag{2}$$

The varying range of the ODT resistance can be expressed as a function of operational amplifier gain *A*:

$$\frac{1-\frac{1}{A}}{1+\frac{1}{A}} < \frac{R}{R_{ref}} < \frac{1+\frac{1}{A}}{1-\frac{1}{A}}. \tag{3}$$

This result shows that the percentage error $(R - R_{ref}) / R_{ref}$ is proportional to 1/A. Therefore, a high open-loop gain is required in order to better match the reference resistor. For example, when A = 200, from (3) yields that targeted resistance will be within 1% or reference impedance. In Fig. 2 LP is a low pass filter for avoiding oscillations in the feedback loop.The basic RC structure can be chosen for that purpose. In the compensation, open-loop small-signal gain is approximated as:

$$\frac{v_0}{v_i} \approx \frac{g_{m1}r_1}{(1+s(r_1 \parallel R_C)C_1)} \frac{g_{m2}r_2}{(1+sr_2C_2)} \frac{g_{m3}r_3}{(1+sr_3C_3)} \frac{1}{[1+s(R_c+r_1)(1+g_{m2}r_2)C_C]}, \tag{4}$$

where $r_1(g_{m1})$ and $r_2(g_{m2})$ are small-signal (transconductance) for the differential input stage and the second stage of the operational amplifier, respectively, $r_3(g_{m3})$ is the smallsignal equivalent transconductance of output stage, and $r_1||R_C = r_1R_C/(r_1+R_C)$.

To evaluate the correct work of proposed resistor in low and full speed modes of USB, the transmitter circuit proposed in [13] was used. Two single ended transmitters were connected to each data line. The common structure of the used transmitter is shown in the Fig. 3.

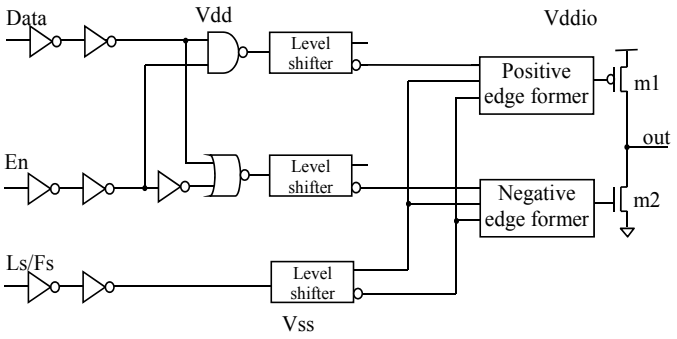

Fig. 3.USB transmitter used

Results. To get characteristics of the proposed on-die resistor, Synopsys HSPICE tool[15] and SAED 90*nm* library[16] were used. Here the behavior of resistor and simulation results in case of voltage parameters' and transistor sizeschanges are discussed.

It was shown above that if the proper aspect ratio of M_1 and M_2 are selected, the total current of MOS-only resistor is approximately a linear function from V_0 at whole change interval. The got I-V characteristic for the resistor circuit with current components passing through each transistor is shown in Fig.4.

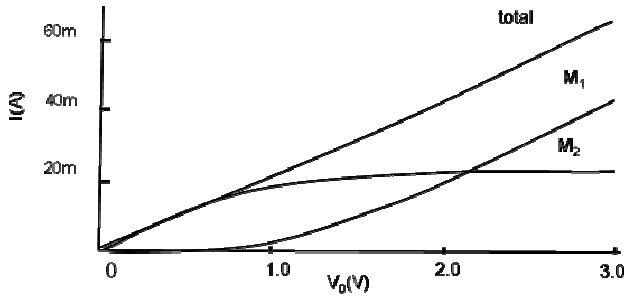

Fig. 4.The I-V curves of presented resistor, separate M_1 and M_2 transistors

Impedance of the resistor can be modified withV_1 change. If change V_1 as a parameter within the range 0 to 3*V*, the group of *I-V* curves will be get. When V_1 is smaller than threshold voltage $I_0 \approx 0$. With V_1 rise (1…3*V*), M_0 becomes open and the current passing through it will increase. Hence, the total current flowing through resistor would also increase as is in Fig.4. So the MOS-only resistor can be controlled by V_1 parameter change.The dependence of resistor impendence from V_1 voltage change when V_0 and V_2 are fixed is given in Fig.5. M_0 becomes more open with V_1 rise, so total current increases causingthe resistance drop. On the other hand, the impedance of the proposed ODT resistor can be controlled by the aspect ratio of M_0. The dependence law is pretty similar to one described in Fig.5.

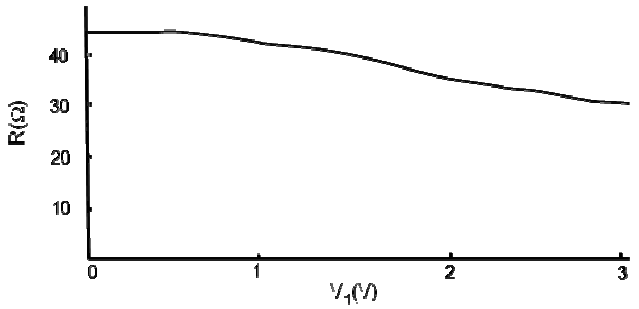

Fig. 5.The impedance of MOS-only resistor as a function of V_1

Increasing W/L parameter of M0 transistor, the impedance of resistor goes low. So the impedance of MOS-only resistor can easily be adjusted by means of changing the value of the aspect ratio of M0 as well as value of V1.

Transmitter's output resistive impedance characteristics for low and full speed modes obtained by simulation using the proposed ODT resistor for outputs logical '0' and '1' are shown in Fig.6.

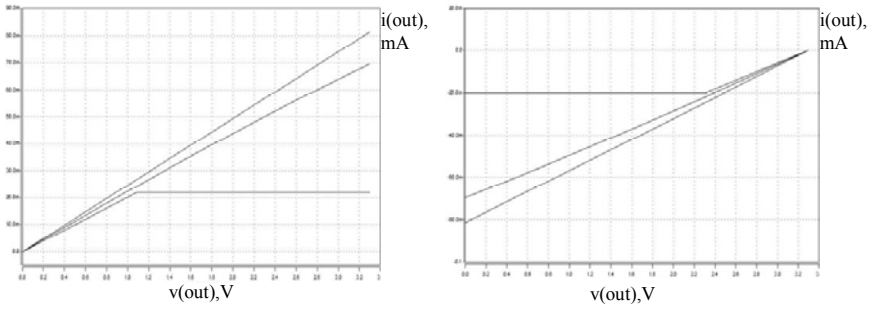

Fig. 6.Transmitter's output impedance for logic '0' and '1'

In Table the simulation measurements performed for three process and temperature variation cases (typical, fast, and slow as represented by TT, FF, and SS) are presented. Numbers and results in Fig. 6 show that deviation from nominal value of resistance is 5-7% that is within USB specification requirements [1].

Table

Resistance values for process and temperature variation cases

	-3σ	Mean	3σ	Deviation from 45Ω
TT	42.75Ω	45.24Ω	47.73Ω	-5.0 / 6.1 %
FF	42.91Ω	45.52Ω	48.13Ω	-4.6 / 6.9 %
SS	43.1Ω	45.73Ω	48.36Ω	-4.2 / 7.4 %

Compared to the CMOS active resistor described in [12], received I-V characteristics and simulation results for different corner cases of proposed ODT resistor has better linearity in case of lower voltages and is able to be adaptively controlled by discussed above control scheme which makes the proposed ODT resistor fully acceptable for USB. The [12] does not have means for adaptive control of impedance and as shown in [8] In case of structure from [12] there are about 30% deviations from 45Ω in case of lower voltages, but our proposed CMOS resistor shows very good linearity in the whole range.

Conclusion. New voltage-controlled CMOS resistor aimed at on-chip termination is proposed. Current–voltage characteristics show that this on-chip active termination resistor has good linearity across a wide range, and can be applied for USB transmitter. Simulations run proves that resistor impedance can vary within the range about 5…7% depending on temperature and process variations that is acceptable by USB specification. Presented on-chip CMOS resistor has about 20% better linearity compared to other PMOS active resistors in case of small voltages while using theanalog adaptive control method eliminates the noises that occur in case of digitally adjusted resistors. The on-chip resistor was aimed at 45Ω nominal value used in USB, but could be easily controlled with modifications of gate voltage and corresponding transistors ratios, hence be acceptable for other drivers with various termination impedance values(45…75Ω) as well.

REFERENCES

1. **Universal Serial Bus Specification**, Rev 3.0, 2009, www.usb.org.
2. **Gupta, R., Pillage, L.**Optimal Termination of Transmission lines Excluding Radiation // 31st Conference on Design Automation.- June 1994.- P. 640-645.
3. **Canright, R.** Practical Design for Controlled Impedance // Proc. of 41st Electronic Components and Technology Conference.- Aug. 2002.- P. 370-377.
4. **Lin, C., Tsai, C., Chen, C., Jou, S.** 4/2 PAM Serial link Transmitter with Tunable Pre-Emphasis // Proc of the International Symposium on Circuits and Systems.- May 2004.- Vol. 1.- P. 952-955.
5. **Lin, C., Chen, C., Jou, S.** Adaptive On-Die Termination Resistors for High-speed Transceiver // 2005 IEEE VLSI-TSA International Symposium on VLSI Design, Automation and Test.- Apr. 2005.- P. 96-99.
6. **Baker, R.** CMOS: circuit design, layout, and simulation. – Second Edition. - John Wiley & Sons, 2007.- 1074p.
7. Laser-Induced Resistance Fine Tuning of Integrated Polysilicon Thin-Film Resistors/ **E.Boulais, J. Fantoni, A. Chateauneuf et al** // IEEE Transactions on Electron Devices.- 2011.- Vol. 58 (2).- P. 572-575.
8. Patent No. US 7102200 B2. On-die termination resistor with analog compensation /**Y.Fan, J.Smith** //www.ip.com.- Sep. 2006.

9. **Koo, K., Seo, J., Kim, J.** A new Impedance Control Circuit for USB2.0 Transceiver //Proceedings of the 27th European Solid-State Circuits Conference.-2001.- P. 237-240.
10. **Özalevli, E.** Tunable Highly Linear Floating-Gate CMOS Resistor Using Common-Mode Linearization technique // IEEE Transactions on Circuits and Systems.- May 2008.- Vol. 55 (4).- P. 999-1010.
11. **Kumngern, M.** Voltage-controlled floating resistor using differential difference amplifier // International Conference on Electrical Engineering and Informatics(ICEEI).-July 2011.-P. 1-4.
12. **Griffin, J., Johnson, D.** Large signal active resistor output driver // 42nd Midwest Symposium on Circuits and Systems.- Aug. 1999.- Vol. 2.- P. 706-709.
13. **Aharonyan, V.** Low and full speed USB transmitter design using CMOS technology // International Scientific Conference “Designing systems on a chip: trends and challenges”, Oct. 2010.- Zelenograd, 2010.
14. **Sze, S., Kwok, K.** Physics of semiconductor devices.-Third Edition.- John Willey & Sons, 2007.-815p.
15. **HSPICE Simulation and Analysis User Guide**, 2010.
16. Synopsys Open Educational Design Kit: Capabilities, Deployment and Future/ **R.Goldman, K. Bartleson, T. Woodet al** // Proceedings of the International Conference on Microelectronic Systems Education: San Francisco, USA, July 2009.- P. 45-48.

Synopsys Armenia CJSC. The material is received 07.02.2011.

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ՆԵՐԲՅՈՒՐԵՂԱՅԻՆ ՓՈԽԱՆՋԱՏՄԱՆ ԿՄՕԿՌԵԶԻՍՏՈՐ ՀՀԴ ՀԱՂՈՐԴՉԻՀԱՄԱՐ

Ներկայումս փոխանջատման ռեզիստորի տեղակայումը բյուրեղի վրա օգնում է նվազագույնի հասցնել ելքային ազդանշանի վրա ազդող աղմուկները և տնտեսելարտադրման ծախսերը: Առաջարկված է նորն երբյուրեղային փոխանջատման ԿՄՕԿ ակտիվ ռեզիստոր: Մոդելավորման արդյունքում ստացված հոսանք-լարում, դիմադրություն-լարում կախումնեբի միջոցով ցույց է տրված, որ առաջարկվող ռեզիստորն ունի լավ գծայնություն լարման փոփոխման թույլատրելի միջակայքում և, ղեկավարվելով անալոգային եղանակով (փականային լարման միջոցով), կարող է կիրառվել հաջորդական համապիտանի դողի (ՀՀԴ) հաղորդչի ելքում: Ցույց է տրված, որ ներկայացվող ռեզիստորն ապահովում է մոտ 20% ավելի լավ գծայնություն՝ համեմատած այլ՝ միայն ՄՕԿ կառուցվածքների վրա հիմնված ներբյուրեղային ռեզիստորների հետ:

Առանցքային բառեր. Հաջորդական համապիտանիդող, հաղորդիչ, ներբյուրեղային փոխանջատման ռեզիստոր, ելքային ազդանշանի աճման արագություն:

В.Ш. МЕЛИКЯН, С.В. ГАВРИЛОВ, В.К. АГАРОНЯН, Н.К. АСЛАНЯН, А.С. ОГАННЕСЯН

ВНУТРИКРИСТАЛЬНЫЙ КМОП РЕЗИСТОР ТЕРМИНАЦИИ ДЛЯ ПЕРЕДАТЧИКА УНИВЕРСАЛЬНОЙ ПОСЛЕДОВАТЕЛЬНОЙ ШИНЫ

В современныхинтегральных схемах использованиевнутрикристальных резисторовыгоднос точки зренияминимизациишумовиэкономиисредств. В данной работепредлагается новый внутрикристальный и управляемыйнапряжением КМОП резистор терминации. С помощью вольт-амперных характеристик доказано, что предложенный резистор обладает хорошей линейностью в допускаемом диапазоне напряжения иможетприменяться дляпередатчика универсальной последовательной шины. Также показано, что предложенный резистор обладает лучшей линейностью (~20%) при низких напряжениях.

Ключевые слова: универсальная последовательная шина, передатчик, внутрикристальный резистор, терминация, скорость нарастания выходного сигнала.