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NEW METHOD OF RSD CORRECTION IN 1.5 BIT STRUCTURE PIPELINE ADC

A new method of redundant signed digit (RSD) correction for high-speed 1.5 bit pipeline analog-to-digital converters (ADCs), which will allow simplifying digital scheme is presented.

Keywords: pipeline ADC, RSD correction, carry-look-ahead adder, digital circuit.

In microelectronics a wide use of high-speed ADCs is observed in the last few years. Because pipeline ADCs are also part of high-speed ADCs, therefore demand for high-speed pipeline ADCs also increases. Pipeline ADCs [1, 2] are widely used because of two main advantages of these ADCs: high sample frequency (up to 400 Msps) and availability to provide high resolution (up to 16 bit). The block scheme of pipeline ADC is presented in Fig.1 [1].

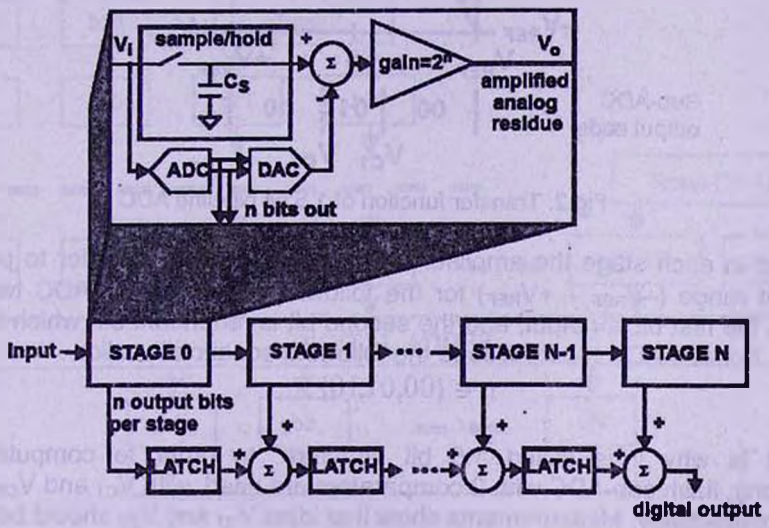

Fig.1. Block scheme of pipeline ADC

There are N similar stages, at the top of the picture the block scheme of the single stage is presented. The sample-and-hold (S/H) circuit in the first stage is used in order to sample the input (V_i). The S/H circuit in subsequent stages is used to sample the residue from the previous stage. This is the main advantage of pipeline ADCs because it allows each stage to start sampling a new value as soon as its residue is sampled by the following stage, and, thus, ADC can work at high-speed.

The residue in each stage is computed in the following way: the n bits output i computed by flash ADC, then it is converted to analog value by simple DAC, then tha the value is subtracted from the sampled input by an analog adder. The 2^n gain i used to amplify the residue for the following stage. That allows use similar stage throughout the ADC. When only a single bit is computed in each stage, the gain i equal to 2.

The principle of RSD correction is that in each stage not only output bits ar computed, but also redundant bits to be later used in the correction circuit. Th simplest RSD correction circuit for pipeline ADCs is 1.5 bit structure [1, 2]. Its transfe function is presented in Fig.2.

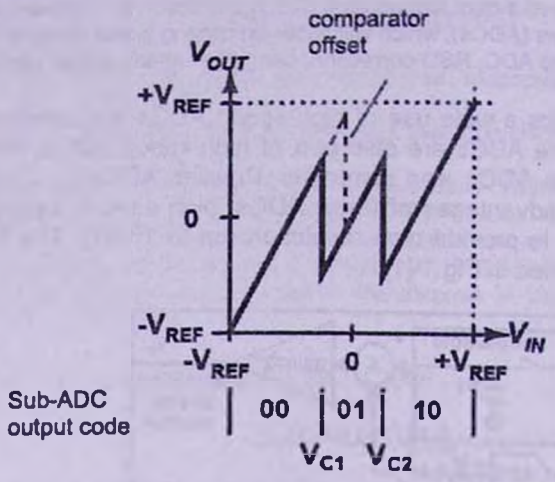

Fig.2. Transfer function of 1.5 bit pipeline ADC

Here, in each stage the amplifier with 2 gains is used, in order to provide th same input range ($-V_{REF} \div +V_{REF}$) for the following stage. In sub-ADC two bits ar computed, the first bit is output, and the second bit is redundant bit, which is used fo correction. For sub-ADC n output code the following equation is valid:

$$n \in \{00,01,10\}. \qquad (1$$

That is why it is called 1.5 bit structure. In order to compute these combinations, flash sub-ADC with 2 comparators are used, with V_{C1} and V_{C2} reference voltages, respectively. Measurements show that ideal V_{C1} and V_{C2} should be equal to

$$V_{C1} = -V_{REF}/4 \text{ and } V_{C2} = +V_{REF}/4. \qquad (2$$

In this case $\pm V_{REF}/4$ comparators offset will be corrected. The correction is done as follows: the second bit of each stage is added to the first bit of the following stage (Fig.3) [2].

stage1	b11	b10					
stage2		b21	b20				
...			...	...			
stage(N-2)				b(N-2)1	b(N-2)0		
+ stage(N-1)					b(N-1)1	b(N-1)0	
output	b1	b2	...	b(N-2)	b(N-1)	bN	

Fig.3. RSD correction in digital domain

The second bit of the last stage presents the least significant bit (LSB) with precision $\pm 0.5V_{REF}$ of the last stage (therefore the precision of ADS will be 0.5LSB). Thus, in order to obtain N bit digital output (N–1) stages are required.

The RSD scheme is generally implemented in the following way: output bits of each stage with shift registers are passed to the adder (Fig.4).

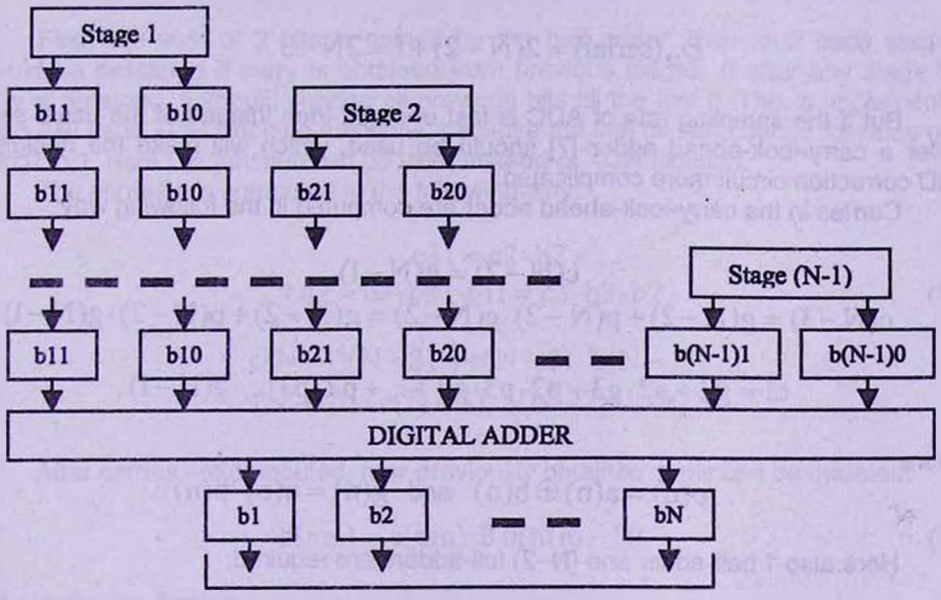

Fig.4. General scheme of RSD correction

In this case for N-bit resolution ADC the following number of registers will be required:

$$S(reg) = \left(\sum_{k=0}^{N-2}(2+2k)\right) + N = (N-1)\cdot N + N = N^2 \qquad (3)$$

Furthermore, to implement the usual serial adder 1 half-adder and (N–2) full adders are required. From [3, 4] for half-adder we can write

$$s(n) = a(n) \oplus b(n) \quad \text{and} \quad c(n) = a(n) \cdot b(n) \tag{4}$$

and for the full-adder

$$s(n) = a(n) \oplus b(n) \oplus c(n-1) \text{ and } c(n) = a(n) \cdot b(n) + a(n) \oplus b(n) \cdot c(n-1) \tag{5}$$

Assume that we have Ω basis, which includes the following basic Boolean functions: AND, OR and XOR. In this case we can compute the complexity of the presented serial adder with Ω basis [5, 6]:

$$S_{\Omega}(\text{serial}) = 5(N-2)+2 = 5N-8. \tag{6}$$

Now compute the depth of the serial adder with Ω basis:

$$D_{\Omega}(\text{serial}) = 2(N-2)+1 = 2N-3. \tag{7}$$

But if the sampling rate of ADC is fast enough, then instead of the usual serial adder a carry-look-ahead adder [7] should be used, which will make the design of RSD correction circuit more complicated.

Carries in the carry-look-ahead adder are computed in the following way:

$$\begin{gathered} c(N-2) = g(N-1), \\ c(N-3) = g(N-2) + p(N-2) \cdot c(N-2) = g(N-2) + p(N-2) \cdot g(N-1), \\ \ldots, \\ c1 = g2 + p2 \cdot g3 + p2 \cdot p3 \cdot g4 + \ldots + p2 \cdot p3 \cdot \ldots \cdot g(N-1), \end{gathered} \tag{8}$$

where

$$p(n) = a(n) \oplus b(n) \quad \text{and} \quad g(n) = a(n) \cdot b(n). \tag{9}$$

Here also 1 half-adder and (N–2) full-adders are required:

$$s(n) = a(n) \oplus b(n) \tag{10}$$

and

$$s(n) = a(n) \oplus b(n) \oplus c(n-1). \tag{11}$$

Now compute the complexity of the carry-look-ahead adder with Ω basis:

$$S_{\Omega}(\text{cla}) = \left(\sum_{k=0}^{N-4}(4+k)\right)+1+(N-1) = (N-2)(N+5)/2+1+(N-1) =$$

$$= (N^2+5N-10)/2 \tag{12}$$

and the depth is equal to

$$D_{\Omega}(\text{cla}) = 4. \tag{13}$$

The main disadvantage of such a structure is that a lot of registers are required. Furthermore, when serial adder is used, it is unable to provide high speed of adding, especially in high resolution pipeline ADCs, because the depth of the serial adder grows with resolution.

In the suggested scheme output codes are summed as soon as they are obtained. The suggested scheme is presented in Fig.5.

After each stage the output is obtained, MSB of the current stage is summed with LSB of the previous stage then updates it when in later stages the carry is obtained. Thus, the number of registers is reduced:

$$S(\text{reg\_new}) = (\sum_{k=0}^{N-2}(3+k)) - 1 + N = (N-1)(N+4)/2 - 1 + N =$$

$$= (N^2 + 5N - 6)/2. \tag{14}$$

First, the sum of 2 bits is gained by the half adder, then after each stage it should be redefined if carry is obtained from previous stages. If after any stage the carry is obtained, it should change all previous bits till the first 0. This is implemented using AND and XOR Boolean functions, because the first bit can change its value only from 0 to 1, here OR function can be used instead of XOR function.

The carries are computed in the following way:

$$\begin{gathered} c31 = c2 \cdot b2, \\ c42 = c3 \cdot b3;\ c41 = c3 \cdot b3 \cdot b2, \\ \ldots, \\ c(N-1)(N-3) = c(N-2) \cdot b(N-2);\ \ldots \\ c(N-1)1 = c(N-2) \cdot b(N-2) \cdot \ldots \cdot b2. \end{gathered} \tag{15}$$

After carries are computed, now previously obtained sums can be updated:

$$b(nm) = c(nm) \oplus b(n(m-1)) \tag{16}$$

and only for the first bit:

$$b(1m) = c(1m) + b(1(m-1)), \tag{17}$$

where $n \in [2, N-2]$ is the number of computed bits, $m \in [3, N-1]$ is the number of stages.

Again compute the complexity of the presented adder with Ω basis

$$S_{\Omega}(\text{adder\_new}) = \sum_{k=0}^{N-3}(3+2k) = N(N-2) = N^2 - 2N \tag{18}$$

the depth being equal to

$$D_{\Omega}(\text{adder\_new}) = 3. \quad (19$$

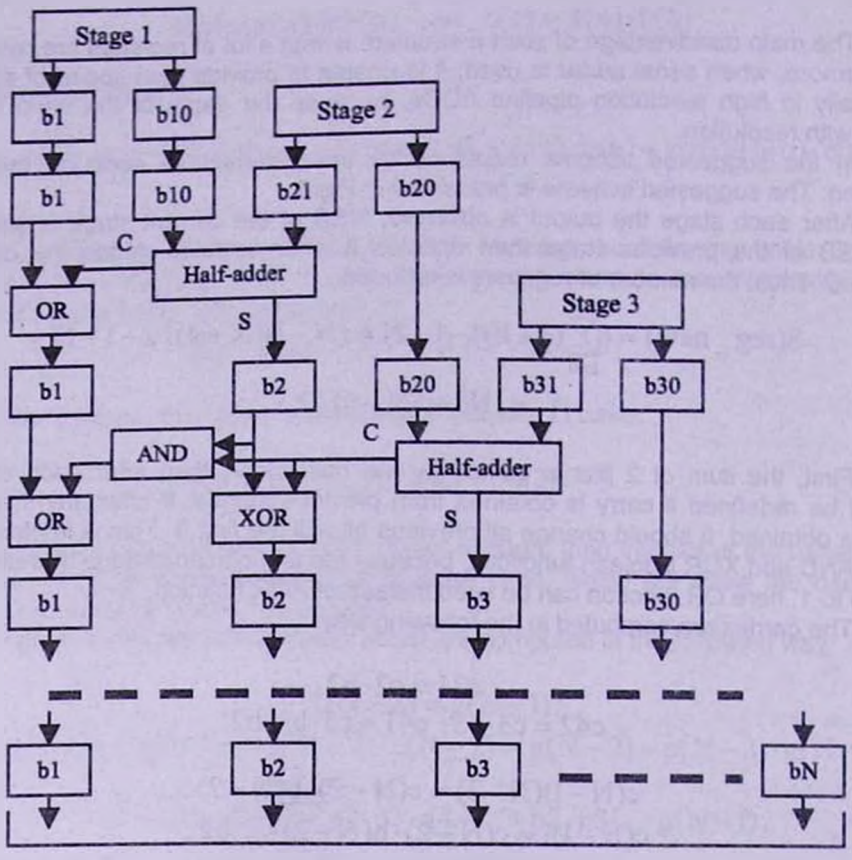

Fig.5. New scheme of RSD correction

Thus, with the presented structure the number of required registers is reduced in comparison with the general method, which is an appreciable advantage, because registers are considered complex digital cells. Furthermore, in comparison with the series adder, the new adder has more complexity but much less depth (note that the depth increases as the resolution of pipeline ADC increases). And finally, in comparison with the carry-look-ahead adder, the new adder has equivalent complexity and less depth.

In order to define advantages of new structure obviously, compute the number of registers for both new and general methods, as well complexities of both new and carry-look-ahead adders, for 6-10 bit resolution pipeline ADCs.

The number of registers can be computed from (3) and (14) equations. In Fig.6 the number of registers' graphs for new and general methods for 6-10 bit resolutions pipeline ADCs is presented.

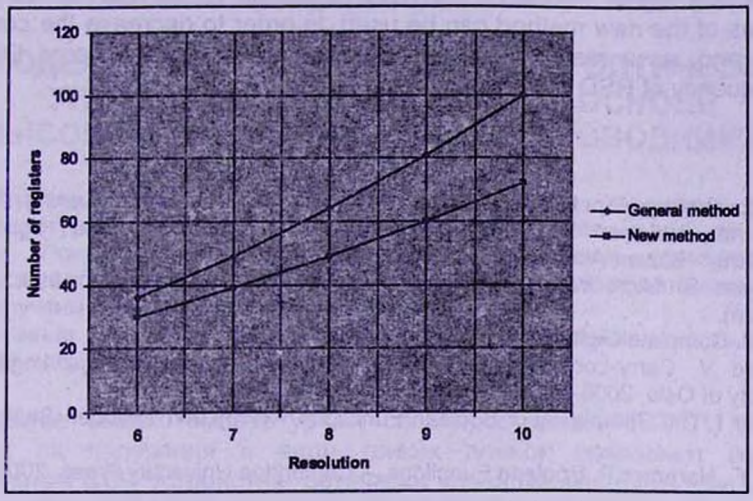

Fig.6. The number of registers and resolution dependences

The complexities can be computed from (12) and (18) equations. In Fig.7 the complexities for new and carry-look-ahead adders for 6-10 bit resolutions pipeline ADCs are presented.

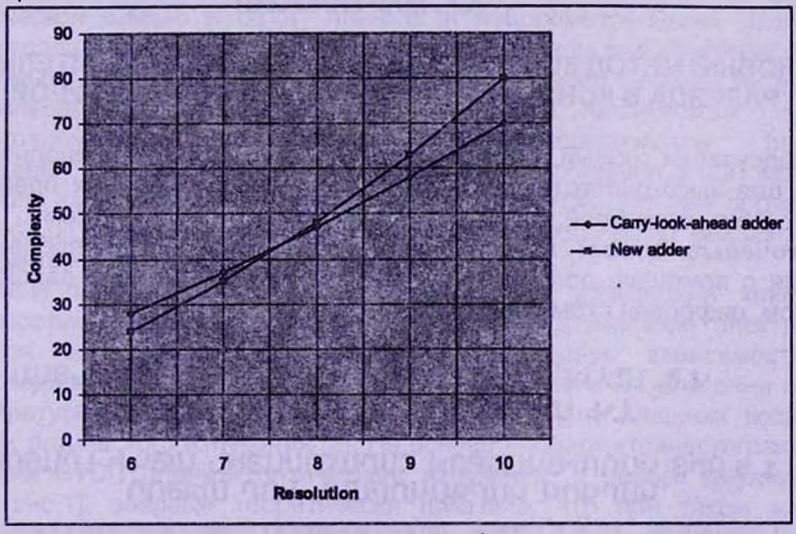

Fig.7. Complexity and resolution dependences

From Fig.6 it is obvious that the number of registers reduces as much as resolution of pipeline ADC increases in the new method. At the same time adder complexity for low resolutions (6 and 7 bits) is low in comparison with the carry-look-

ahead adder in the new method, but it increases as resolution increases starting from 8 bits. But note that the number of registers in the general method increases much faster. At the same time the depth of the adder in the new method is smaller, which allows providing higher frequency for RSD correction circuit. Furthermore, different modifications of the new method can be used, in order to decrease the complexity of the circuit, and, as a result, to increase the depth, but at the same time provide enough frequency of RSD correction circuit.

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НОВЫЙ МЕТОД КОРРЕКЦИИ С ПОМОЩЬЮ ДОПОЛНИТЕЛЬНОГО РАЗРЯДА В КОНВЕЙЕРНЫХ АЦП С 1.5 БИТ СТРУКТУРОЙ

Представлен новый метод коррекции с помощью дополнительного разряда для высокочастотных конвейерных аналого-цифровых преобразователей с 1.5 бит структурой, что позволит упростить цифровую схему.

Ключевые слова: конвейерный аналого-цифровой преобразователь, коррекция с помощью дополнительного разряда, сумматор с параллельным переносом, цифровая схема.

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1.5 ԲԻՏ ԿԱՌՈՒՑՎԱԾՔՈՎ ՀԱՐԱՀՈՍԱՅԻՆ ԱԹԿ-Ի ԼՐԱՑՈՒՑԻՉ ԿԱՐԳՈՎ ԿԱՐԳԱՎՈՐՄԱՆ ՆՈՐ ՄԵԹՈԴ

Ներկայացված է 1,5 բիտ կառուցվածքով արագագործ հարահոսային անալոգա-թվանշանային կերպափոխիչների (ԱԹԿ) համար լրացուցիչ կարգով (ԼԿ) կարգավորման նոր մեթոդ, ինչը հնարավորություն կստեղծի պարզեցնելու թվային սխեման:

Առանցքային բառեր. հարահոսային ԱԹԿ, ԼԿ կարգավորում, զուգահեռ փոխանցումով գումարիչ, թվային սխեմա: