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UDC 621.3.049.77 **MICROELECTRONICS**

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A VOLTAGE - CONTROLLED OSCILLATOR AIMED AT REDUCING OPERATIONAL FAILURES AND RESISTANT TO VARIATIONS OF THE PROCESS, VOLTAGE AND TEMPERATURE

A voltage - controlled oscillator resistant to variations of the process, voltage and temperature is presented. The proposed method allows to detect and compensate the control voltage value deviations due to the process variations. The system stabilizes the voltage value during the Voltage-Controlled Oscillator (VCO) operation and therefore improves the circuit reliability and reduces the parameter variability. The mixed-signal circuit is detecting the changes in input reference voltage values, and based on the deviation direction, reduces its impact. The compensation system is adjusting the reference signal value at the VCO operation start. The proposed system is compatible for most high-speed data links and is implemented with a standard VCO block.

Keywords: integrated circuit (IC), process voltage vemperature variations (PVT variations), voltage-controlled oscillator (VCO)

Introduction. With the rapid scaling of transistor sizes in modern ICs, it becomes harder to maintain wafer manufacturing and yield tests. With moving towards more advanced technological nodes, the layout density, as well as the number of interconnects vias and physical layers increase, which leads to further wiring congestions and therefore additional issues during IC manufacturing. The mentioned phenomenon leads to a longer yield ramp duration and cost inefficiency. In order to avoid additional faults and functional fails during wafer test process, it becomes important to create reliable structures, that will be resistant to external and internal variations. This will help to increase the wafer yield and reduce the ramp time. For calculating the yield and determining the faulty circuits, a full structural and functional testing is performed [1].

Fig. 1 presents the comparison of the yield ramp for the latest technological nodes.

Structures in the ICs become more sensitive to the process, temperature, and voltage (PVT) variations, therefore parameter-related functional tests become more impactful during the wafer testing process. In order to get higher yield after testing, several PVT variation detection and calibration methods are introduced. Those methods are implemented in various mixed-signal blocks such as Current Sources, High-Speed Serial Links, Voltage Controlled Ring Oscillators (ring VCO), etc.

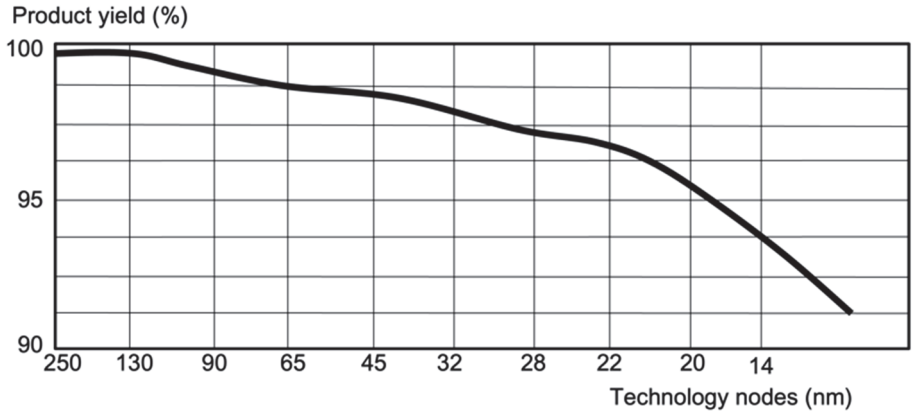


Fig. 1. The final yield (%) depending on the technology node

Voltage-controlled ring oscillators are widely used in such systems as, phase-locked loops (PLL), function generators, or can serve as a quantizer in analog-to-digital converter (ADC). A VCO-based quantizer has a non-ignorable nonlinearity due to its nonlinear tuning curve, and the quantizer performance varies drastically with the process, voltage, temperature (PVT) deviations, which degrade overall performance [2]. VCO calibration should maintain the VCO gain and tuning range in accordance with PVT variations. In the compensation technique introduced in [3], at the beginning of the calibration process, VCO starts to oscillate with a preset tuning code, and the f_0 and K_{vco} are being calculated and compared with their ideal values. Once the deviation between ideal and real values is detected, the tuning code is increased or decreased based on the deviation direction. The process is repeated if the system can capture a deviation between two signals. In the proposed system two transistor arrays are added in order to gain control over VCO gain and frequency. In the presented paper, the ring VCO is realized with 7-stage delay buffers. Each stage consists of two cross-coupling inverters with a tail-current source. In standard solutions the input of the NMOS transistor of current source is being connected to some bias voltage. With this approach, the frequency deviation from the worst to best case was fixed from 400 *MHz* to about 100 *MHz*. This means that the system will remain stable during its operation. The problem with the system is that it compares the current values with the ideal ones, and those can be deviated as well, besides the system uses a large number of operational blocks, which occupy a larger area and can lead to a yield loss as well.

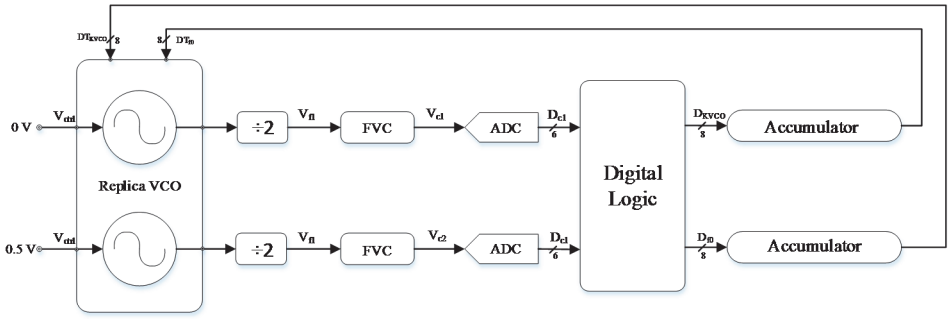


Fig. 2. The block diagram of the calibration system

Fig. 2 presents the diagram of PVT detection system, which consists of replica VCO, frequency divider, frequency- to-voltage converter and digital logic. In [4], the process variation is determined based on the Vthn and Vthp difference related to VDD/2. In order to compare the p-type and n-type MOS transistors' threshold values, a process relative signal generator (PRSG) is used. Figure 3 presents the diagram of the proposed system.

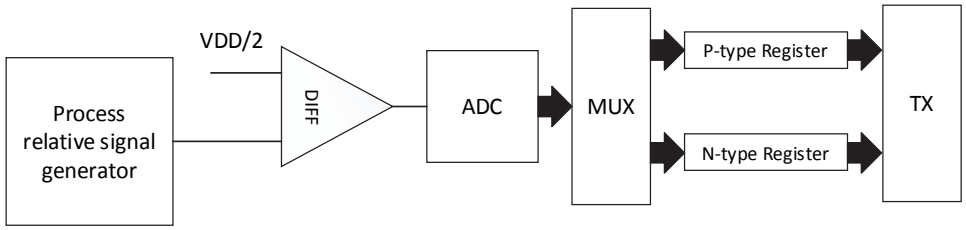


Fig. 3. The structure of the process compensation method

Without the PVT compensation circuit, the rise and fall times of variations are near 40%. After adding the PVT compensation circuit, the deviation between the worst- and best-case scenarios is ~4%. The presented system compensates the transition times of deviated processes. This means that by using a PVT compensation circuit, it is possible to increase the IC yield, by implementing this in systems such as current sources, or voltage-controlled oscillators (VCO).

The problem description. In modern integrated circuits, it is required to generate a signal with frequency, that is based on the voltage value of some other signal [5]. The main goal during the design process of such a structure is to build a system with high accuracy, stability and reliability. An example of such a system is the voltage-controlled oscillators (VCO). The functionality of these devices is to generate an output signal with frequency, that is based on the input signal voltage value. VCOs are used in phase-locked loops (PLL), system clock generators. VCO generates a signal with various frequencies based on the tuning voltage of the system.

Due to PVT variation, the controllability of output frequency can vary, which leads to an error in the systems that use the generated frequency for their operations.

In recent years several solutions were purposed in order to overcome the mentioned VCO nonlinearity issues. Nevertheless, those solutions are not addressing the issues related to PVT distortions. Those are mostly based on solving the nonlinearity issues in the VCO by implementing a digital calibration mechanism. Figure 4 shows one of the delay cells of the VCO. The delay cell consists of two cross-coupling inverters with a tail-current source.

One of the most important parameters for VCO is the frequency variations for different PVT corners. Based on the designed systems those variations can reach up to 50% in the worst- and best-case scenarios. The variations are causing a functional test failures, and therefore a significant yield loss. Based on the number of blocks that are connected to VCO, its deviations can lead to a significant yield loss. In order to avoid such behavior, the VCO system can be self-calibrated based on PVT variations. To do so, it is required to have a PVT monitoring system. The system should capture the variations and process the calibration.

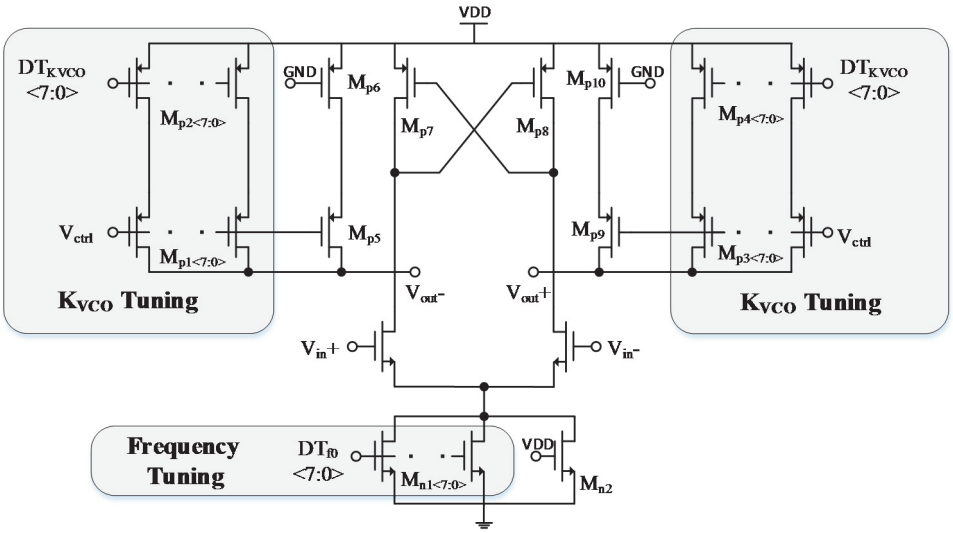


Fig. 4. The delay cell of VCO with additional control tuners

The proposed solution. Fig. 5 presents a PVT compensation system which is based on the system introduced in [4].

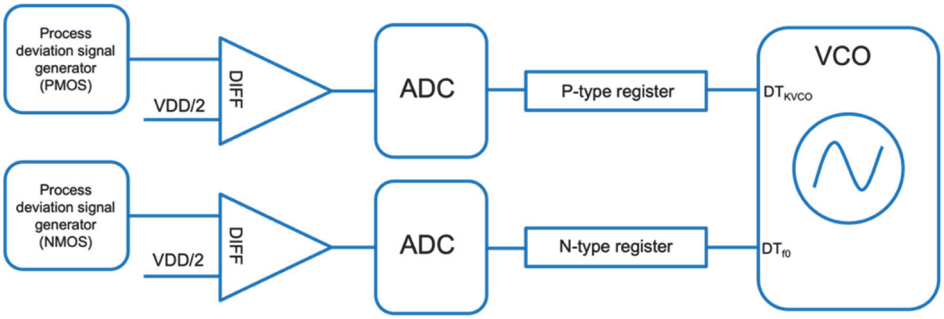
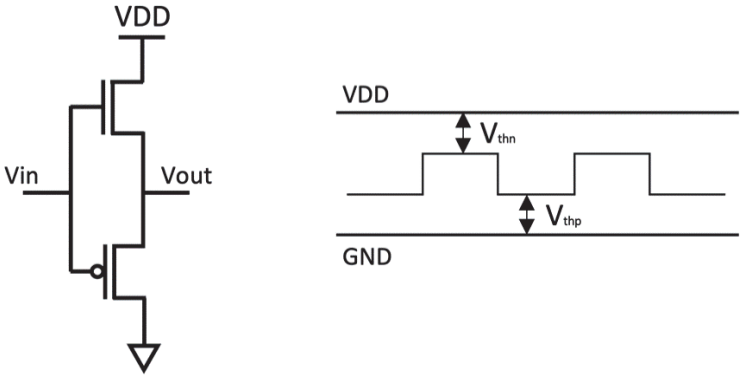


Fig. 5. A PVT detection and calibration system for VCO

In the proposed system, the variation detection for PMOS and NMOS transistors is separated in order to achieve continuous deviation capturing and compensation during the system's entire operation. The process deviation signal generator is two transistors buffer with NMOS transistor connected to VDD and PMOS to GND (Fig. 6) [4]. By doing so, the output of the buffer is going to have logic "1" degraded by Vth, and the logic "0" will be higher by Vth. The output of each PDSG is being fed to each of the differential amplifiers' inputs. The other inputs of differential amplifiers are connected to a VDD/2 signal, therefore the outputs should be (VDD-Vthp) and (VDD-Vthn) for PMOS and NMOS transistors respectively. One of the most important part during the design is the creation of the PDSG in such a manner that it would be an exact replica to the arrays that are connected to VCO control blocks.

Fig. 6 presents the process-relative signal generator block (a simple buffer), whose output voltage for logical "1" and "0" is considered as "weak", since the NMOS and PMOS transistors are connected to VDD and GND respectively.



a) b)

Fig. 6. a- Process-relative signal generator, b- Process detection

Ideally, the difference between two signals should be 0, but due to PVT variation, the values are going to vary. In order to compensate the variations, the output signal of the differential amplifier is connected to ADC, which digitalizes the signal and connects it to the corresponding p-type and n-type registers. Those registers are storing the control value for PMOS and NMOS transistors arrays. The control voltages of the VCO are connected to the transistor arrays of the respective type. Figure 7 presents the VCO systems' delay cell with additional transistor arrays connected to its control voltage inputs.

P-type register controls the PMOS transistors' array. The p-type transistors' array controls the number of PMOS transistors connected to the Vctrl of VCO. Those transistors affect the Kvco gain value, therefore by tuning the number of transistors that are turned-on, it will be possible to keep Kvco value stable during the system operation. The same approach was used to tune the n-type transistors' array. Mn1 transistor controls the current source of the delay cell and therefore determines the tuning range of the VCO.

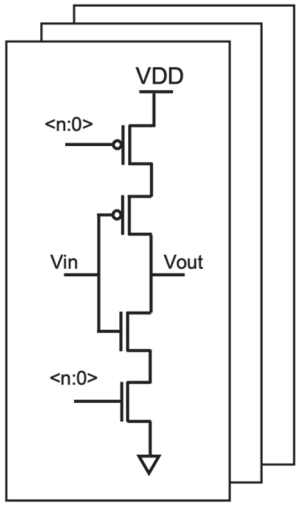


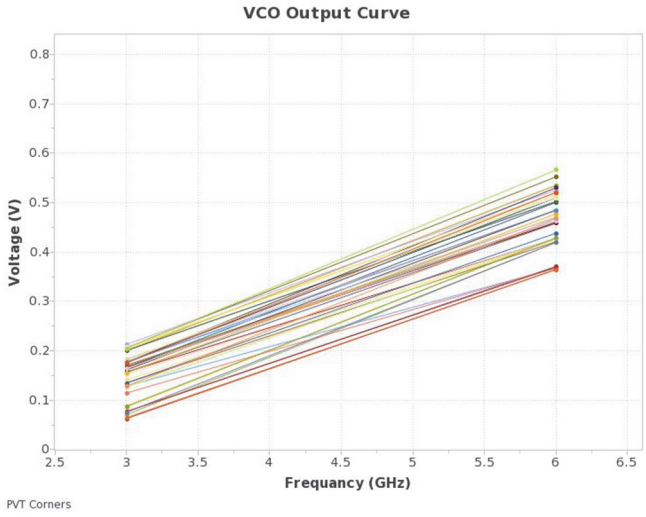
Fig. 7. The VCO cell of the purposed system

The simulation results. The simulation results for 80 PVT corners are presented. HSPICE [6] circuit level simulator is used to obtain results for the mentioned cases, including SS (slow-slow), TT (typical-typical) and FF (fast-fast) corners with temperature and voltage variations for 14 *nm* CMOS technology. The PVT variation detection and compensation system is compatible for most of analog and mixed-signal circuits and is tested on a standard VCO block.

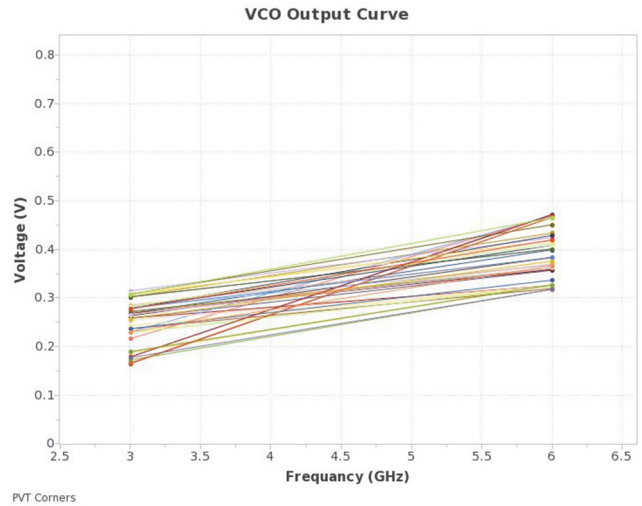
During the simulation process, the voltage values were found to achieve a signal with 3 *GHz* and 6 *GHz* frequencies at the output of the VCO system. In

order to simulate VCO system control voltage, a 10-bit ADC is used. The control voltage changes until the moment when the desired frequency is captured in the output system. Depending on the PVT variation, the Vctrl range for a particular frequency can be different.

Fig. 8 presents the VCO output curve before and after the PVT compensation system implementation.



a)



b)

Fig.8. Voltage-frequency curve: a- before PVT compensation, b-after PVT compensation

According to simulation results, the Vctrl variation for 3 was ~0.17 *V* and for 6 *GHz* it was ~0.23 *V* before PVT compensation. After the PVT compensation, the variations were ~0.13 *V* and ~0.15 *V* respectively. This means that the variations impact was reduced approximately by 30%. The simulation results for typical cases before and after calibration are summarized in Tables 1 and 2 accordingly. The results show that the voltage variations drastically change after a PVT detection and compensation system is applied to VCO.

Table 1

Simulation results before compensation

	FF	TT	SS
3 *GHz*	0.18 *V*	0.24 *V*	0.31 *V*
6 *GHz*	0.31 *V*	0.38 *V*	0.46 *V*

Table 2

Simulation results after compensation

	FF	TT	SS
3 *GHz*	0.18 *V*	0.24 *V*	0.31 *V*
6 *GHz*	0.31 *V*	0.38 *V*	0.46 *V*

It is important to mention the area increase of the entire system as its main disadvantage. In order to add the controllability over each VCO buffer, PMOS and NMOS transistors should be added into them. Besides, in order to get continuous variation detection and calibration, 2 ADC blocks and 2 differential amplifiers should be added. Considering these changes, the entire area of the system is increased by 10-15%.

Conclusion. A PVT tolerant VCO system is proposed in this paper. As the results show, the proposed system reduces the variations up to 30%, which makes the system more sustainable to them. This will reduce the operational failures and improve the testing results after IC production, thus improving the yield value and speed up the yield ramp process. The disadvantage of the proposed system is the 10-15% area increase, whose impact on total failures will depend on the manufacturing process. The proposed system is compatible for most of data links and is tested on a standard VCO block.

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Հ.Վ. ԳՈՒՄՐՈՅԱՆ

ԿԱՅՈՒՆ ԼԱՐՄԱՄԲ ԿԱՌԱՎԱՐՎՈՂ ՀԱՃԱԽՈՒԹՅՈՒՆՆԵՐԻ ԳԵՆԵՐԱՏՈՐ՝ ԿՈՂՄՈՐՈՇՎԱԾ ԱՇԽԱՏԱՆՔԱՅԻՆ ԽԱՓԱՆՈՒՄՆԵՐԻ ՆՎԱԶԵՑՄԱՆԸ

Ներկայացված է գործընթացի լարման և ջերմաստիճանի (ԳԼՋ) շեղումների նկատմամբ կայուն լարմամբ ղեկավարվող գեներատոր (ԼՂԳ)։ Առաջակվող համակարգը հնարավորություն է տալիս հայտնաբերել և կոմպենսացնել ԳԼՋ շեղումների հետևանքով առաջացող կառավարող լարման արժեքների տատանումները։ Համակարգը կայունացնում է ԼՂԳ-ում լարման արժեքը և, հետևաբար, բարձրացնում է համակարգի հուսալիությունը և նվազեցնում պարամետրերի փոփոխությունները։ Խառը ազդանշանային սխեման հայտնաբերում է մուտքային հենակային լարման արժեքների փոփոխությունը և կախված դրա ուղղությունից՝ շտկում այն։ Լարման ուղղման գործընթացը սկսվում է ԼՂԳ-ի աշխատանքի սկզբում։ Առաջարկվող համակարգը կիրառելի է տվյալների փոխանակման արագագործ հանգույցներում և իրագործված է ստանդարտ ԼՂԳ համակարգի հիման վրա։

Առանցքային բառեր. ինտեգրալ սխեմա (ԻՍ), գործընթացի լարման և ջերմաստիճանի շեղումներ (ԳԼՋ շեղումներ), լարմամբ ղեկավարվող գեներատոր (ԼՂԳ)։

Р.В. ГУМРОЯН

ГЕНЕРАТОР ЧАСТОТ, УПРАВЛЯЕМЫЙ НАПРЯЖЕНИЕМ, НАЦЕЛЕННЫЙ НА СНИЖЕНИЕ РАБОЧИХ СБОЕВ И УСТОЙЧИВЫЙ К ВАРИАЦИЯМ ПРОЦЕССА НАПРЯЖЕНИЯ И ТЕМПЕРАТУРЫ

Предлагается устойчивый к вариациям процесса, температуры и напряжения генератор частот, управляемый напряжением. Представленная система дает возможность обнаружить и компенсировать изменения управляющего напряжения, вызванные вариациями. Интегральная схема со смешанным сигналом обнаруживает изменения входного сигнала и в зависимости от направления изменения компенсирует его. Процесс исправления и стабилизации напряжения выполняется в самом начале работы генератора. Система сопоставима с большинством высокоскоростных систем передачи данных и реализована для стандартного генератора частот, управляемого напряжением.

Ключевые слова: интегральная схема; вариации процесса, температуры и напряжения; генератор частот, управляемый напряжением.