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A NOVEL PULSE SYNCHRONIZER DESIGN WITH THE PROPOSED SYNC CELL MODEL

The behavioral model of previously proposed novel sync cell and pulse synchronizer design is presented The behavioral model is developed using Verilog HDL. Pulse synchronizer designed is based on the sync cell model and verified with X-injection during the simulations to identify failures in early design stages. The use of the designed synchronizers reduces overall area and the clock cycle required for synchronization which improves the performance of the overall system where they are used.

Keywords: clock domain crossing (CDC), synchronizer, metastability.

Introduction. Modern System on Chip (SoC) designs have multiple high frequency clocks due to high interface requirements. Inaccurate clock domain crossing (CDC) handling in early design stage can bring critical issues to system inoperability. CDC issues occur while it is required to transfer data or control signals from one clock domain to another. Unsynchronized data or control signals can cause destination flops to get into metastable state. Metastability is caused by setup and hold violations, which occur because of timing issues, different clock phases at destination and source domain, etc.

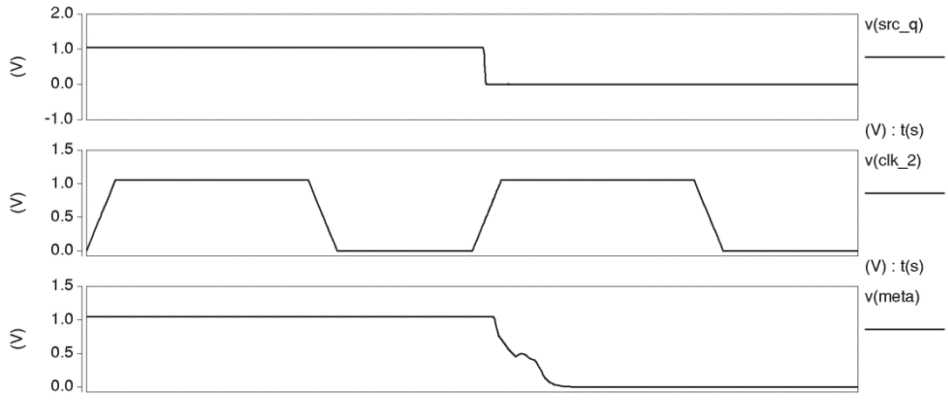

Fig. 1. A metastability simulation example

Metastability in such cases stands for state where the output of the flop is unknown and unpredictable. At the end of metastability, the output of the flip flop

settles down to either logical '1' or '0'. An example of metastability is shown in Fig. 1. As shown in the Figure, metastable state X occurs when the input data of the flop changes right before the clock edge causing a setup time violation. Same will occur if the data is changed too early after the clock edge. In this case, metastability will occur because of the hold time violation. When the flop is in a metastable state, the output of the flop can be somewhere in between the logical '1' and '0'. This can cause a damage to the circuit to which it is connected. Not only that, but the unstable state can also propagate through the logic and result in functional issues [1].

The duration of the metastability is also unknown. It can stabilize in a short period of time which will lower the risk of any potential logical issue, but it can also take some significant time which will most likely lead to problems. The potential issues described above are the reasons why metastability should be avoided, otherwise the design cannot be stable. The highest risk of metastability is in between the clock domain crossing (CDC). To lower the risk, special CDC circuits are developed to mitigate the risk. One of such circuits is described in this paper.

Previous work. The novel synchronizer cell design and the timing diagram are presented in the paper [2]. The schematic design of the synchronization scheme is presented in Fig. 2.

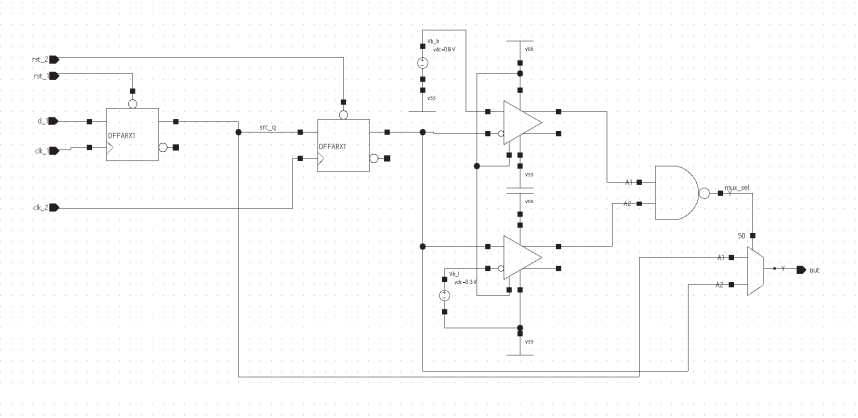

Fig. 2. The proposed sync cell scheme

This design allows to transfer control signals from asynchronous clock domains without losing additional 2…3 clock cycle delay compared with the traditional synchronization method. Also, for high-speed applications, where 3…4 synchronization stages are required, at least 30% area reduction is achieved.

The designed Verilog model. To create a pulse synchronizer for multi-bit data and stream data synchronizers based on a mixed-signal synchronizer cell, the

behavioral model's developed with Verilog hardware description language (HDL). This model has configurable parameters for setup hold time and output buffer delays. These parameters can be overridden on the instantiation of the cell and help to identify issues on early design stages. While the setup/hold violations are occurring, inside the model the X value is injected on the output of the meta D-flip-flop, which is done to simulate the metastability inside the synchronizer. Once timing violations have occurred on the meta D flip-flop and X value is injected, it forces the flop output to random value – logical '1' or '0'. The metastability duration is also parametrized [3]. Based on these numbers, the developed model is accurately simulating the design and providing realistic waveforms. There are strict timing requirements on the output delay of the synchronizer cell and meta flop D input delay propagation. As the analog comparator circuits detect the metastability, the multiplexer passes meta input D signal to the output, and if a corresponding delay is not inserted, the same metastability issue can occur on the flip-flop, in the destination domain driven by the synchronizer. In (1), the timing requirements are given:

$$\begin{cases} T_{DO} = T_{MMD}\ (T_{MMD} > T_{su} + T_h), \\ T_O = T_{su} + T_h\ (T_{MMD} \leq T_{su} + T_h). \end{cases} \quad (1)$$

In (1), T_{DO} stands for the delay from meta D input to sync cell output, T_{MMD} is the maximum possible metastability duration, T_O -the minimum output delay, T_{su} and T_h -the setup and hold time of the destination flop. These delays need to be handled in the design synthesis stage by inserting the corresponding buffers to meet the timing requirements. The corresponding design timing constraints should be applied on the design. The required delays are already inserted in the behavioral model, so simulations will show accurate results and the designer can validate its design even before doing synthesis and running gate level simulation.

In Fig. 3, simulation waves are presented. The first group contains the inputs of the sync cell: _s and _d correspond to the source and destination domain signals. From the Figure, it is seen that dff_s change causes meta flip-flop to get into metastable state, for which output of meta is marked as X. Then, due to the random value of the output, the meta flop is forced to 0, which means it is settled down after metastability. After mandatory delay which is calculated based on formula (1), sync_out signal is assigned to dff_s value. This delay is enough to have stable input on the dff_d and the corresponding value will be assigned on the next destination clock cycle. Here is the scenario when the changed value has passed to the output of the synchronizer without violating the setup/hold time on the sampling flop.

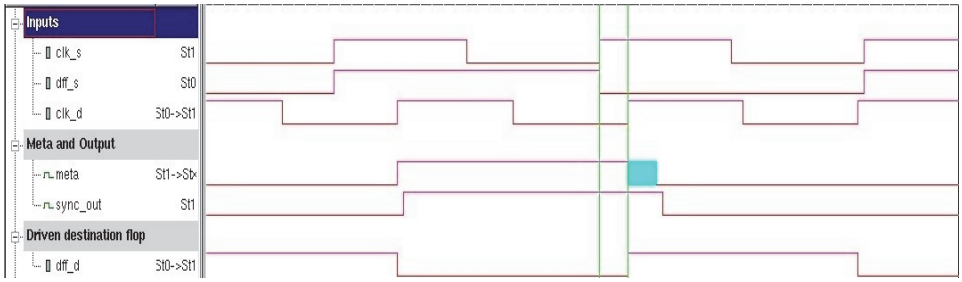

Fig. 3. The synchronizer cell model simulation waves 1

The other scenario is the one where the changed input value hasn't propagated directly to the output of the meta flip-flop. It is shown in Fig. 4. Once the meta flop has got into a metastable state, on the output, the mux picks the data coming from the source domain. This results in a small glitch. If in the scheme T_{DO} is increased, there is a possibility to filter that glitch, but even in this scenario, if delay calculated from (1) is kept during the design stage, this glitch will not be passed to the destination sampling flop, which will not cause any functional violation. If the source and destination frequencies are close, the output delay in case of 2 missamples can be maximum 2 clock cycles.

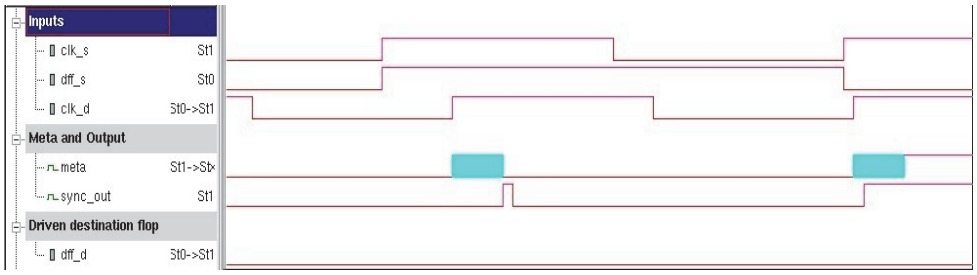

Fig. 4. The synchronizer cell model simulation waves 2

Comparison with conventional synchronizer. In Fig. 5, the waveform comparison of the novel sync cell and the conventional synchronizer is shown. For the conventional synchronization 2-stages are used and even in this case it is seen that 1 clock cycle improvement is achieved. If 3…4 stages are used, improvement in the face of more saved clock cycles will be achieved. This will bring to a performance improvement in complex multi-clock domain Integrated Circuits (ICs).

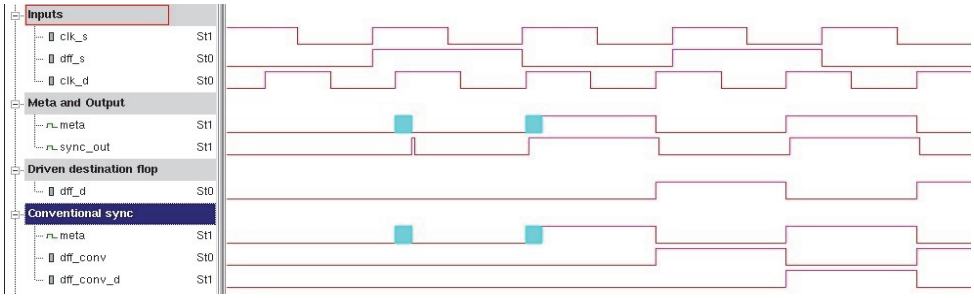

Fig. 5. Comparison with a conventional synchronizer

Pulse synchronizer design and comparison. Pulse synchronizer is designed based on a novel synchronization cell. The pulse synchronizer is used, when it is required to transfer pulse-type data/control signal from fast domain to slow domain [4]. The issue occurs when the slow destination domain is not able to capture the pulse because of the absence of the active clock edge during source pulse duration. Inside the pulse synchronizer, there is feedback driven from destination to the source domain [5]. Due to the low latency of the novel sync cell, the modified pulse synchronizer asserts the pulse in the destination domain at least 1 clock cycle earlier compared with the standard pulse synchronizer. In Fig. 6, the simulation results for both, standard and modified pulse synchronizer, is presented.

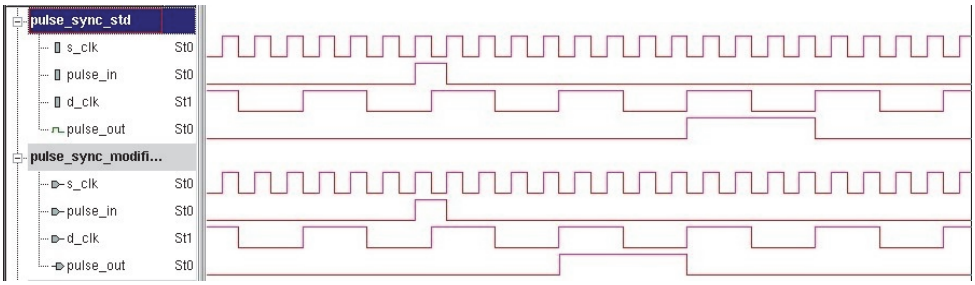

Fig. 6. Comparison of a standard pulse synchronizer

Future work. The complex multi-bit data synchronizer with different approaches will be presented based on the novel sync cell. It is expected to get more performance improvement for the implementation of 2-clock FIFO. The main idea will be removing gray encoding logic and use binary pointers. With this, area reduction will also be achieved.

Conclusion. The behavioral Verilog model for previously presented sync cell and pulse synchronizer cell is designed and presented. The design handles the major CDC issues and filters the metastability. The use of the synchronizer cell improves the synchronization latency by at least 1 clock cycle compared with 2-stage

conventional synchronizer, but it consumes 20% more area. In high frequency applications, where 3 and more synchronization stages are used, the latency is improved by more than 2 clock cycles, and at least 30% area reduction is achieved. The power consumption is expected to increase due to the mixed-signal design. The comparison will be presented in future works in scope of SoC.

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National Polytechnic University of Armenia. The material is received on 08.12.2021.

Տ.Կ. ԿԱՊԼԱՆՅԱՆ

ՆՈՐ ԻՄՊՈՒԼՍԱՅԻՆ ՀԱՄԱԺԱՄԱՆԱԿԱՑՈՒՑԻՉԻ ՆԱԽԱԳԾՈՒՄԸ ԱՌԱՋԱՐԿՎԱԾ ՀԱՄԱԺԱՄԱՆԿԵՑՄԱՆ ԲՋՋԻ ՄՈԴԵԼՈՎ

Ներկայացված են մեր նախորդ աշխատանքում առաջարկված նոր համաժամանակեցման բջջի վարքագծային մոդելի և իմպուլսային համաժամանակեցման սխեմայի նախագծերը։ Վարքագծային մոդելը նախագծված է Verilog ՍՆԼ-ով։ Իմպուլսային համաժամանակեցման սխեման նախագծված է վերը նշված վարքագծային մոդելի հիման վրա և ստուգված է “X”-ներմուծման մեթոդով նմանակման ժամանակ, ինչը հնարավորություն է տալիս հայտնաբերել սխալները նախագծման նախնական փուլերում։ Նախագծված համաժամանակեցման սխեմաների կիրառումը նպաստում է մակերեսի և համաժամանակեցման համար անհրաժեշտ տակտային ազդանշանների հապաղման նվազեցմանը, ինչը լավացնում է ընդհանուր համակարգերի արագագործությունը, որտեղ դրանք կիրառվում են։

Առանցքային բառեր. տակտային ազդանշանների կղզյակների հատում (ՏԱԿՀ), համաժամանակացուցիչ, մետակայունություն։

Т.К. КАПЛАНЯН

РАЗРАБОТКА НОВОГО ИМПУЛЬСНОГО СИНХРОНАЙЗЕРА НА ОСНОВЕ МОДЕЛИ ПРЕДЛОЖЕННОГО СИНХРОНИЗИРУЮЩЕГО ЭЛЕМЕНТА

Представлена модель предложенной ранее новой схемы синхронизации, а также синхронизатора импульсов. Поведенческая модель разработана с помощью ЯОА Verilog. Разработан импульсный синхронайзер на основе созданной модели, который верифицирован с X-инжекцией во время моделирования для выявления дефектов на ранних стадиях разработки. Использование разработанных синхронайзеров уменьшает использованную площадь и число тактовых задержек, требуемых для синхронизации, что приводит к улучшению производительности всей системы, в которой они используются.

Ключевые слова: пересечение тактовых доменов (ПТД), синхронайзер, метастабильность.