ISSN 0002-306X. Proc. of the RA NAS and NPUA Ser. of tech. sc. 2021. V. LXXIV, N4

UDC 621.3.049.77 **MICROELECTRONICS**

DOI 10.53297/0002306X-2021.v74.4-457

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DEVELOPING A NEW SENSE AMPLIFIER BY APPLYING THE METHOD OF THE DISSIPATION POWER REDUCTION FOR SRAM

A voltage latch sense amplifier by applying the power consumption reduction method is introduced. The presented sense amplifier is compared with the classical voltage latch-type sense amplifier and an amplifier with a leakage control (LECTOR) technique is applied. The designs are carried out by 14 *nm* FinFET technology. The results of simulations show that in the case of the proposed design, the power dissipation and propagation delay is improved. Simulation is performed for typical-typical (tt), slow-slow (ss), and fast-fast (ff), process voltage temperature (PVT) corners.

***Keywords*:** static random-access memory, sense amplifier, LECTOR, power reduction, FinFET.

Introduction. Nowadays, the variety of the battery-powered mounts has led to more demanding requirements for the design of low-power integrated circuits. Particularly, in the static random-access memories (SRAM), power consumption is one of the important parameters.

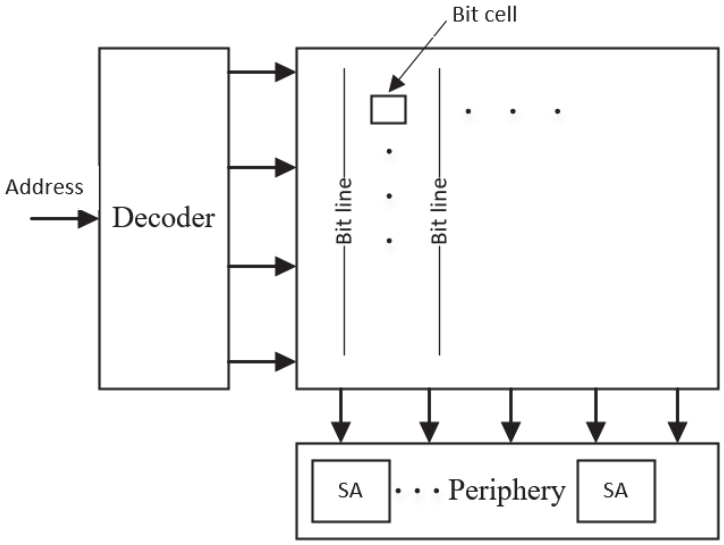

Fig. 1. A high level SRAM block diagram

This idea has been researched for the SRAM sense amplifier. Fig. 1 introduces the high-level block diagram of SRAM. It shows that the SRAM periphery consists of a row of sense amplifiers, which are connected to bit lines. While the word line and bit line are selected, the corresponding sense amplifiers perform the reading operation from the selected bit cell. In that period of time, other sense amplifiers are in non-working mode and consume static power.

A method of static power consumption reduction in the sense amplifier is introduced. The delay and dynamic power consumption of the proposed sense amplifier has been analyzed. A comparison with other leakage reduction methods, is presented.

A typical sense amplifier. The role of sense amplifier (SA) in SRAM is to detect the slight voltage difference across the bit lines and amplify it. As a typical SA, a voltage latch sense amplifier (VLSA) is picked. It is shown in Fig. 2 [1].

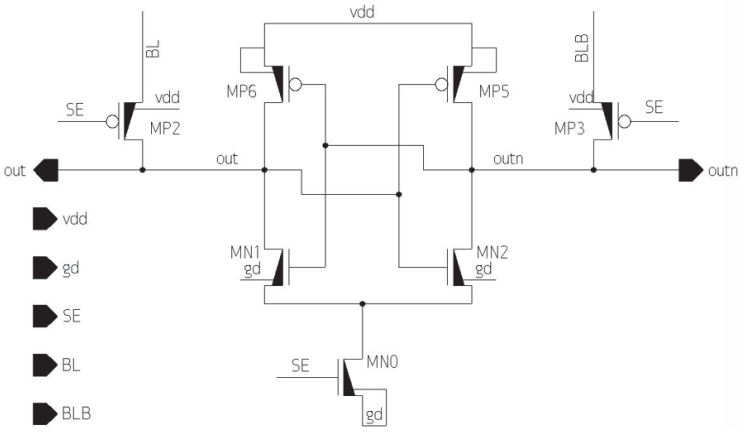

Fig. 2. A typical VLSA scheme

If EN equals logical 1, the amplifier is enabled. While voltage difference appears between BL and BLB, VLSA will amplify that difference to full-swing signal at the output. When EN = 0 amplifier is in the sleep mode, due to the small channel length and the threshold voltage, current flows between the drain and the source in cross-coupled inverters. I_{sub} in Fig. 2 stands for the subthreshold leakage current [2].

Leakage power improvement approaches. Since VLSA forms CMOS cross-coupled inverters, two leakage power reduction techniques are discussed for inverters.

Leakage Control approach. This is one of the widely spread approaches for reduction of leakage current and is known as a leakage control transistor (LECTOR) technique [3]. In the sense amplifier presented in Fig. 3, the LECTOR method is applied.

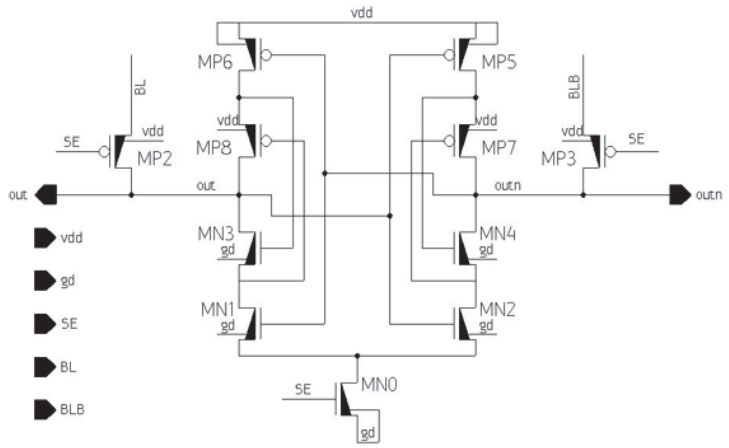

Fig. 3. An amplifier with a LECTOR-technique applied scheme

Here, MN3, MP8 and MN4, MP7 extra transistors are to restrict the flow of current when MP6, MN1 and MN2, MP5 are in the subthreshold region. The disadvantage of this technique is the additional delay introduced by the method [4].

The diode-connected approach. The CMOS inverter application by this method is presented in [5]. The approach is presented in Fig. 4. The idea of this method is to decrease the voltage between the source and the drain. As shown in Fig. 4-b, there are two additional transistors, diode-connected P2 and N2. The objective of transistor P2 is to provide a leakage current to N1. That causes a rise of the potential of the N1 source node, therefore the V_{DS} voltage of the N1 transistor will decrease, while the output node will have logical "1" [5].

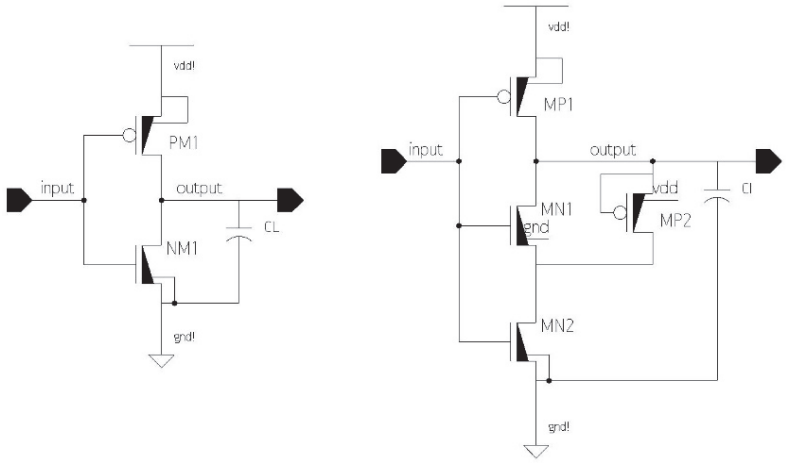

Fig. 4: a CMOS inverter, b – CMOS inverter with the diode-connected method

The new voltage latch sense amplifier is presented in the next section. VLSA is designed by the above described technique using the SAED 14 *nm* technology [6]. The power consumption and the delay are analyzed. The results are compared with those of the amplifier shown in Fig. 2 and Fig. 3.

The proposed sense amplifier. The proposed VLSA is shown in Fig. 5. Here, the extra transistors are MP7 and MP8. While the slight voltage difference appears between the nets BL, BLB, and SE is equal to logical "1", the amplifier can perform the reading operation. In this amplifier, in the cross-coupled inverters, there are no extra transistors, which can cause an incomplete output swing and a I_{sub} leakage current. The design and configuration of MP7, MP8 transistors are performed to make them work in a cut-off region. The leakage current that flows between extra transistors increases the V_{DS} voltage of MN3 and MN4, so the current, which flows between those transistors in the subthreshold region would increase, which could cause an increase in the value of the dissipated average power.

Since the designed circuit in Fig. 3 does not have a full swing, the output buffers of the sense amplifier need to solve that issue.

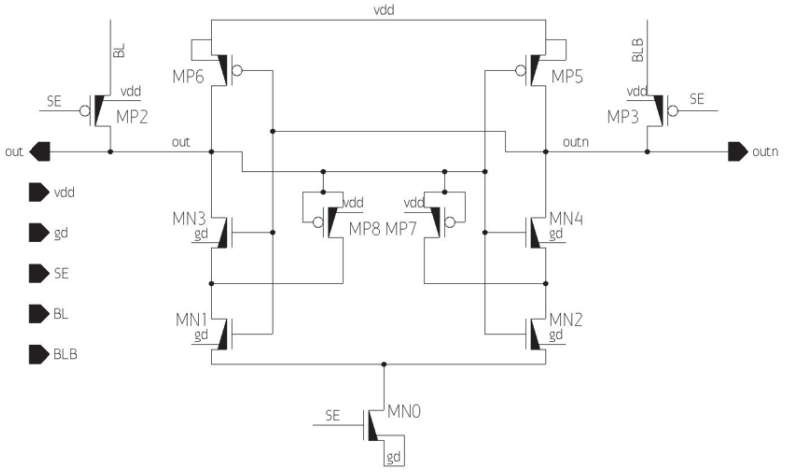

Fig. 5. The proposed latch sense amplifier

The design was performed by FinFET technology. In this process, the dependency between the increase in the number of fins and current is not linear. The reason of that leakage current is the quantum mechanical tunneling [7]. To minimize these effects instead of having two big multi-fin transistors (MN3 and NM4) four transistors with a lower fin count is used. It is shown in Fig. 5. The design was done with the Custom Compiler tool.

The total power consumption and the delay are analyzed. The results are compared with those of the amplifier shown in Fig. 3-b.

Simulations and results. The simulation results of the amplifier with LECTOR technique applied and the proposed amplifier are introduced in Fig. 6 and Fig. 7 respectively. Simulations are performed for tt, ss, ff processes voltage temperature (PVT) corners with a supply voltage of VDD = 0.75V ± 10%. The power consumption and propagation delay of typical, LECTOR-connected, and proposed sense amplifiers for tt corner, are introduced in Fig. 6 and Fig. 7.

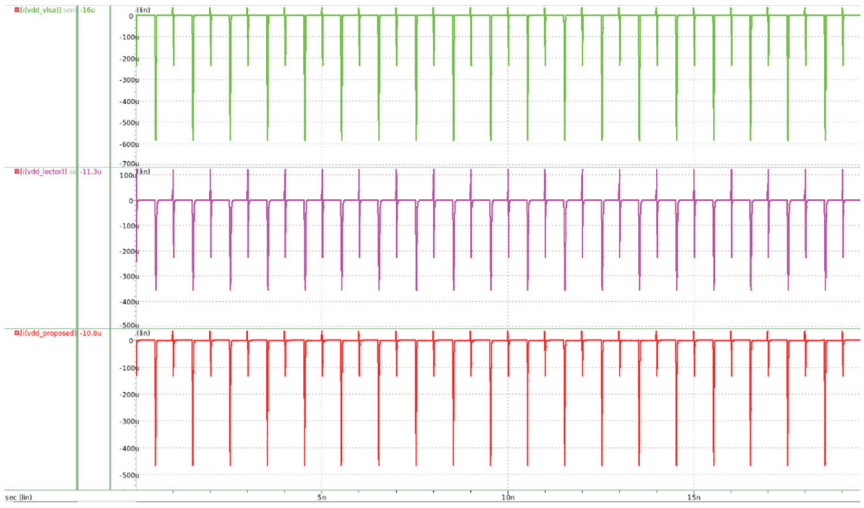

Fig. 6. Power consumption of sense amplifiers in the TT corner

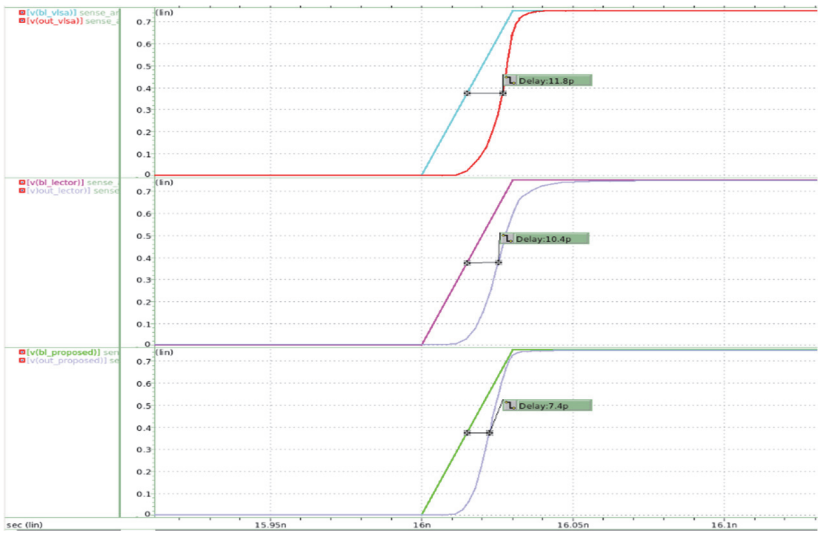

Fig. 7. Propagation delay of sense amplifiers in the TT corner

The table below presents the results of power consumption and propagation delay for the typical, LECTOR-connected and proposed SAs.

Table

Results of consumed power and propagation delay

Sense amplifiers	Power, *uW*			Propagation delay, *ps*		
	tt	ff	ss	tt	ff	ss
Typical SA	12	20.7	5.6	11.8	9.9	15.2
LECTOR SA	8.4	16	4.2	10.4	7.9	14.6
Proposed SA	8.1	14.6	4.1	7.4	5	12.2

Conclusion. The sense amplifier for SRAM is introduced by the method of power consumption reduction. As an object of comparison, a typical VLSA and a sense amplifier with a LECTOR technique is applied. The design is performed with the SAED 14*nm* FinFET technology. The simulations are carried out in tt, ss, ff technological processes. The results of simulations show that the average power consumption and propagation delay of the proposed amplifier is 32.5% and 37.3% less than typical VLSA in the TT corner. The results of the comparison show that the proposed SA has a 4% less consumed power than the LECTOR sense amplifier. Another important advantage of the proposed approach is the 28.9% less propagation delay than in case of the LECTOR sense amplifier due to the absence of two extra transistors in the current path, which causes instability within PVT variations.

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National Polytechnic University of Armenia. The material is received on 12.08.2021.

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ՍՏԱՏԻԿ ՕՊԵՐԱՏԻՎ ՀԻՇՈՂ ՍԱՐՔԻ ՀԱՄԱՐ ՆՈՐ ԸՆԹԵՐՑՈՂ ՈՒԺԵՂԱՐԱՐ՝ ՀԶՈՐՈՒԹՅԱՆ ՆՎԱԶԵՑՄԱՆ ՄԵԹՈԴԻ ԿԻՐԱՌՄԱՄԲ

Ներկայացված է նոր լաչ ընթերցող ուժեղարար՝ հզորության նվազեցման միջոցի կիրառմամբ: Զգայուն ուժեղարարը համեմատվել է դասական լարման լաչ և կորստի հոսանքի կառավարման (ԼԵԿՏՈՐ) մեթոդի կիրառմամբ ուժեղարարի հետ: Նախագծումը կատարվել է 14*նմ* FinFET տեխնոլոգիայով: Նմանակման արդյունքները ցույց են տալիս, որ առաջարկված նախագծի դեպքում ունենք բարելավված հզորության ցրում և հապաղում: Նմանակումները կատարվել են տիպային-տիպային (tt), դանդաղ-դանդաղ, արագ-արագ գործընթաց, լարում, ջերմաստիճան (ԳԼՋ) եզրային պարամետրերով:

Առանցքային բառեր. ստատիկ օպերատիվ հիշող սարք, ընթերցող ուժեղարար, ԼԵԿՏՈՐ, հզորության նվազեցում, FinFET:

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НОВЫЙ СЧИТЫВАЮЩИЙ УСИЛИТЕЛЬ С ПРИМЕНЕНИЕМ МЕТОДА УМЕНЬШЕНИЯ РАССЕИВАЕМОЙ МОЩНОСТИ ДЛЯ СТАТИЧЕСКИХ ОПЕРАТИВНЫХ ЗАПОМИНАЮЩИХ УСТРОЙСТВ

Представлена новая схема чувствительного усилителя типа латч с применением метода уменьшения энергопотребления. Проведено сравнение предложенного чувствительного усилителя с классическим усилителем типа латч и с усилителем, к которому применена техника контроля утечного тока (ЛЕКТОР). Схема разработана по технологии FinFET 14 *нм*. Результаты симуляции схемы показывают, что в случае предложенной схемы были улучшены рассеиваемая мощность и задержка распространения. Выполнено моделирование с применением следующих граничных значений по напряжению и температуре: типичное-типичное, медленное-медленное и быстрое-быстрое.

Ключевые слова: статическое оперативное запоминающее устройство, считывающий усилитель, ЛЕКТОР, понижение мощности, FinFET.