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H.T. KOSTANYAN

THE MINIMIZATION METHOD OF THE THERMAL DRIFT INFLUENCE ON ANALOG INTEGRATED CIRCUITS

The existing offset cancellation methods are based on digital-to-converters (DAC) and the calibration paths. During thermal drift the parameters of transistors in calibration path change, which increase the offset of the system. The proposed offset cancellation method includes current DAC which is directly connected to the output of the system. The absence of the calibration path makes the circuit more stable during temperature drifts without voltage-current-voltage conversion. The offset variation of the circuit during thermal drift is reduced 19 times (1.42 mV). The circuit occupies 43.2 % less area as in the current DAC, only transistors have been used instead of the resistor-transistor structure of voltage DAC. Power consumption increases 7 % as the branch of the current DAC is always on.

Keywords: analog, integrated circuits, offset, digital to analog converter.

Introduction. In modern integrated circuits (IC), operating frequencies have been raised to hundred Gbps, resulting signal degradation after the channel to a very high level of concern [1]. In modern high-speed serial-links, transmitter-channel-receiver structures are used to transfer the data. A channel is the line which connects the transmitter and the receiver. It acts like a low pass filter, which means that higher frequencies will be more affected in the input of the receiver [2]. To overcome the channel effect, a continuous time linear equalizer (CTLE), and a decision feedback equalizer (DFE) circuits are proposed [3]. DFE is a more complicated circuit which has nonlinear equalization and is used to cancel the inter symbol interference (ISI).

CTLE (Fig 1) is a differential-pair-based circuit which has a different behavior in low and high frequencies. It acts like common source amplifier in high frequencies and common source amplifier with source degeneration in low frequencies. It gives a chance to have a circuit with an inverse channel behavior and compensate high frqeuency rejection by the channel [4].

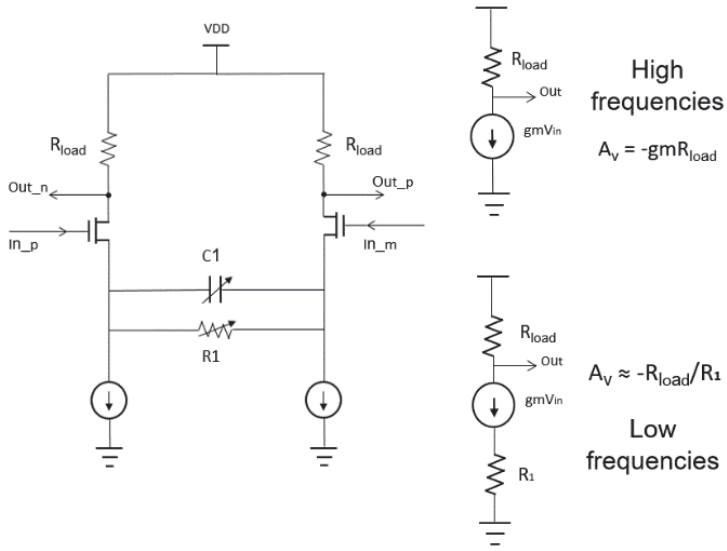

Fig. 1. CTLE circuit and gain values in low/high frequencies

To minimize the offset of such circuits, digitally assisted offset cancelation techniques are used [5-7]. The structure of such circuits is based on R-string digital- to-analog converters (DAC) connected with calibration path which minimize the offset by inserting additional current to the output of the system (Fig. 2). Such a method reduces the offset till millivolts, but considering the fact that modern circuits are operating in nonstandard environments where external conditions could be changed even after calibration, it has some disadvantages. During the temperature drift, the threshold of transistors in the calibration path changes. It can affect the transistors operation leading them to triode or cut off states.

The CTLE offset cancellation circuit has been designed by the SAED 14 *nm* FinFet technology (Fig. 2) [8], and HSpice simulations have been performed. The thermal drift effect has been checked for the CTLE circuit (-40^0C to 150^0C drift). The idea is that the circuit can startup in one temperature condition with defined codes during the calibration process and continue working in another conditions. In ICs bandgap reference is widely used, which provides temperature independent constant voltage [9], but in case of CMOS structured operational amplifiers and equalizers the temperature variation may affect the circuit functionality.

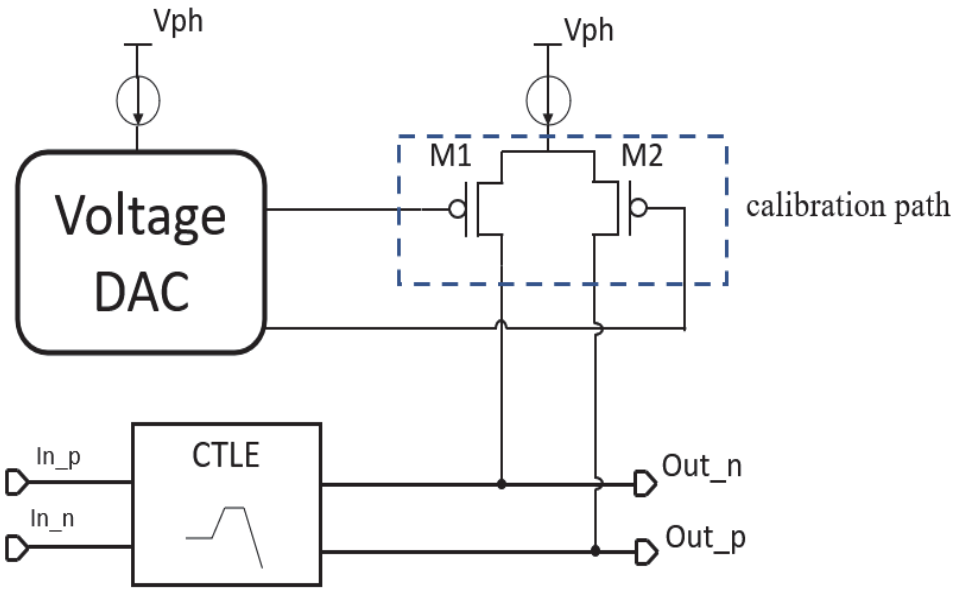

Fig. 2. CTLE circuit and gain values in low/high frequencies

The circuit has been verified with constant g_m circuit-biased current [10] and temperature independent bias current to understand the thermal drift effect for both cases.

In case of the current from the constant g_m circuit (Fig. 3 a) the thermal drift impact on the offset is small on low codes as the calibration path works as a differential amplifier (DA) and the constant g_m current compensates the gain variation depending on temperature. At high-code temperature impact on the offset is more visible because cancellation current flows through one branch, and the constant g_m current strongly depends on temperature.

In case of temperature-independent bias current (Fig. 3 b), for low code thermal drift impact on the offset is higher as the calibration path works as DA whose gain depends on temperature while bias current does not depend on temperature. At high code thermal drift impact on the offset is smaller as the cancelation current flow through one branch and bias current does not depend on temperature.

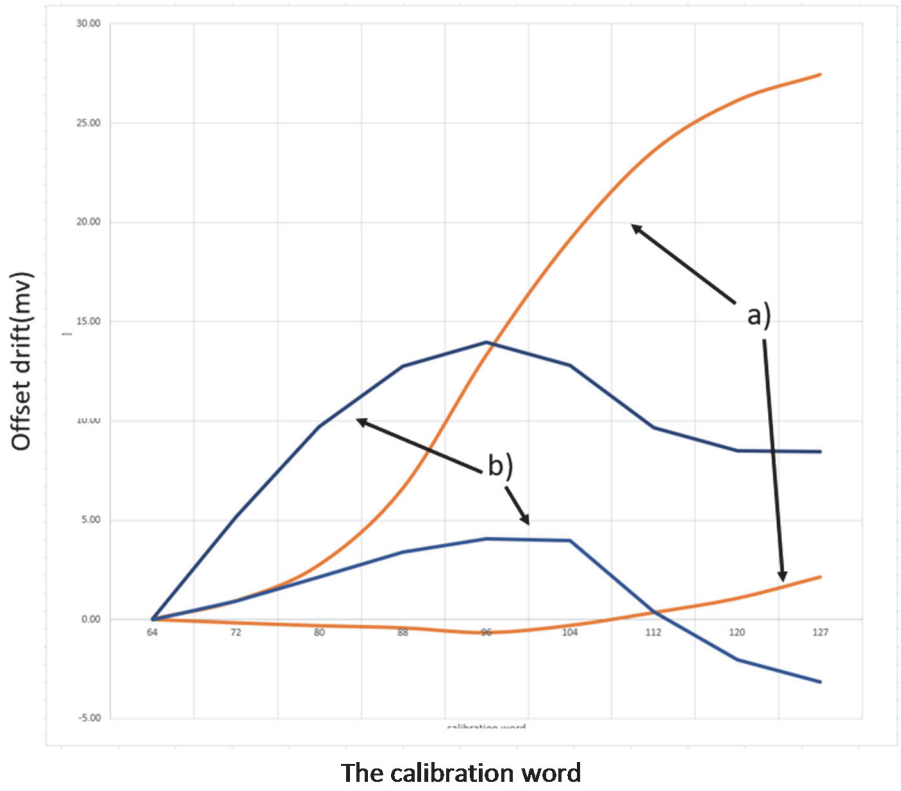

Fig. 3. The offset variation dependence on the calibration word during the thermal drift

The results in Table 1 show that even in case when the biasing current is a temperature-independent offset variation, ~10 *mV* exists. The issue comes from calibration branches (M1, M2 transistors), as the temperature effect on transistors (Vth change, Ids change) causing offset variation for a fixed code. Taking into account the problems described above new offset cancellation methods are needed to overcome the thermal drift effect.

Table 1

The worst-case PVT results with thermal drift implementation

The CTLE offset variation due to the thermal drift		
	Temperature independent current	constant g_m circuit current
Max offset	*10 mV*	*27 mV*

The proposed solution. Instead of the voltage DAC usage, during which operation voltage-current-voltage conversion exists, current DAC has been implemented. To keep the logic the same, an always-on current DAC has been added, for the case when both M1, M2 transistors have the same code and an equal current

from each branch. As it could bring additional offset because of parasitic resistances and capacitances of routing nets, always-off DAC has been added to keep the layout symmetry for both branches (Fig. 4).

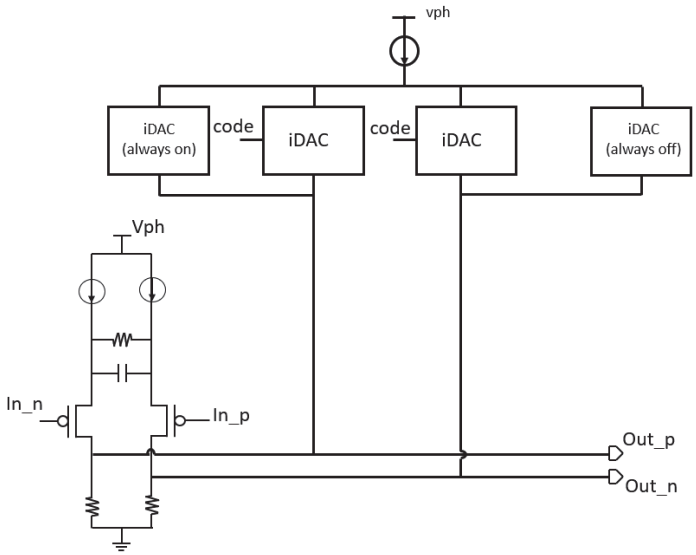

Fig.4. The proposed circuit

To test the proposed circuit a 50 *mV* offset has been added to one of the CTLE branches and the cancellation mechanism has been enabled, As shown in Fig. 5. Before calibration, the offset value is 50 *mV* and after calibration it is less than *1 mV*. Offset variation during the thermal drift from -40^{0}C to 150^{0}C is 1.42 *mV*.

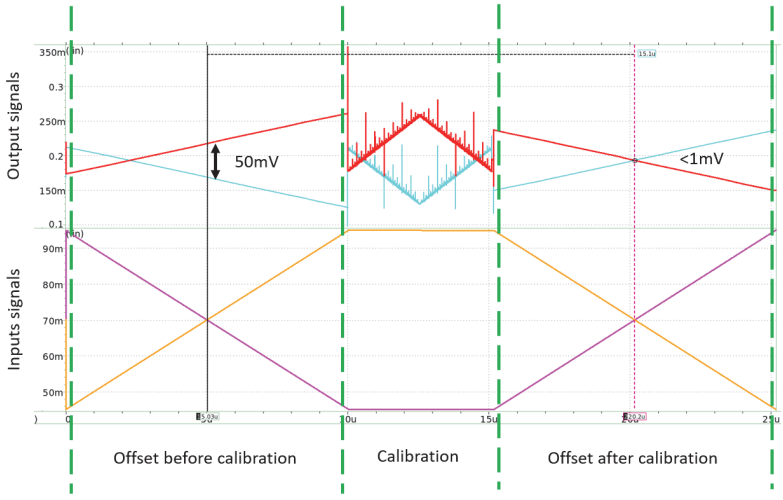

Fig.5. The simulation results with the proposed method

As the voltage obtained directly on resistors, the offset cancellation range is more linear (Fig. 6).

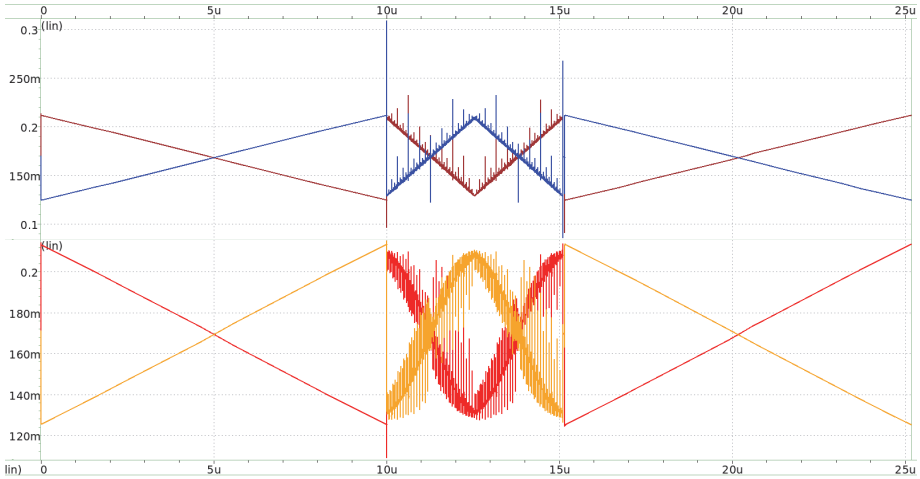

Fig.6. The simulation results for the proposed method before its implementation

Spice Monte Carlo (MC)[11] simulations have been performed for the proposed circuit to consider the deviations of the technological process. MC variation is more linear compared to voltage DAC case (Fig. 7,8).

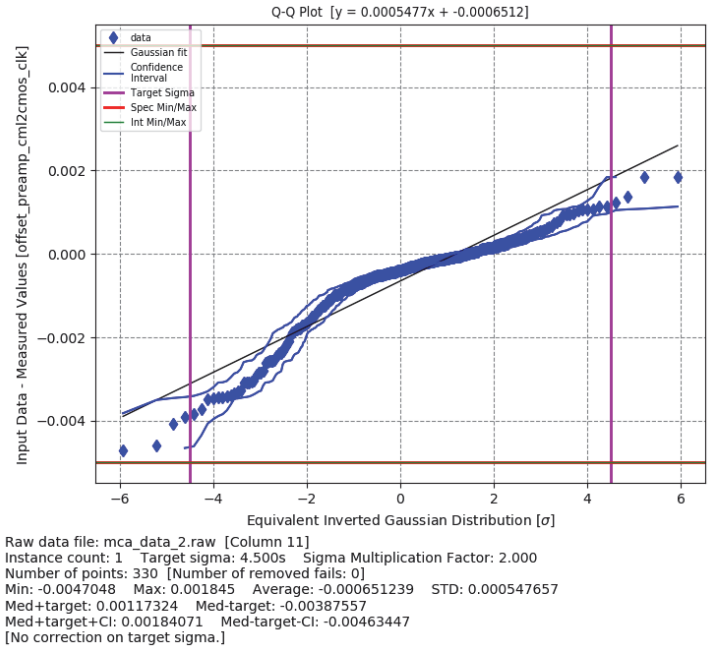

Fig.7. MC simulation results for the offset before the circuit modification (4.5 sigma)

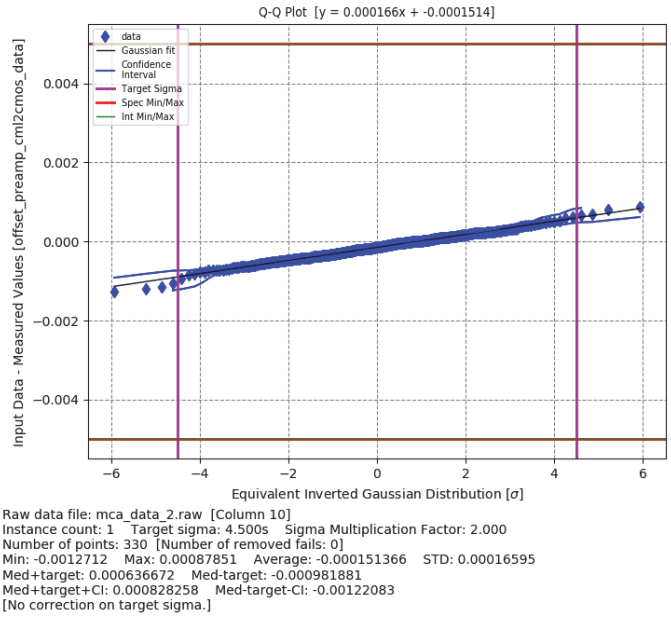

Fig.8. MC simulation results for the offset for the proposed method (4.5 sigma)

According to the Table 2, after the proposed changes, the total area of the circuit decreases about by about 43.2%, as the resistors in voltage DAC have been removed. The disadvantage of the proposed method is always on the current DAC branch which increases power consumption by 7%.

Table 2

Comparison with the existing methods

	[5]	[6]	The proposed method
Max offset variation due to thermal drift (mV)	26.98	15.12	1.42
Area (um^2)	2361.31	1631.529	1341.2
Power consumption (uW)	8341.25	8074.1	8924.87

Conclusion. The proposed offset minimization method includes current DAC which is directly connected to the output of the system. The absence of the calibration path makes the circuit more stable during temperature drifts without voltage-current-voltage conversion which was the main problem of the existing methods. The offset variation of the circuit during the thermal drift is reduced 19 times (1.42 mV). The circuit occupies 43.2% (1341.2 um^2) less area as in current DAC only transistors have been used instead of the resistor-transistor structure of voltage DAC. Power consumption increases by 7% (8924.87 uW) as current DAC is always on branch.

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Հ.Տ. ԿՈՍՏԱՆՅԱՆ

ԱՆԱԼՈԳԱՅԻՆ ԻՆՏԵԳՐԱԼ ՍԽԵՄԱՆԵՐԻ ՎՐԱ ՋԵՐՄԱՍՏԻՃԱՆԱՅԻՆ ՇԵՂՄԱՆ ԱԶԴԵՑՈՒԹՅԱՆ ՆՎԱԶԵՑՄԱՆ ՄԵԹՈԴ

Շեղման լարման նվազեցման գոյություն ունեցող մեթոդները հիմնված են թվաանալոգային ձևափոխիչների (ԹԱՁ) և կարգաբերման ուղու վրա: Ջերմային դրեյֆի ժամանակ կարգաբերման ուղու տրանզիստորների պարամետրերը փոխվում են, ինչը մեծացնում է համակարգի շեղման լարումը: Շեղման լարման նվազեցման առաջարկված մեթոդը ներառում է հոսանքի ԹԱՁ, որն ուղղակիորեն միացված է համակարգի ելքին: Կարգաբերման ուղու բացակայությունը շղթան ավելի կայուն է դարձնում ջերմաստիճանի շեղումների նկատմամբ՝ առանց լարում-հոսանք-լարում փոխակերպման: Ջերմային դրեյֆի ժամանակ շեղման լարման փոփոխությունը կրճատվել է 19 անգամ (1,42 *մՎ*): Սխեման զբաղեցնում է 43,2%-ով ավելի քիչ մակերես, քանի որ հոսանքի ԹԱՁ-ն օգտագործում է միայն տրանզիստորներ՝ լարման ԹԱՁ-ի ռեզիստոր-տրանզիստորային կառուցվածքի փոխարեն: Հզորության սպառումն ավելացել է 7%-ով՝ հոսանքի ԹԱՁ-ի միշտ միացված ճյուղի պատճառով:

Առանցքային բառեր. անալոգային, ինտեգրալ սխեմաներ, շեղման լարում, թվաանալոգային ձևափոխիչ:

А.Т. КОСТАНЯН

МЕТОД МИНИМИЗАЦИИ ВОЗДЕЙСТВИЯ ТЕПЛОВОГО ДРЕЙФА НА АНАЛОГОВЫЕ ИНТЕГРАЛЬНЫЕ СХЕМЫ

Существующие методы минимизации смещения напряжения основаны на цифроаналоговых преобразователях (ЦАП) и пути калибровки. При тепловом дрейфе параметры транзисторов на пути калибровки изменяются, что увеличивает смещение системы. Предлагаемый метод компенсации смещения включает ЦАП тока, который напрямую подключен к выходу системы. Отсутствие калибровочного тракта делает схему более устойчивой при температурных дрейфах без преобразования напряжение-ток-напряжение. Изменение смещения схемы при тепловом дрейфе уменьшено в 19 раз (1,42 *мВ*). Схема занимает на 43,2% меньше площади, так как в ЦАП тока использованы только транзисторы вместо резисторно-транзисторной структуры ЦАП напряжения. Энергопотребление увеличивается на 7% из-за всегда включенной ветки ЦАП тока.

Ключевые слова: аналоговый, интегральные схемы, смещение напряжения, цифроаналоговый преобразователь.