ISSN 0002-306X. Proc. of the RA NAS and NPUA Ser. of tech. sc. 2022. V. LXXV, N1

UDC 621.3.049.77 **MICROELECTRONICS**

DOI: 10.53297/0002306X-2022.v75.1-100

O.H. PETROSYAN, A.M. MOMJYAN, D.S. SHALJYAN, D.V MANUCHARYAN

A NOVEL METHOD OF POWER REDUCTION FOR A SRAM SENSE AMPLIFIER WITH A SELF-CALIBRATION MECHANISM

A latch sense amplifier with a biasing technique is designed and a new self-calibration unit (SCU) of power is presented for static random access memory (SRAM). Calibration of current which is the same as power consumption is calibrated for various frequencies is the range 0.5*Ghz* to 2.3*Ghz*. The advantage of such a sense amplifier is to control the current due to the bias-connected, saturated NMOS transistor. The simulation of the SCU scheme is applied in the presented sense amplifier. The results of simulation show that using the proposed SCU, the power consumption can reduce from 19% to 73% depending on frequency. The disadvantage of the proposed amplifier with a biasing technique increases the propagation delay from 8% to17% depending on frequency.

***Keywords*:** static random-access memory, FinFET, self-calibration, sense amplifier, power reduction, FSM.

Introduction. Shrinking of the device sizes and the increase in the performance requires the solution of a new problem: optimized power dissipation of the system. Nowadays, integrated circuits, including SRAMs can have several operation modes in terms of performance. Besides, due to technological processes and external influences, such as temperature, the operating frequency of the system may change. Therefore, it is necessary to optimize the power consumption of the system for different operation modes and different frequencies.

An important requirement of the SRAM design is the reduction of the power during the data reading process. For that purpose, reduction of power consumption of sense amplifier is required. One of the common types of the used sense amplifier is latch-sense amplifier due to its small area and performance [1]. In this work, as a reference amplifier, basic latch type sense amplifier is selected and a biasing technique to control the current flows during the read operation is applied to it.

A sense amplifier with a biasing technique. For the power consumption and noise resistance, a differential pair can be used as a sense amplifier, in which the current of the differential pairs is regulated by the saturated biased transistor [2]. However, due to the low gain, it is more effective to use latch-type sense amplifier. Obviously the reading frequency and the consumed power are directly

comparable [1,3]. The purpose of the proposed sense amplifier with a biasing technique (Fig. 1) is to calibrate the current for various frequencies.

The MN0 transistor is responsible for enabling the sense amplifier before reading the data from BL and BLB. While recharge is taking place in BL and BLB, EN is equal to logic 0. In this condition, the amplifier is in the operational state and can detect the minor voltage difference (ΔV) between the BL and BLB nodes.

The purpose of additional MN3 biasing transistor is to control the current flowing to the MP6-MN1 and MP5-MN2 branches. During the reading process the MN3 transistor is in the saturation region and it decides the amount of the current that flows.

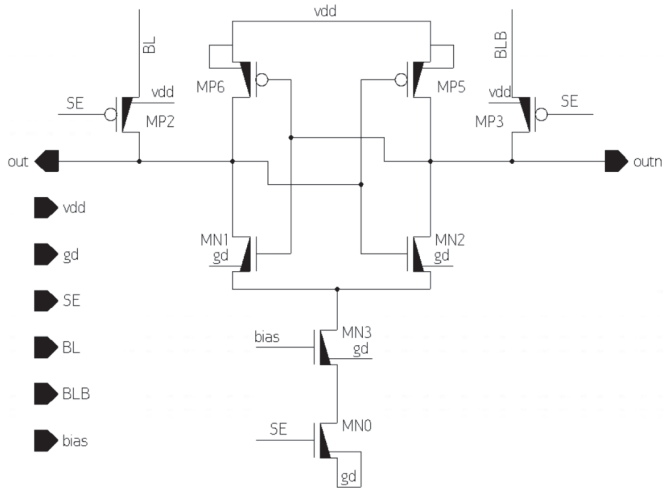

Fig. 1. A latch-type sense amplifier with a biasing technique

Depending on the reading frequency and the sensitivity threshold, $V_{gs} = V_b$ of MN3 could be different. For the certain f_{SE} frequency appropriate V_b voltage would be selected. The purpose of the latch - type sense amplifier with bising technique is to restrict or enlarge the current depending on the data reading frequency.

The main problem is that modern IC and SRAMs can operate with various frequencies and the goal is to calibrate the current during the reading process for SRAM sense amplifier [4]. The article proposes a mechanism for self-calibration of power of the sense amplifier in SRAM depending on the established reading frequency.

Architectural overview. The architecture of the SCU mechanism is proposed. The sense amplifier for applying this method is presented in Fig. 1. The main idea of the proposed SCU is to calibrate the V_b bias voltage of the MN3 transistor. The

high level block diagram of the proposed SCU is shown in Fig. 2. In SRAM, the reading block is an array of sensitive amplifiers. Those amplifiers must have the same sizes, the same operation voltages and the same topology, to avoid the timing issues during the reading process. For that reason, SCU is made as a replica of sense amplifiers, which is the same as in the SRAM sense amplifier array.

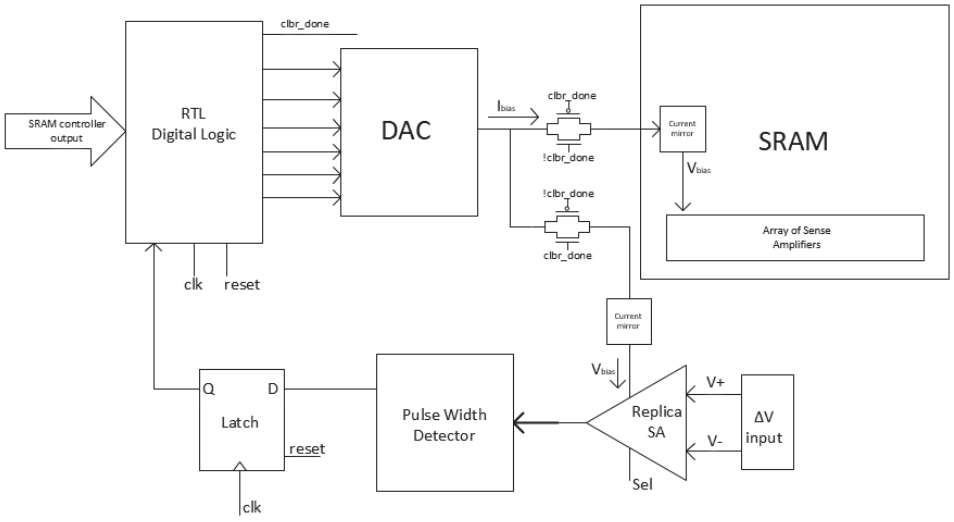

Fig. 2. The block diagram of SCU for SRAM

The SCU consists of five blocks, a digital calibration block, the current digital analog comparator (DAC), the voltage difference source (ΔV), the sense amplifier and pulse width detector. The proposed calibration is meant to be for post-production process. The principle of operation of the proposed SCU is as follows: first, we have defined the operating frequencies and the ΔV voltage sensitivity threshold. The digital calibration logic is a finite state machine (FSM) which generates a digital 8-bit signal as an input of current DAC. As an input of a replica sense amplifier, ΔV voltage is given. Depending on the output of digital logic, the output current of the DAC will increase until the output of replica SA will be a full swing signal (logical 1). Finally, the founded current will generate the V_b voltage through the current mirror. The digital code for every defined frequency will be saved.

FSM which describes the calibration logic of the proposed method is shown in Fig. 3. There are 5 states which are:

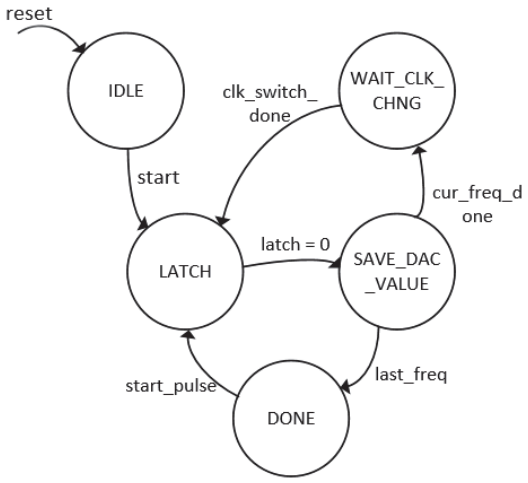

Fig. 3. FSM of the digital calibration logic

IDLE. FSM is waiting for START pulse to start operation.

LATCH. In this state bit lines of SRAM will be precharged. Depending on the previous state, the current 8-bit digital code is given to the DAC input. To clarify, if the previous state is *Idle*, the digital code will increase until the corresponding I_{b1} current is found. In case of the *LATCH* state, the code will be I_{b2} and so on. The input value from the latch is read if SA is able to read with that bias voltage (formed from I_{b1} current). In that case logical 0 will be at the output of the latch and FSM will move to the *SAVE_DAC_VALUE* state. In case of logical 1, the FSM will stay in the *LATCH* state.

SAVE_DAC_VALUE. In this state FSM saves the digital value corresponding to the calibrated I_b current. Those values are saved in the registers. If all frequencies are done, FSM moves to the *DONE* state, where it is asserting the "clbr_done" signal to indicate to the SRAM controller that calibration is completed, and bias current values are saved in the registers. In case the whole calibration is not completed, FSM moves its state to the *WAIT_CLK_CHNG*.

WAIT_CLK_CHNG. In this state, FSM waits for the SRAM controller to indicate that the clock switching is completed. Once received, it moves to the *LATCH* state.

DONE. In this state, DAC inputs are set based on frequency values provided by the SRAM controller.

In case of receiving the "start" pulse, FSM performs the calibration again.

Simulation results. Analog and digital parts are designed using the SAED 14 *nm* FinFET libraries [5]. The digital component of the calibration process is shown in Fig. 4.

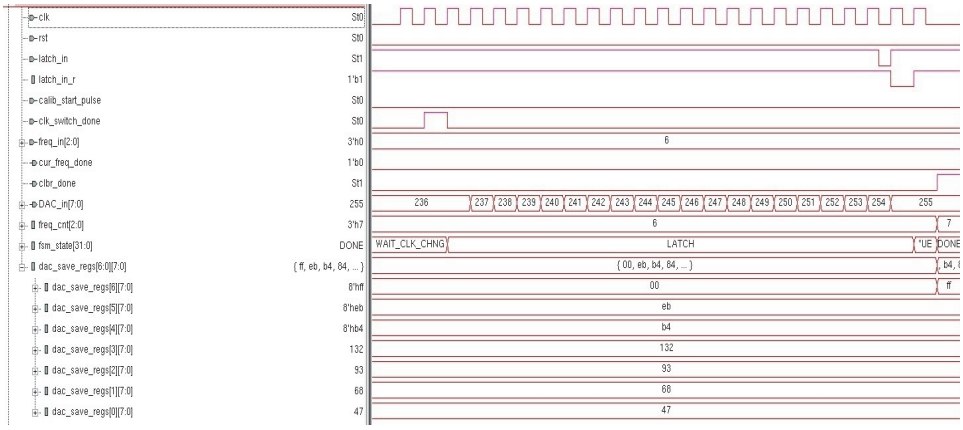

Fig. 4. The simulation results in the calibration process

For designing the proposed SCU, the HSPICE simulator is used. Fig. 5 shows the output current of the DAC. This scenario happens in the case when current I_b and then V_b is not enough for the driving SA in SRAM. Calibration is done for defined frequencies, which starts from 0.5 *GHz* to 2.3 *GHz* with the 0.3 *GHz* step. Fig. 5 presents only calibration of the current for the 2.3 *GHz* frequency. Until the marked red part is reached, the pulse with the detector will not be able to assert its output. That output reaches the digital logic through the latch. Digital logic will save the discovered current.

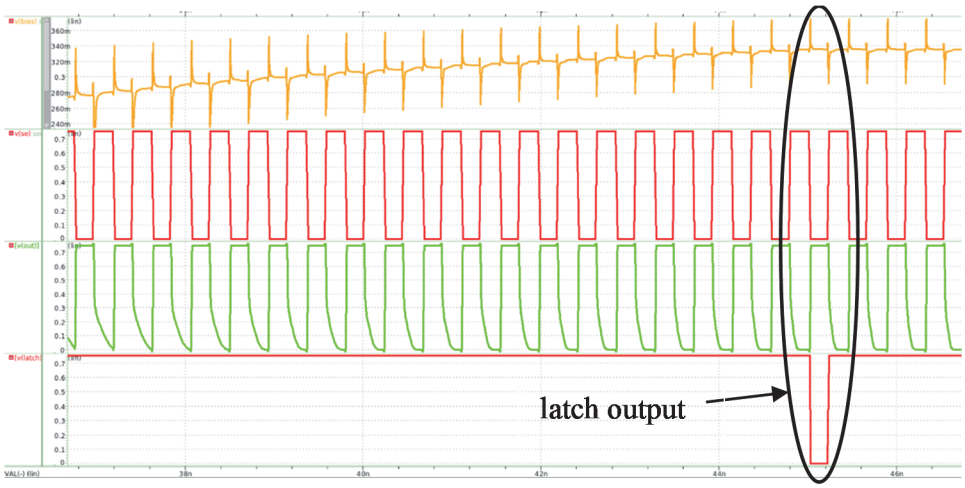

Fig.5. The calibration flow for detecting I_b for 2.3 GHz

Simulations were done for TT FF SS technological processes with $0.75V \pm 10\%$ power supply. For the above-mentioned frequencies, calibrated currents and bias voltages are shown in the Table below.

Table

Results of the calibrated power consumption and propagation delay for the defined frequencies

Frequency, GHz	Current, *uW*		
	tt	ff	ss
0.5	5.61	9.61	3.61
0.8	8.97	12.97	6.98
1.1	9.97	15.37	7.32
1.4	11.81	18.91	9.81
1.7	15.22	22.22	13.22
2	16.8	27.8	14.8
2.3	20.89	35.89	19.8

The dependency of frequency and power consumption, calibrated power consumption is shown in Fig. 6. The design is done for the maximum frequency of 2.3 *GHz*. The table above shows, that the proposed SCU allows to reduce the power consumption by minimum 19% for minimum frequency of 0.5 *GHz* and up to 73% for the 2.3 *GHz* frequency.

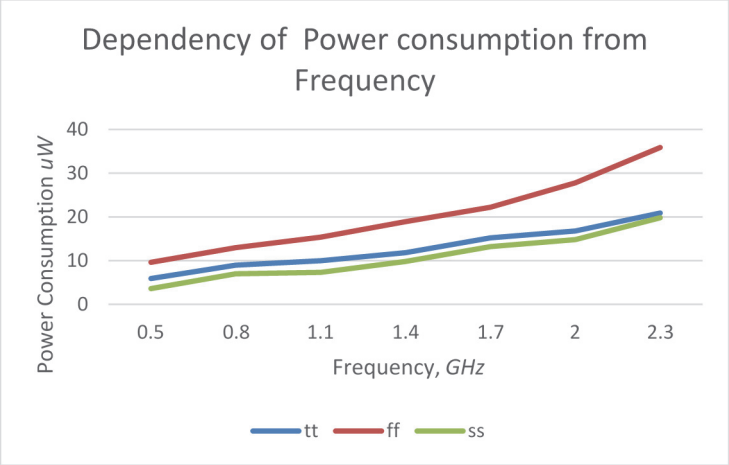

Fig.6. The dependency of calibrated power consumption on frequency

Since the calibration process results in a sense amplifier current change, it causes a delay in the reading process. The comparison of the propagation delay-frequency for biased SA and simple SA is shown in Fig. 7.

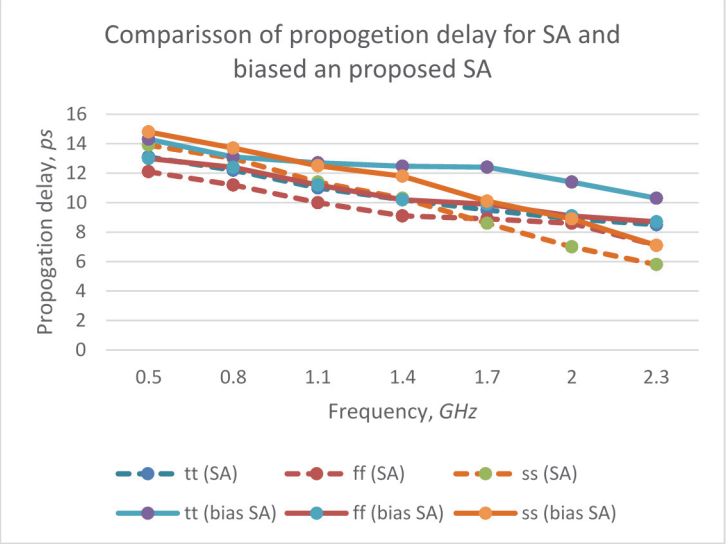

Fig.7. The comparison of the delay for the biased and proposed sense amplifier

Conclusion. The sense amplifier with a biasing technique is designed. The purpose of sense amplifier is to limit the current and hence power consumption for different frequencies. The SCU for the current is proposed. The SCU has analog and digital parts. The principal of its work is to find and save the digital value for every calibrated current for the defined frequency. The design has been done for slow, fast, and typical technological processes. The frequencies for calibration are picked starting from 0.5 *GHz* to 2.3 *GHz* with the 0.3 *GHz* step. From the simulation results, it can be seen that power consumption of sense amplifier during the reading process for different operating frequencies is reduced from 19% to 73%. The tradeoff here is the increased propagation delay. Again, for different frequencies, the propagation delay increased from 8% to 17% up to the frequency for the typical case.

REFERENCES

1. **Saini A., Gupta K. and Vivek K.** Analysis of Low SRAM Sense Amplifier // 2019 International Conference on Electrical, Electronics and Computer Engineering *(*UPCON*)*. – 2019. -P. 1-6.
2. **Elaakhdar M., Adly I. and Ragai H.** High Performance Time-Continuous Differential Sense Amplifier in Time Domain Sensing with 28 nm Technology for Automotive Applications // 2018 International Conference on Computing, Electronics & Communications Engineering (ICCECE). – 2018. -P. 256-265.
3. **Arora D., Gundu K. and Hashmi M.G.** A high speed low voltage latch type sense amplifier for non-volatile memory // 2016 20th International Symposium on VLSI Design and Test (VDAT). – 2016. -P. 1-5.

4. **Chotten P. and Richa A.J.** Performance Comparison of Body Biasing and Coupling Capacitor Sense Amplifier for SRAM // 2019 Devices for Integrated Circuit (DevIC). – 2019. -P. 75-78.
5. 14 *nm* Educational Design Kit: Capabilities, Deployment and Future / **V. Melikyan, M. Martirosyan, A. Melikyan, et al** // Proceedings of the 7th Small Systems Simulation Symposium, 12th-14th 2018.- Niš, Serbia, 2018.-P. 37-41.

National Polytechnic University of Armenia. The material is received on 09.02.2022.

Օ.Հ. ՊԵՏՐՈՍՅԱՆ, Ա.Մ. ՄՈՄՋՅԱՆ, Դ.Ս. ՇԱԼՋՅԱՆ, Դ.Վ. ՄԱՆՈՒՉԱՐՅԱՆ

ՍՕՀՍ-ՈՒՄ ԶԳԱՅՈՒՆ ՈՒԺԵՂԱՐԱՐԻ ՀԶՈՐՈՒԹՅԱՆ ՆՎԱԶԵՑՄԱՆ ՆՈՐ ՄԵԹՈԴ՝ ԻՆՔՆԱԿԱՐԳԱԲԵՐՄԱՆ ՄԵԽԱՆԻԶՄԻ ԿԻՐԱՌՄԱՄԲ

Նախագծվել է շեղման տեխնիկայով զգայուն ուժեղարար, և ներկայացվել է նոր հզորության ինքնակարգաբերման մեթոդ ստատիկ օպերատիվ հիշող սարքի համար: Հոսանքի կամ, որ նույնն է, սպառման հզորության կարգաբերումը կատարվել է տարբեր հաճախությունների դեպքում 0,5 *ԳՀց* -ից 2,3 *ԳՀց* միջակայքում: Այդպիսի զգայուն ուժեղարարի առավելությունը հոսանքի ղեկավարումն է՝ հենակային լարումով N տիպի մետաղ - օքսիդ - կիսահաղորդիչ տրանզիստորի միջոցով: Ինքնակարգաբերման սխեմայի նմանակումը կատարվել է ներկայացված զգայուն ուժեղարարի կիրառմամբ: Նմանակման արդյունքները ցույց են տալիս, որ կիրառելով առաջարկված ինքնակարգաբերման հանգույցը՝ սպառման հզորությունը կարող է նվազել 19%-ից 73%, կախված հաճախությունից: Առաջարկված շեղման տեխնիկայով ուժեղարարի թերությունը հապաղման աճն է 8%-ից 17%, կախված հաճախությունից:

Առանցքային բառեր. ստատիկ օպերատիվ հիշող սարք, FinFET, ինքնակարգաբերում, զգայուն ուժեղարար, հզորության ծախս, վերջավոր վիճակների ավտոմատ:

О.А. ПЕТРОСЯН, А.М. МОМДЖЯН, Д.С. ШАЛДЖЯН, Д.В. МАНУЧАРЯН

НОВЫЙ МЕТОД СНИЖЕНИЯ МОЩНОСТИ ЧУВСТВИТЕЛЬНОГО УСИЛИТЕЛЯ СТАТИЧЕСКОГО ОПЕРАТИВНОГО ЗАПОМИНАЮЩЕГО УСТРОЙСТВА С ПРИМЕНЕНИЕМ МЕХАНИЗМА САМОКАЛИБРОВКИ

Разработан чувствительный усилитель с техникой смещения и представлен новый метод самокалибровки мощности для статического оперативного запоминающего устройства. Калибровка тока, совпадающего с потребляемой мощностью, проведена для различных частот в диапазоне от 0,5 до 2,3 *ГГц*. Преимущество такого чувствительного усилителя состоит в том, что он позволяет управлять током благодаря подключенному со смещением насыщенному NMOS-транзистору. Моделирование схемы самокалибровки применено с представленным чувствительным усилителем. Результаты моделирования показывают, что при использовании предлагаемой схемы самокалибровки можно снизить энергопотребление от 19 до 73%, в зависимости от частоты. Недостатком предложенного усилителя со смещающим приемом является увеличение задержки распространения от 8 до 17%, в зависимости от частоты.

Ключевые слова: статическое оперативное запоминающее устройство (СОЗУ), FinFET, самокалибровка, чувствительный усилитель, рассеиваемая мощность, конечный автомат.