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SIMULATION METHODOLOGY BASED ON CONDITIONAL EXTRACTION AND SHORTEST PATH REPRESENTATION FOR ELECTROSTATIC DISCHARGE (ESD) ANALYSIS IN CMOS TECHNOLOGIES

Electrostatic discharge (ESD) is one of the reliability problems of today's IC. In addition, there is no such a tool, which will help to design ICs reliable against ESD. The problem is that ESD protection devices have always complex configuration, such as SCR ggMOS, etc., because of their working range, which is not well investigated and measured. Moreover, the other problem is the simulations complexity in the simulator machines from horse power point of view. The represented methodology allows designers to make their IC first spin reliable.

***Keywords**:* ESD, conditional extraction, shortest path, network flow.

1. Introduction. ESD protection devices are usually located inside the I/O circuit, which is connected to the pad and is the place, where external hazards are coming in, such as high currents caused by electrostatic discharges [1]. Moreover, during those events, the usual circuit representation given by the designer and/or commercial extractor tools is not enough. The limitation of commercial extractor tools is as follows:

- They perform device extraction based on Boolean operations of layout masks. The tools cannot extract parasitic devices such as field devices, SCRs or parasitic BJTs, which are often unintended side effect of the layout and not recognized by designers. However, they can play an important role during ESD stress events.
- They only extract circuit schematics under normal operating condition, i.e. when the chip is powered up. However, the circuit is not powered up during ESD events. An ESD event can generate stress current in excess of 1 A. The normal device models are not applicable, because devices are operating in high current regimes or biased differently from normal operating modes. Therefore, the schematic for circuit simulation must be determined according to the ESD conditions.

Therefore, an extraction tool, which would extract all parasitic devices aroused during ESD events that outlined in the first section of this paper, is necessary. However, extracting all those devices is not solving the whole problem. There is also a simulation part, which is also a challenge, since the simulation of the whole chip in device level (and this should be done, according to the ESD standard requirements) is something unreachable, so another approach is necessary to solve this problem too. The methodology for CMOS I/Os is proposed in Fig. 1. As depicted in the picture, the technological information (design rules, dielectric constants, diffusion thickness, etc), modeled ESD events and the layout in GDSII format are the inputs for further analyses.

In the conditional extraction part, the first is normal operating condition extraction process, by using a generic device extraction approach, and then in stress annotation part a specified ESD stress condition is given, the device bias conditions are identified

and the circuit schematic is extracted. The ESD stress condition is defined by specifying an I/O pad zapped positively or negatively with respect to another pad.

In BJT extraction part, parasitic BJTs are extracted and detected.

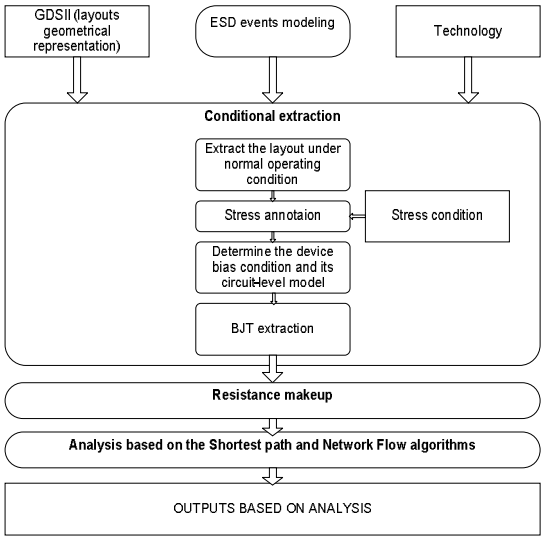

Fig.1. Simulation methodology's flow algorithm

Then comes the analysis based on the shortest paths and network flow algorithms.

2. Conditional Extraction. This part is intended for layout representation in the form, which is providing more process, happening during ESD events. During this event, chips usually are not powered up, the ESD zapping should be done for all possible pin combination of a chip for both positive and negative stresses, and the chip should pass 2 KV and more HBM-ESD level for all stresses. When the ESD zapping is performed between two pads, all other pads are kept floating.

Since the behavior of a device is bias-dependent, its circuit model should be determined according to its operating condition. The proposed static analysis technique, called *stress annotation,* determines each device's applicable circuit model.

In Figure 2 the depicted stress annotation is performed for the I/O circuit in a specified stress condition, i.e. positive stress on the pad with respect to Vss pad. First, the circuit schematic for the pad is extracted (Figure 1). Then stress annotation is conducted using the stressed current from stressed pad. The stressed current passes through forward biased p-n junctions and semiconductor resistors. The search is stopped when a reversed biased p-n junction is reached. Each interconnected net in the current path is annotated with stress strength. The relative voltage levels can be compared by checking their stress strength; also, these stress annotations help to make BJTs identifications. Starting with an initial value as 10 the stress strength will be reduced by one every time when the stress current passes through the resistor.

After the biased condition is determined from the stress annotation, each device's circuit model can be determined. When a device is under ESD current stress a high current model must be used, such as the NMOS model, which will cover the snapback regime range, and a resistor model, which can cover velocity saturation effect. When the p-n junction in a transistor is forward-biased under ESD stress it operates as a diode. When the junction formed between the drain diffusion of the driver PMOS transistor and the n-well is forward biased, the n-well is charged up and the high current is propagated to the Vdd power line via the well contact. For this case, we substitute the PMOS transistor with the serial combination of forward-biased diode and a well resistor. This is the applicable circuit model for the PMOS transistor under this specific bias condition.

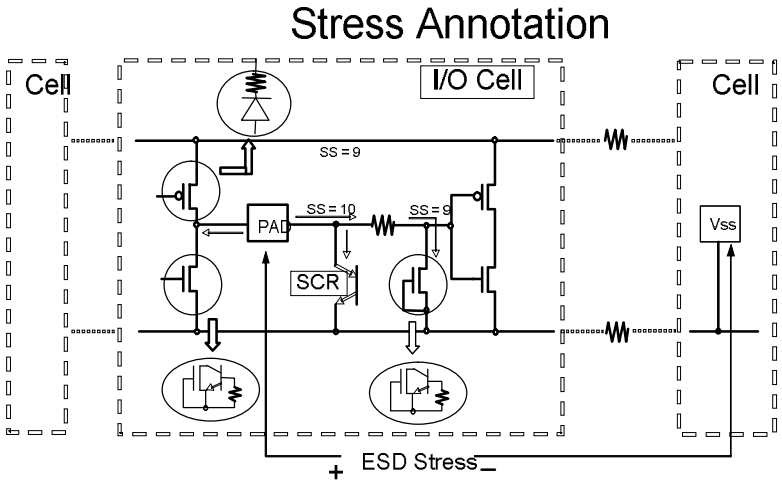

Fig.2. Stress annotation to identify devices bias condition and determiing its circuit model

The device graph is used for device extraction. Each device graph is used to describe one device [2].

The resistor makeup part is also a place where some investigation needs to be done, but this part will be skipped for further investigations.

3. Analysis based on the Shortest Path and network flow algorithms. After graphical representation of the electrical network, done especially for ESD events and abstracted using resistor's makeup system (Figure 3), the analysis on the network should give output results as an input for designers to make their discussions on how to change their design as to satisfy all reliability requirements. As a help for this item, the Network Flow algorithms called Convex Minimum Cost Maximum Flow is used.

Algorithm motivation. The basic theme of the ESD protection schemes is based on diverting huge amount of current from one bond pad to a bond pad with a connection to ground without passing through the core of the chip. The voltage drop between zapped and grounded bond pads can measure the success of the protection circuit. The voltage drop for each bond pad pair is commonly referred to as the ESD

budget for that pair. If the voltage drops are too high, then dangerous amount of current will trigger the gate oxide and possibly damage the circuit. By using graphical representation of the electrical network and the magnitude of the ESD current incident on the device, Network Flow algorithms enable to know maximum possible current flow rate, which will give also a good understanding on where to widen the current flow channels.

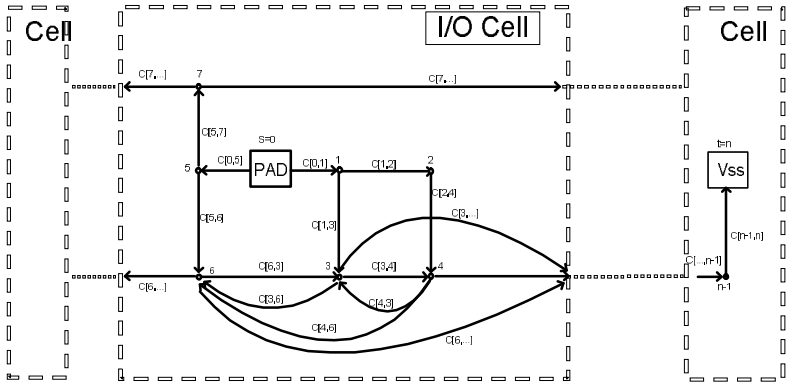

Fig.3. The graphical representation of electrical network based on ESD conditions. C is the weight vector, i.e. resistors in the electrical network

The representation of Convex Minimum Cost Maximum Flow (CMCMF) optimization problem from the ESD event point of view. Usually the CMCMF optimization problem is as follows:

$$\sum_{j=1}^{n} c_{ij} x_{ij} \to \min,$$

$$\begin{cases} \sum_{j:(i,j)\in A}^{n} x_{ij} - \sum_{j:(i,j)\in A}^{n} x_{ji} = b(i), \forall i \in N, \\ 0 \le x_{ij} \le u_{ij}, \forall (i,j) \in A, \end{cases}$$

where $c(i,j)$ is the cost of transportation and the $x(i,j)$ is the flow, $b: N \to R$ is the supply/demand vector and in an instance of CMCMF each $i \in V$ is either a supply node, corresponding to $b(i)$ > 0, or a demand node when $b(i)$ < 0 is an intermediate node if $b(i)$ = 0. The vector b is referred to as the *mass balance constraint* for the CMCMF problem. In addition, it should be noticed that in order for the problem to make sense we must have:

$$\sum_{\forall i \in N} b(i) = 0 .$$

The notations N (graphs vertex vectors) and A (adjacency graph) are representation of graph, as $G=(N,A)$ [3]. By approximating these assumptions for our electrical network, it should be accounted that the arcs in our network represent resistors, diodes, etc., which carry the current. Moreover, what should be found is: How much current is flowing on each resistor (arc) in the network? Once the amount of current, flowing on each component of the electrical network, is found, it is a simple matter to apply Ohm's law to each component along any single path, and to sum voltage drop contributions. So, according to Ohm's law the representation of CMCMF from ESD point of view shows that a resistor with resistance r dissipates rI^2 watts of power, where I is the amount of current flowing along the resistor. Therefore, the equilibrium current will be found on each arc in our network under this cost model. That is for each arc $(i,j)\in A(G)$, which collectively depicts our network graphically, the equilibrium current $x(i,j)$ will be found, where the cost of augmenting current along the arc (i,j) varies (convexly) as the square of the amount of flow along that arc, multiplies its resistive component c_{ij}. Keeping this in mind, we rewrite the CMCMF as

$$\sum_{j=1}^{n} C\ (x_{ij}) \rightarrow \min,$$

$$\begin{cases} \sum\limits_{j:(i,j)\in A}^{n} x_{ij} - \sum\limits_{j:(i,j)\in A}^{n} x_{ji} = b(i) \forall i \in N, \\ 0 \le x_{ij} \le u_{ij} \forall (i,j) \in A, \end{cases}$$

and our convex cost C will be $C(x_{ij}) = c_{ij} * x_{ij}^2$.

With these assumptions it is possible to compute the optimal (equilibrium) current on each arc, after which it is possible to compute the voltage drop on the shortest path (minimal resistance path) between the source and sink, by using Dijkstra's *Single Source Shortest Path (SSSP)* algorithm. The basic idea of SSSP is that a path $P=\langle s=a_1 \ldots a_k=t\rangle$ between *s* and *t* is the *shortest path*, only if for any other path $P'=\langle s=a_1' \ldots a_j'=t\rangle$, thus:

$$\sum_{i=1}^{k-1} c(a_i, a_{i+1}) \le \sum_{i=1}^{j-1} c(a_i', a_{i+1}').$$

According to the electrical analysis, we can say that this algorithm allows to find the path with the possible minimum resistance between source and sink. And if the shortest path $P=\langle s=v_1, v_2, \ldots, v_k=t\rangle$, the voltage drop will be:

$V = \sum_{i=2}^{n} c(v_{i-1}, v_i) \cdot x^*(v_{i-1}, v_i)$, where x^* is the equilibrium current.

This result is the main desired result which means there must be further analysis.

4. Conclusion. Thus, by having the amount of current flown through each arc, which is possible to get by using the CMCMF algorithm, and the path with minimal resistance, found by Dijkstra's SSSP algorithm, it is a simple matter to compute the excitation level between two pad pairs, and the needed information for designers' further analysis.

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Վ.Շ. ՄԵԼԻՔՅԱՆ, Դ.Ֆ. ԴԱՎԹՅԱՆ, Կ.Ա. ՖԱՆՅԱՆ

ՎԻՃԱԿԱՅԻՆ ՔԱՂՎԱԾՔԻ ԵՎ ԿԱՐՃԱԳՈՒՅՆ ՃԱՆԱՊԱՐՀԻ ՆԵՐԿԱՅԱՑՄԱՆ ՎՐԱ ՀԻՄՆՎԱԾ ՄՈԴԵԼԱՎՈՐՄԱՆ ՄԵԹՈԴԱԲԱՆՈՒԹՅՈՒՆ ԿՄՕԿ ՏԵԽՆՈԼՈԳԻԱՆԵՐՈՒՄ ԷԼԵԿՏՐԱՍՏԱՏԻԿ ԼԻՑՔԱԹԱՓՄԱՆ (ԷՍԼ) ՀԵՏԱԶՈՏՈՒԹՅՈՒՆՆԵՐԻ ՀԱՄԱՐ

Էլեկտրաստատիկ լիցքաթափումը (ԷՍԼ) այսօրվա ինտեգրալ սխեմաների (ԻՍ) ապահովության հիմնահարցերից է: Չնայած այդ փաստին՝ չկա այնպիսի ավտոմատացված գործիք, որը կօգներ նախագծել ԷՍԼ-ից պաշտպանված ԻՍ-եր: Խնդիրն այն է, որ ԷՍԼ պաշտպանական սարքերն (հարթակը ղեկավարող ուղղիչները, փականով հողանցված ՄՕԿ-երը) ունեն բարդ կառուցվածք՝ աշխատանքային միջակայքերի պատճառով: Բացի դրանից, գոյություն ունի նաև մոդելավորման բարդություն՝ մոդելավորման ընթացքում օգտագործվող մեքենաների մեքենայական ժամանակի և հզորության օգտագործման տեսակետից: Ներկայացված մեթոդաբանությունը թույլ է տալիս նախագծել ԷՍԼ-ից պաշտպանված ԻՍ:

Առանցքային բառեր. ԷՍԼ, վիճակային քաղվածք, կարճագույն ճանապարհ, ցանցի հոսք:

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МЕТОДОЛОГИЯ МОДЕЛИРОВАНИЯ ДЛЯ ИЗУЧЕНИЯ ЭЛЕКТРОСТАТИЧЕСКОЙ РАЗГРУЗКИ В КМОП ПРИ ИСПОЛЬЗОВАНИИ ОБУСЛОВЛЕННОГО ИЗВЛЕЧЕНИЯ И ПРЕДСТАВЛЕНИИ ЭСР КРАТЧАЙШИМ ПУТЕМ

Электростатическая разгрузка (ЭСР) является одной из проблем надежности сегодняшних интегральных схем (ИС). Несмотря на это, до сих пор не было создано ни одного инструмента, который помог бы проектировать ИС надежными в отношении ЭСР. Проблема состоит в том, что устройства, которые помогают защищать ИС от ЭСР, такие как выпрямитель, управляемый подложкой, МОП с заземленным затвором, имеют сложную структуру. При этом существует сложность моделирования с точки зрения машинного времени и мощности. Представленная методология позволяет проектировать ИС, защищенные от ЭСР.

Ключевые слова: ЭСР, обусловленное извлечение, кратчайший путь, поток сети.