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A.V. BABAYAN, G.A. ABGARYAN

GENERIC BIST ARCHITECTURE FOR MEMORIES

A generic Built-In Self-Test (BIST) architecture which is suitable for different types of well-known memories is proposed. This architecture consists of different components which are responsible for BIST features as operation execution and algorithm storage with a defined format. The main components of the proposed architecture are described. This architecture reduces the average test time by 0.85…3.21% (depends on the memory size).

***Keywords*:** embedded memory BIST, memory fault, test algorithm, System-on-Chip.

Introduction. It is a well-known fact that most demanded and used intellectual properties (IP) in a System-on-Chip (SoC) are memories. But they are most defect sensitive components because they are fabricated with minimum feature widths. Nowadays, there are numerous of types of memories each of which has its own pros and cons and can be used in certain types of integrated circuits (IC). Therefore, their reliability is of great importance and the BIST is known to be one of the most efficient solutions for large systems, which mainly consist of memories. The implementation of such a BIST solution, requires understanding of some basic notions and commonly used approaches. Some of them are described below.

Fault Modeling. There are many different types of memories (e.g., SRAM, DRAM, CAM, etc.) and each of them may be prone to certain specific fault types. For example, there are additional match port and valid bits in CAMs except the control and data ports. Hence, there can be stuck faults as well as transition faults for those ports and bits (always (mis)match faults, stuck (in)valid bit, etc.).

On the other hand, there are faults, which are common for most of the memories. Having the classification of the main fault types, which are common across the different memory types (Table 1), will help to create the corresponding test sequences and test mechanisms for them.

Memory Access Mechanism. The easiest way to access the memories is the direct access mechanism. In that case processors, driving memory signals, are connected to the inputs directly. There are other approaches like connection with interface or physical layer (PHY) in case of external memories [1]. But, in general, it is very common now that there are pipes between the memory and the processor. This resolves the possible timing issues.

Test sequence. To detect certain types of faults, different test sequences (algorithms) should be applied [2]. For example, to detect stuck-at 0/1 fault, simple write and read are used with an alternating background:

$$\{W0, R0, W1, R1\}. \quad (1)$$

To detect the transition fault 0 to 1 and 1 to 0, transitions should be applied. The below sequence contains both transitions:

$$\{W0, R0, W1, R1, W0, R0\}. \quad (2)$$

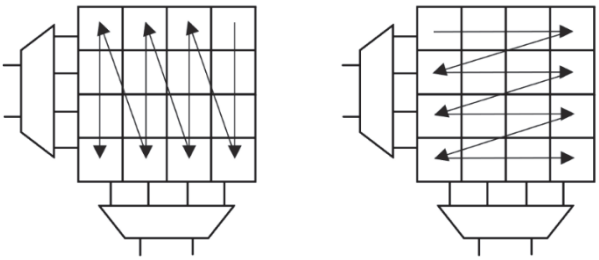

Fig 1. Addressing directions (fast column and fast row)

Table 1

Memory fault classification

Fault Type	**Fault Name**	**Fault Description**
Single-cell faults	Stuck-at 0/1	The logic value of a stuck-at (SA) cell or line is always 0 or 1. It is always in state 0 or in state 1 and cannot be changed to the opposite state.
	Transition 0/1	A cell that fails to undergo a 0 to 1 transition when it is written is said to contain an up-transition fault, and a down transition fault indicates that a cell fails to undergo a 1 to 0 transition.
	Write destructive faults	A non-transition write operation in a memory cell causes the cell to flip.
	Read destructive faults	A read operation is performed to the cell causes inversion of the value in the cell and returns the incorrect value.
	Stuck-open faults	The memory word cannot be accessed. When the sense amplifier contains a latch, during a read operation, the previously read value may be produced.
Two-cell faults	Static coupling faults	A given value 0 or 1 of the cell in the aggressor word forces a certain value 0 or 1 in a cell of the victim word.
	Transition coupling faults	A write transition operation applied to a cell of the victim word does not cause a transition if the aggressor word is in each state.

In general, memories have a word-oriented structure and non-bit-oriented, so certain background patterns (BP) can be applied to memory words that can help to detect two cell-related faults such as coupling faults. To detect all the combinations of two coupled bit-cells, (1) sequence can be used with two varying background patterns:

BP 1: Solid pattern (all 0/1) {W1, R1, W0, R0}
BP 2: Checkerboard pattern (all 01/10) {W(D), R(D), W(~D), R(~D)}

The Processor Components: Below are described the primary component blocks which are necessary to have complete memory BIST. A certain block can be different for certain type of memory, but the fundamental approaches are identical [3].

Table 2

March test operations

Operation name	Description
W	Applies simple write operation on the memory.
R	Applies simple read operation on the memory. Compares actual data with expected one (expected data is held until comparison).
RW	If memory has at least two control (read or write) ports than all these ports will be accessed simultaneously. Makes stress condition for the memory.
WW (Content Addressable Memory-CAM specific**)**	Applies write operation with logic patterns on both arrays of CAMs.
Compare (CAM specific)	Applies search operation in the whole memory during one cycle.
Hit (CAM specific)	Expects a single hit (match) on the current address.
Activate, Activate_2 (External Memory specific)	Applies a page activation.

Address Decoder. There are a few addressing types for a memory, each of which is used in different march algorithms [4]. There are fast row, fast column (Fig. 1), walking and galloping addressing modes which can be used with different data background patterns (solid, checkerboard).

Opcode Decoder. Once we have the described the memory pinout and the access mechanism for that, corresponding operations can be applied through the operation decoder. Table 2 describes the test operations used for different memories.

Data Comparator. This compares actual and expected data values and generates one-bit signal as a result. There is a possibility to have failing I/O bits via provided register.

March Element Format. March element consists of two parts. The first one is the configuration of the current operation set. The configuration which is a register with size of 10…20 *bits*. The size is defined based on memory type and algorithms, which should be used. The addressing direction and data patterns are described in this configuration. The second part contains the operations' sequence. The size of this part is fixed by the maximum number of operations, which is configurable. The rest of this part which is not used for operations are skipped during the march element execution. The possibility of algorithm programming allows to have own test sequences. Using the parallel loading mechanism for configuration register, the test time is improved for different sized memories compared with the results presented in [5].

March Element State Machine. To execute certain operations in a defined sequence, the algorithm format is defined. There can be different containers for march elements with specified format. In this solution, there are two ways to have an algorithm in a processor: hardwired, which means having the specified algorithm fixed in the processor, and programmable, which allows to load the algorithm through certain inputs of the processor. After selecting an algorithm, the internal logic parses it and executes the test operations using the march element state machine. The graph in Fig. 2 describes the state machine for a march algorithm.

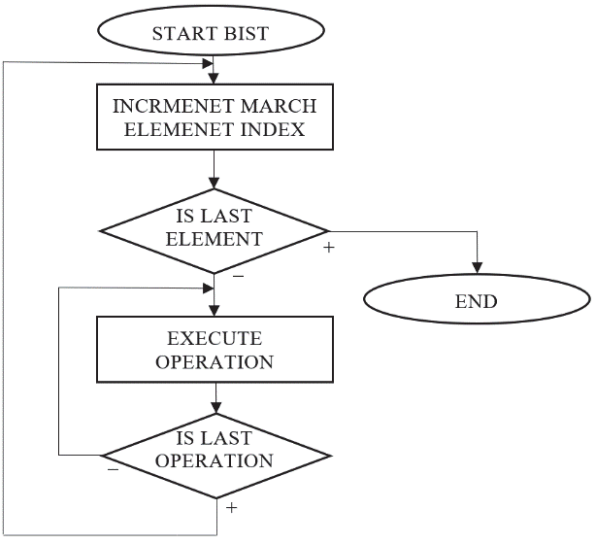

Fig 2. March element execution

Repair Mechanism. This feature exists if memory has an ability to be repaired. It is usually done via redundant cell groups. Knowing the configuration of redundant elements in a memory, the processor analyzes the location of captured failures and based on the results replaced the faulty rows/columns with redundant ones.

Specific Blocks. It is clear, that the proposed architecture for testing different types of memories cannot be absolutely the same with its main components. Therefore, there are some special purpose components which allow to use the main idea as a testing processor. Below is the description of these blocks.

Reference Calibration for MRAM. The logical "0"/"1" of this type of memory is defined as the amplification of the voltage of its bit-cell. For high resistance, the logical value is accepted as "1" and "0" for a low one. Because these resistances are close to each other, it is necessary to find the reference voltage for comparison of the output voltage of a bit-cell. Knowing the characteristics of the bit-cell behavior, the search mechanism can be suggested. It is usually implemented via provided registers as a memory input. Using the specified search algorithm, the best reference value can be found.

Memory Controller for External DRAM. In general, external dynamic memories have a special initialization and test sequence. Initialization sequence contains DRAM memory reset, some configuration registers and physical layer (PHY) reset. After initialization step, memory test should be asserted, but the test operations cannot be executed at once. There are more stages, which memory must be during the test [6,7] (i.e. activation, pre-charge, refresh, etc.). The memory controller allows to execute both protocols.

Conclusion. An architecture, which is compatible with different memories, is presented. The usage of the introduced BIST architecture for different memory types reduces the test time 0.85…3.21% for different memories with different sizes.

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Ա.Վ. ԲԱԲԱՅԱՆ, Գ.Ա. ԱԲԳԱՐՅԱՆ

ԸՆԴՀԱՆՈՒՐ ՆԵՐԴՐՎԱԾ ԹԵՍՏԱՎՈՐՄԱՆ ՃԱՐՏԱՐԱՊԵՏՈՒԹՅՈՒՆ ՀԻՇՈՂՈՒԹՅՈՒՆՆԵՐԻ ՀԱՄԱՐ

Առաջարկվում է ներդրված թեստավորման համակարգ, որը համատեղելի է տարբեր տիպի հիշողությունների համար: Ճարտարապետությունը կազմված է տարբեր ենթակառուցվածքներից, որոնք պատասխանատու են թեստավորման իրականացման համար, ինչպիսիք են՝ օպերացիաների կատարումը և թեստավորող ալգորիթմի պահպանումը որոշակի ֆորմատով: Ներկայացված են ճարտարապետության հիմնական բաղադրիչները: Այս համակարգը նվազեցնում է թեստավորման ժամանակը միջինում 0.85-3.21%-ով (կախված հիշողության ծավալից):

Առանցքային բառեր. ներդրված հիշողությունների թեստավորում, հիշողության անսարքություն, թեստավորող ալգորիթմ, համակարգ բյուրեղի վրա:

А.В. БАБАЯН, Г.А. АБГАРЯН

ОБЩАЯ АРХИТЕКТУРА ВСТРОЕННОГО САМОТЕСТИРОВАНИЯ ДЛЯ ПАМЯТИ

Предлагается общая архитектура встроенного самотестирования, которая подходит для различных типов хорошо известных видов памяти. Эта архитектура состоит из различных компонентов, которые отвечают за функции самотестирования, такие как выполнение операций и хранение алгоритмов в определенном формате. Описаны основные компоненты предлагаемой архитектуры. Данная архитектура снижает среднее время тестирования на 0,85...3,21% (в зависимости от объема памяти).

***Ключевые слова*:** самотестирование встроенной памяти, неисправность памяти, тестовой алгоритм, система на кристалле.