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THE TEMPERATURE DRIFT IMPACT COMPENSATION METHOD IN A HIGH-SPEED RECEIVER

The temperature drift impact compensation method in high-speed SerDes applications is proposed in this paper. The operating temperature range of modern VLSI circuits is -40...125°C. During the normal operation modes of integrated circuits, the ambient temperature may have big variations. Based on the SPICE simulation results, the impedance of MOSFET transistor varies in the range of -20% to 13% affecting the reference current generation circuits' temperature stabilities. Based on the proposed solution, an analog-to-digital conversion algorithm detects the variation of reference currents during the operation period of integrated circuits due to the temperature drift impact, and a digital algorithm compensates that impact.

The simulation results show that the variation of the total current due to the temperature drift is reduced by 22%. The solution is essential for the high-speed receivers in the sensitive applications such as UAV systems, automobiles. aircrafts where ambient temperature may vary drastically and in wide ranges.

Keywords: analog, comparator, operational amplifier, integrated circuit, IC, VLSI, reliability, degradation.

Introduction. High-speed (HS) interface IPs are widely used in modern applications. An example of such IPs are USB, D-PHY, M-PHY, HDMI etc. The most sensitive part of those interface IPs are the receiver (RX) parts. They should detect the signal transferred from transmitter (TX) PHYs through the transmission line. To minimize the signal reflection in (1) TX output stage, the transmission line and the receiver input stage impedances should be equalized:

$$\Gamma_{rx} = \frac{Z_{rx} - Z_0}{Z_{rx} + Z_0}, \quad (1)$$

where Z_{rx} represents the receiver input stage impedance, while Z_0 is the transmission line or the transmitter output stage impedance.

Modern RX IPs are using multi-PHY protocols where several serial data come from parallel TX IPs. For such applications, the RX input stage replicates in one place while the calibration bits for all lanes are generating simultaneously. For such an operation, external precision resistor outside the integrated circuit (IC) is placed [1]. An example presenting the block-diagram of the replica calibration

mechanism is presented in Fig.1. The PMOS transistor operating in the saturation region injects current to the external resistor. The current value is always equal to the reference voltage generated by the internal bandgap reference generator [2] divided to the resistance value of the external resistor and controlled by the operational amplifier [3] operating in a negative feedback mode. The current mirror architecture implemented by the Iref-Irext pair generates another reference current which flows through the replica circuit. The comparator and SAR logic digital algorithm is searches for the digital word code which better equalizes the voltage drops on the replica and external resistor circuits.

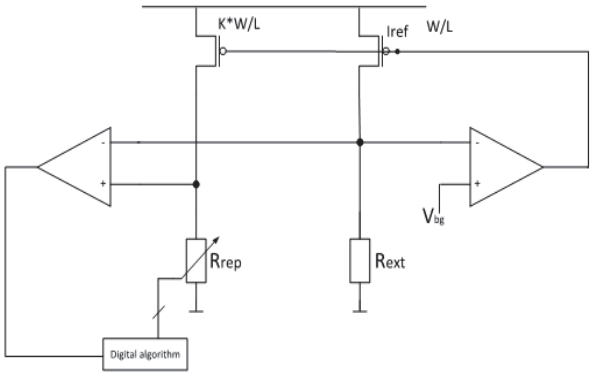

Fig. 1. The HS RX replica calibration mechanism

The I_{ref}-I_{rext} pair inside the calibration block operates as a stable current source generator. For other parts of HS RX where the stable currents play key roles, the design of current sources should be implemented by using the gate-source voltage of the PMOS devices and applying the corresponding W/L ratios for further references. For NMOS-based current sources, architecture redesign is necessary as shown in Fig.2.

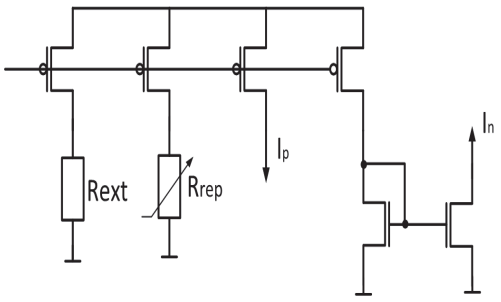

Fig. 2. Bias current generation

The problem description. The calibration mechanism of replica block is described in Fig.3.

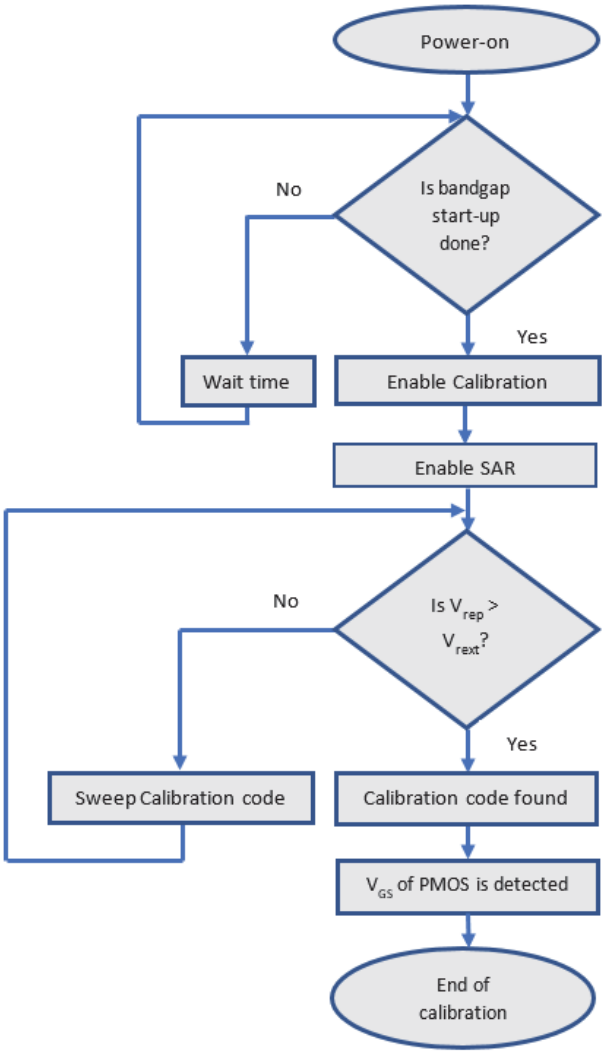

Fig. 3. The default mechanism of HS RX replica calibration

As presented above, the calibration algorithm realization is done once during the power-up of the HS RX. That means the required impedance value and the corresponding calibration code and Vgs voltage detections are done considering the current ambient temperature value. To determine the impact of the temperature drift on the calibrated impedance value, the following test has been implemented: the calibration mechanism enabled in case of -40˚C ambient temperature and after it done temperature has been shifted to the 125˚C. The maximum calibration code is

equal to 15 due to the 4-bit digital calibration mechanism. At -40˚C calibration code, the replica is equal to 13 as shown in Fig. 4. Replica impedance to the external resistor impedance ratio is 24 which results in 1.5 *mA* current flowing through the external resistor with 300 *mV* reference voltage applied on top of it. The current flowing through the replica should always be equal to 62.5 *uA* based on the impedance ratio value.

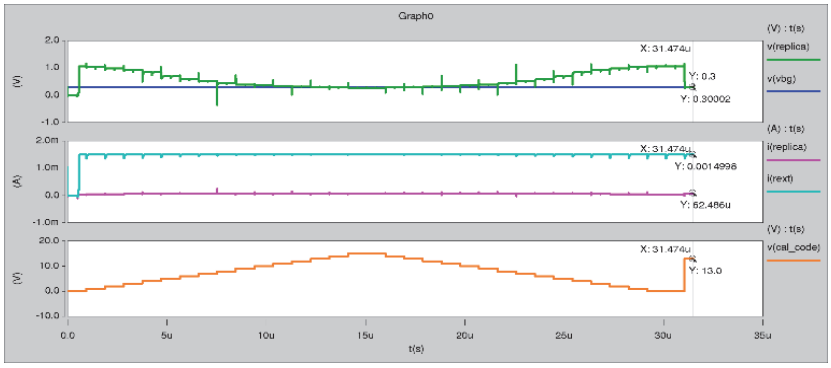

Fig. 4. Replica calibration at -40^{0}C

To evaluate the impact of temperature on the calibration process, the simulation with 125˚C has been performed. As shown in Fig.5, the calibration word code has been decreased to 9. The code difference is equal to 4.

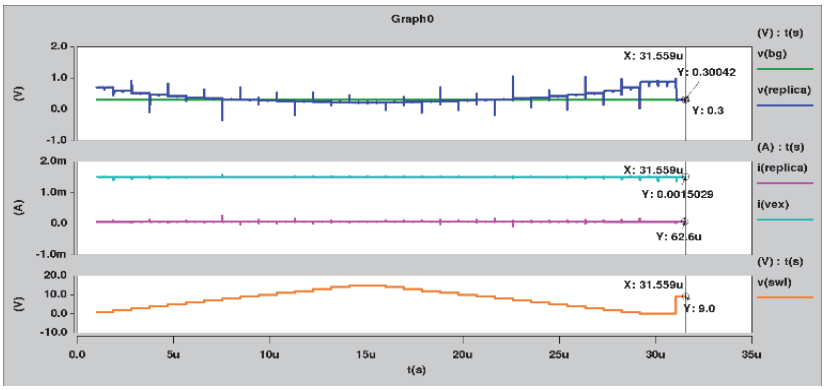

Fig. 5. Replica calibration at 125^{0}C

To evaluate the impact of temperature on the calibrated impedance value, simulation with a calibration code in the -40˚C case has been implemented. As shown in Fig.6 the impedance of the replica has been decreased from 4800 Ω to 3831 Ω which equals to more than 25% difference.

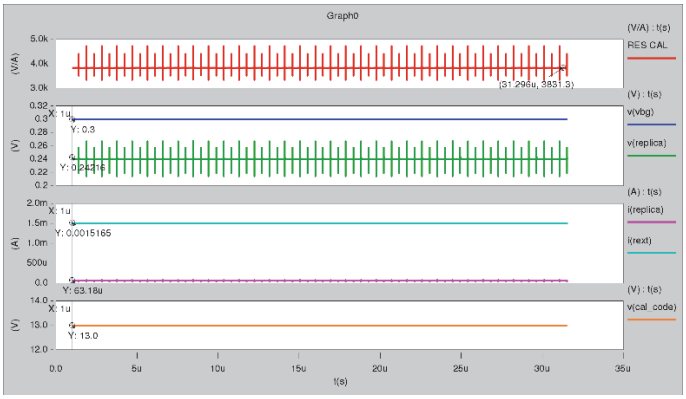

Fig. 6. Temperature drift impact on the impedance of HS RX replica

Technical specifications for the calibrated impedance variations are within the 10…10% range considering all the impact factors such as technology deviation, supply voltage variation, reference voltage uncertainty, etc. Considering the obtained results and the above-mentioned aggressors, the temperature drift impact on the impedance value should not exceed 5%. More variation will result out of specification terminated resistance values and will cause huge reflections of the transmitted HS data. So, it is necessary to reduce the variation by at least 20%.

The proposed solution. To solve the problem, we firstly need to have the clear description of the root cause of the problem. The root cause is the temperature impact on the calibrated impedance. Calibration process is time consuming and during the data transmission and restarting it during data transmission may impact on the reliability of the system. So the solution should be based not on the process itself but the digital algorithm which should track the voltage on the replica after the calibration ends and do the corresponding tuning when it exceeds the maximum or minimum allowable value.

Reg1 register keeps the code corresponding to voltage on replica and is periodically updated based on the sensed voltage on the replica (Fig. 7). Reg2 register keeps the LSB value calculated during the default calibration mechanism. Reg3 register keeps the converted digital code which corresponds to the voltage on top of replica during the default calibration mechanism. Reg4 register is used for doing the subtraction of the Reg3 and Reg1 register values. Reg5 register is used to keep the new calculated calibration word code. The digital algorithm realizes subtraction between the Reg1 and Reg3. If the replica voltage difference exceeds 1LSB calculated after the default calibration mechanism, it updates the Reg5 register value. Reg5 register output is tied to the calibration block and the algorithm can update the termination code without stopping the HS data transmission.

The Schematic implementation of the proposed solution is presented in Fig. 7. ADC [4] has 2 modes: default during which it samples the Replica voltage value and converts it into a digital code and tracking mode during which the system does not change the replica calibration value in case there is no temperature drift impact on the Replica voltage value. Data into the register can be written when the write enable – 'WE' signal goes to the high state. Output data can be captured when the read enable – 'RE' signal goes high.

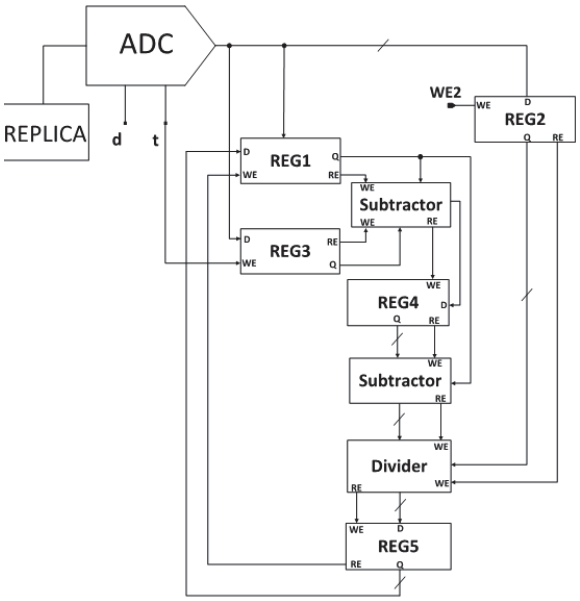

Fig. 7. The schematic implementation of the proposed solution

Results. Based on the proposed solution the new architecture is able to sense the variation of the voltage on the replica. Hspice Simulation [5] results performed by SAED14 nm [6] FinFet technology have shown great improvement. The temperature drift impact on the calibrated impedance value decreased from 25% to 3%.The results are summarized in the Table. Due to the architectural updates the total has been increased by 50% and the total power consumption has been increased by 10%. While taking into account the fact that the HS RX areas are around 20 times bigger compared to the calibration area, the overall impact on the IC area will be less than 3%. Meanwhile the total power consumption is around 10 times bigger than the calibration power, so the total power, consumption increase will be around 1%.

Table

OBTAINED RESULTS

	Without proposed solution	*With proposed solution*
T-drift impact	25%	3%
Occupied area	1000 um^2	1500 um^2
Power consumption	3.6 mW	3.96 mW

Conclusion. A temperature drift impact reduction method in high-speed receiver applications is proposed in this paper. The new architecture of impedance calibration system has been designed. The obtained results have shown around 22% improvement of the temperature drift impact on the impedance calibration. This will result in less reflection during high speed data transmission and better impedance matching between the receiver and transmission line. This architecture can be easily integrated in modern automotive designs.

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ՋԵՐՄԱՍՏԻՃԱՆԻ ՇԵՂՄԱՆ ՓՈԽՀԱՏՈՒՑՄԱՆ ԵՂԱՆԱԿԸ ԲԱՐՁՐ ԱՐԱԳՈՒԹՅԱՄԲ ՀԱՂՈՐԴԻՉ ՀԱԳՈՒՑՑՈՒՄ

Ներկայացված է շրջակա միջավայրի ջերմաստիճանի փոփոխության ազդեցության նվազարկման մեթոդ արագագործ տվյալների հաջորդական փոխանցման կապերում: Ժամանակակից ինտեգրալ սխեմաներում աշխատանքային ջերմաստիճանը սահմանվում է −40-ից 125°C միջակայքում: Մինչդեռ աշխատանքային ռեժիմում գտնվող ինտեգրալ սխեմաների արտաքին միջավայրի ջերմաստիճանը կարող է դրսևորել մեծ տատանումներ: SPICE մոդելավորման արդյունքները ցույց են տվել, որ ՄՕԿ տրանզիստորի դիմադրությունը փոփոխվում է -20%-ից +13% միջակայքում, որի հետևանքվ նվազում է հենակային հոսանքի աղբյուրների կայունությունը: Առաջարկվող լուծման շրջանակներում մշակված ալգորիթմը և իրականացման սխեման ցույց են տալիս արտաքին ջերմաստիճանի փոփոխության արդյունքում ի հայտ եկող հենակային հոսանքի փոփոխությունները և անալոգաթվային կերպափոխման հիման վրա կոմպենսացնում են այդ ազդեցությունները:

Մոդելավորման արդյունքները ցույց են տվել, որ ջերմաստիճանի տատանման հետևանքով առաջացող հենակային հոսանքի փոփոխությունը նվազեցվել է 22%-ով: Առաջարկված լուծումը առանցքային դեր ունի արագագործ ընդունիչներում, որոնք օգտագործվում են զգայուն համակարգերում՝ ԱԹՍ-երում, մեքենաշինության մեջ, օդանավերում, որտեղ շրջակա միջավայրի ջերմատիճանը կարող է կտրուկ փոփոխվել մեծ միջակայքերում:

Առանցքային բառեր՝ անալոգ, համեմատիչ, օպերացիոն ուժեղարար, ինտեգրալ սխեմա, ԳՄԻՍ, վատացում:

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МЕТОД КОМПЕНСАЦИИ ТЕМПЕРАТУРНОГО ДРЕЙФА В ВЫСОКОСКОРОСТНОМ ПРИЕМНИКЕ

Предлагается метод компенсации воздействия температурного дрейфа в высокоскоростных приложениях SerDes. Диапазон рабочих температур современных сверхбольших интегральных схем (СБИС) составляет -40...125°C, в то время как в нормальных режимах работы интегральных схем температура окружающей среды может сильно колебаться. На основе результатов моделирования SPICE импеданс MOSFET-транзистора варьируется в диапазоне от -20% до 13%, что влияет на температурную стабильность схем генерации эталонного тока. На основе предложенного решения алгоритм аналого-цифрового преобразования обнаруживает изменение опорных токов в течение периода работы интегральных схем из-за воздействия температурного дрейфа, а цифровой алгоритм компенсирует это влияние.

Результаты моделирования показали, что изменение полного тока из-за температурного дрейфа уменьшилось на 22%. Предложенное решение необходимо для высокоскоростных приемников в таких приложениях, как системы БПЛА, автомобили, самолеты, где температура окружающей среды может колебаться в больших пределах.

Ключевые слова: аналог, компаратор, операционный усилитель, интегральная схема, сверхбольшие интегральные схемы (СБИС), деградация.