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HIGHLY EFFICIENT HIGH-PERFORMANCE SENSE AMPLIFIER DESIGN IN NANOSCALE CMOS TECHNOLOGIES

Nowadays the tendency of design of integrated circuits goes in the power and area reduction way. Power reduction requires usage of low-power design methodologies. The latter, in turn, requires decreasing the supply voltage values. This impacts on the stability of the sensitive parts of analog and mixed-signal integrated circuits. Sense amplifiers are widely used in modern integrated circuits. They play a key role in memory circuits and act as the most complex parts from the standpoint of designing. A stability improvement method of those circuits in modern nanoscale integrated circuits is proposed in this paper. A new sense amplifier architecture has been proposed in which the current - controlled bandwidth has been provided highly efficient power consumption results. Besides the current-controlled architecture has ensured the minimization of comparator offset dependency on the power supply value.

Keywords: sense amplifier, clocked comparator, sensitivity, current source, complementary metal-oxide-semiconductor (CMOS).

Introduction. Comparators or sense amplifiers are an essential part of analog-to-digital conversion circuits, memory applications, high-speed receiver systems, etc [1]. The main role of those blocks is to convert the voltage difference between the two inputs to the binary logic level signals. In Fig. 1 the symbol view with input and output signals' definitions is presented. The Vout output signal goes to the logic high level if the voltage applied on the positive node is higher than the applied value on the negative one. To be able to bring the output signal level to the supply values, the CMOS logic is used as an output stage [2].

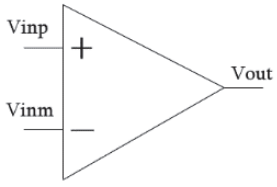

Fig. 1. The comparator symbol view

The block is able to work in several modes: single-to-single, differential-to-single, single-to-differential or differential-to-differential. The most complex situation is when the input signal is single-ended and the input voltage swing is two

times lower than in differential input signalling scenarios. The realization of this scenario requires a fixed reference voltage to be applied on the positive input. The complexity of the problem requires high open-loop gain support and low dependency of supply values. In parallel to the abovementioned limitaions the reference voltage should remain stable when power supply varies [1-3].

Problem description. Modern high-speed applications such as are memory circuits, special purpose input-output circuits, etc should support at least 1 *GHz* data reception and conversion speeds. Data reception through the transmission channels reduces the swing of the transferred signals. Lossless operation in parallel to the low power consumption necessity requires an increase of stability of sense amplifiers by decreasing the dependency of its main parameters on supply values such as open-loop gain, power consumption, sensitivity, etc.

The main problem to which the research is targeted is the development of new design strategies and corresponding architecture which will guarantee the block capability to convert the input voltage difference with a higher than 2 *mV* swing.

Clocked comparators. Such comparators are the most commonly used types of sense amplifiers which are triggered by a synchronous clock. The clock signal source is the phase-locked-loop application which exists in any precision high-speed application. The output signal decision is realized by doing the amplification of input voltage difference during the rising or falling edge of a clock signal. Fig. 2 represents a block diagram of a clocked comparator [2-4]. The first stage is the main amplification part of the block. So, the performance and accuracy of the data sensing mainly depends on this part. The second regenerative latch stage consists of 2 back-to-back inverters and is used for further amplification of the output voltage of the first stage up to the CMOS level. After the data conversion comparator enters the reset mode. In that mode, both outputs of the sense amplifier are at the same logic levels. To avoid comparison algorithm failures, the third R-S latch stage is used which keeps the previous state when both inputs are equal.

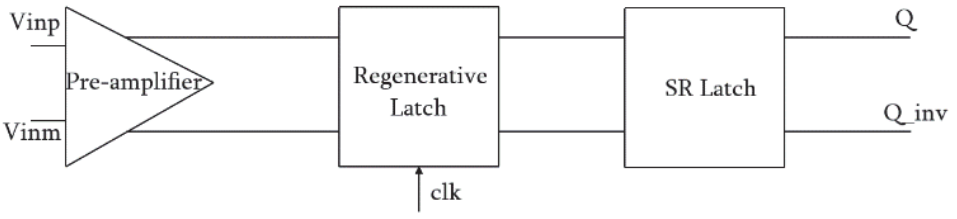

Fig. 2. The block diagram of the clocked comparator

The circuit level implementation of the sense amplifier is presented in Fig.3 [4]. During the rising edge of the clock signal, the M4 and M5 transistors are open, M2-M6 and M3-M7 NFET-PFET pairs act as regenerative latch stage. The M0 and M1 input pair acts as a common-source amplifier with regenerative latch load at the top [5]. During the clock signal rise, those two common source stages are amplifying the difference between the input voltages. The amplified signals further increase their values propagation through the M2-M3 common gate stage. At the end, the voltages at the bottom of M6 and M7 devices receive logic 0 or 1 values, thus realizing the comparison process during this mode.

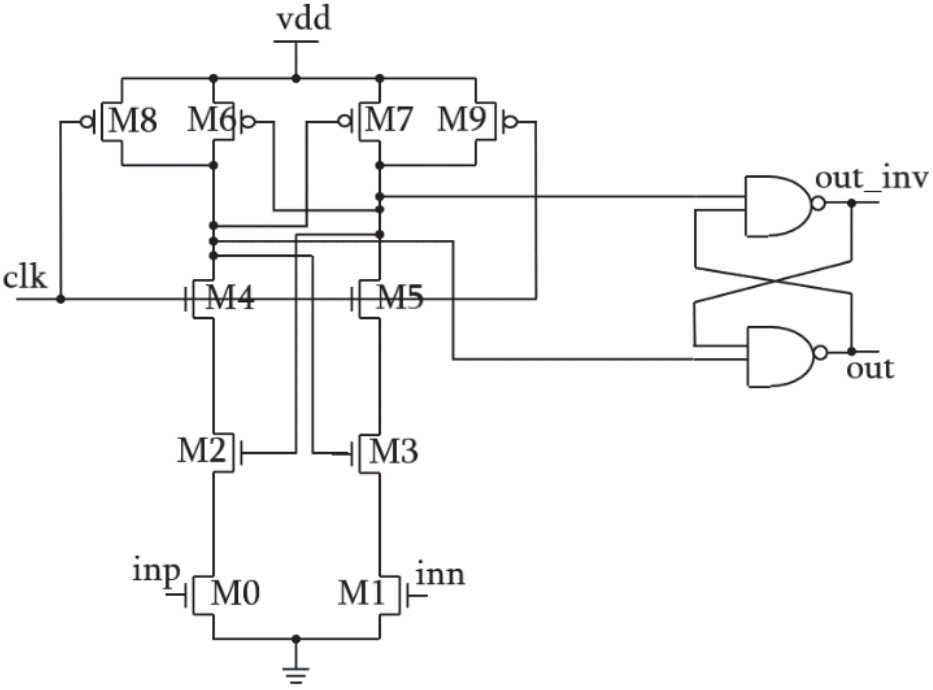

Fig. 3. The sense amplifier circuit

In the reset mode the clock signal goes to cutting the M6 and M7 devices off and turning on the M10 and M11 ones connecting the output signals to the power. R-S latch keeps its previous state during the whole reset mode period.

Based on the SPICE simulation results performed in SAED14 *nm* FinFet technology, the sensitivity of the sense amplifier with such an architecture strongly depends on the data rate and the supply voltage values and is not able to meet the 2 *mV* target specification in higher bitrates. The results are shown in Table 1.

Table 1

Sense amplifier sensitivity simulation results of the clocked comparator

Supply voltage (*V*)	Clock frequency (*MHz*)	Sensitivity (*mV*)
VDD = 0.8	10	1.2
	2000	3.1
	5000	6.2
VDD = 0.72	10	1.8
	2000	6.3
	5000	8.2
VDD = 0.88	10	0.8
	2000	2.9
	5000	4.7

The proposed solution. To reduce the dependency of the comparator functionality on the power supply value and the frequency without impacting the block performance, a new architecture has been designed and provided in Fig.4. The block has an always enabled current source branch organized by the M0-M1 NMOS pairs wotking in the saturation region. In parallel to the main current source branch, 4 new branches have been added whose outputs are connected to the same node as the M1 drain. In a low bitrate mode, when the data signal frequency is in the range of 1…10 *MHz*, the M1 current is enough to ensure the proper functionality and sensitivity. When the data reception frequency stands higher the corresponding current sources increase the bandwidth of the amplifier. The ratio between the channel widths of M1 and M1_1 is equal to 1, while the ratio of M1_2 is 5, M1_3 is 10, M1_4 is 20. When the data bitrate is betweent the 0.1 *Gbps* and 0.5 *Gbps* the en_05G signal goes high, enabling the current to pass through the M1_2 current source NMOS. If the bitrate is between the 0.5 *Gbps* and 1 *Gbps* the en_1G signal goes high, enabling the M1_3 current source to pass through the path and so on.

The main advantage of such architecture is its current controllability. There is no need to force the amplifier to work at highest current consumption condition to be able to support all data rates. As a result, in each data rate condition, the proper amount of current flows through it, increasing the efficiency without any negative impact on the performance. Besides that, the dependency of the comparator sensitivity reduces due to the constant current value and the more independent transconductance of input common source stages.

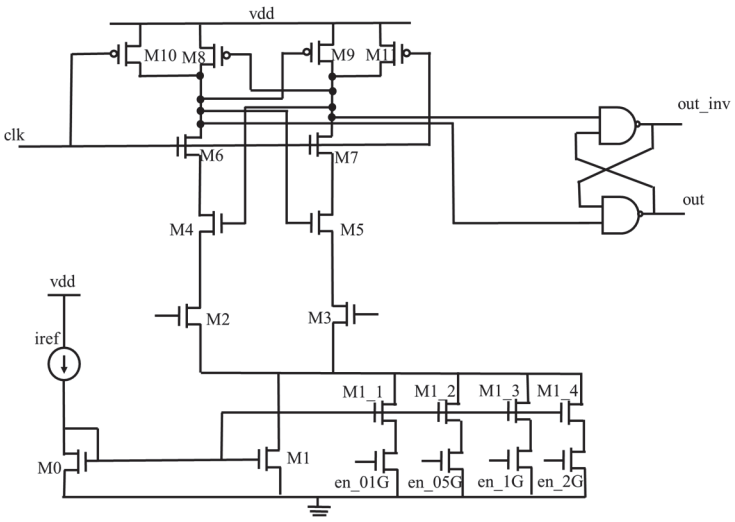

Fig. 4. The proposed architecture of sense amplifier

To verify the functionality of the comparator the SPICE transient simulation with 5 *GHz* data rate in SAED14 *nm* FinFet technology has been implemented. To check the offset value over the technology deviations Monte Carlo simulation has also been performed in the 4.5 sigma range. The results are shown by Q-Q plot view in Fig.5. The comparator offset value is less than the 1 *mV* in ±4.5 sigma range.

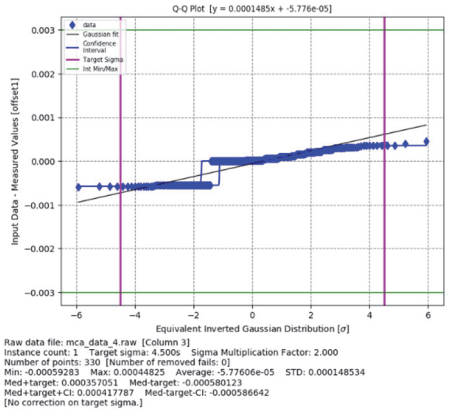

Fig. 5. The Q-Q plot of Monte Carlo offset simulation results

To achieve such results, the channel length of the current source branches should be enough to compensate the channel length modulation without impacting the saturation margins of those devices. This requires proper W and L detection. For the considered technology node, the minimum L is 0.8 *um* and the minimum W is 2 *um*. In parallel to this approach, the input amplifier stages have been designed

by considering the tradeoff between the amplifier offset over Monte Carlo and the block bandwidth which limits the big sizes of those stage.

Summary. The simulation results and comparison with the existing architecture has been provided in Table 2. The sensitivity of the amplifier has been decreased from 8.2 *mV* to 0.9 *mV*. Meanwhile the power consumption has been deceased by 50 times in lower data rate conditions and 2.5 times in 2 *GHz* data rate case. The dependency of the offset sensitivity on power supply value has been dramatically decreased due to the proposed architecture.

Table 2

Comparison between the existing and proposed sense amplifier architectures

Supply Value (*V*)	Data Rate (*MHz*)	Sensitivity (*mV*)		Power consumption (*uW*)	
		Existing architecture	Proposed architecture	Existing architecture	Proposed architecture
0.8	10	1.2	0.2	500	10
	2000	3.1	0.4	500	200
	5000	6.2	0.8	500	500
0.72	10	1.8	0.25	500	10
	2000	6.3	0.6	500	200
	5000	8.2	0.9	500	500
0.88	10	0.8	0.15	500	10
	2000	2.9	0.32	500	200
	5000	4.7	0.71	500	500

Conclusion. The highly efficient high-performance sense amplifier architecture has been proposed in this paper. The current controlled bandwidth implemented by the digitally controlled switches and the biased transistors operating in saturation regions have improved the sensitivity and power consumption efficiency several times. Simulations have been performed by the HSPICE simulator in SAED14 *nm* FinFet technology. The schematic design has been implemented in Custom Compiler environment. The structure proposed in the paper can be easily integrated in modern analog-to-digital conversion application, high-speed receivers, memory systems, etc. The reduction of power consumption allowed the interoperability in mobile applications as well. The achieved area, power consumption and sensitivity results meet the technical specifications of modern latched comparators. The latter has been tested during the design of different types of high-speed analog-to-digital convertor architectures and shown its high reliability and proper functionality.

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ԲԱՐՁՐ ԱՐԴՅՈՒՆԱՎԵՏՈՒԹՅԱՄԲ ԵՎ ԱՐԱԳԱԳՈՐԾՈՒԹՅԱՄԲ ԶԳԱՅՈՒՆ ՈՒԺԵՂԱՐԱՐԻ ՆԱԽԱԳԾՈՒՄԸ ՆԱՆՈՉԱՓԱԿԱՆ ԿՄՕԿ ՏԵԽՆՈԼՈԳԻԱՅՈՎ

Ներկայումս ինտեգրալ սխեմաների նախագծման գործընթացը միտված է էներգասպառման նվազեցմանը և դրանց զբաղեցրած մակերեսի փոքրացմանը: Էներգասպառման փոքրացումը պահանջում է ցածր էներգասպառմամբ նախագծման մեթոդների կիրառում: Վերջինս առաջացնում է սնման լարման արժեքի նվազեցման անհրաժեշտություն, ինչն իր հերթին անալոգային և խառը ազդանշանային ինտեգրալ սխեմաների զգայուն հանգույցների կայունության վրա ունի բացասական ազդեցություն: Զգայուն ուժեղարարները լայնորեն օգտագործվում են ժամանակակից ինտեգրալ սխեմաներում: Դրանք առանցքային դեր են խաղում հիշողության սխեմաներում և նախագծման տեսանկյունից հանդիսանում են ամենաբարդ մասը: Առաջարկվում է նանոչափական ինտեգրալ սխեմաներում զգայուն ուժեղարարների կայունության բարձրացման մեթոդ: Նախագծված նոր ճարտարապետությունում հոսանքի արժեքի կառավարման հաշվին հաջողվել է բարձրացել է զգայուն ուժեղարարի էներգասպառման արդյունավետությունը՝ միաժամանակ ապահովելով սխեմայի լարման շեղման արժեքի՝ սնման լարումից ավելի ցածր կախվածություն:

Առանցքային բառեր. զգայուն ուժեղարար, սինքրոն համեմատիչ, զգայնություն, հոսանքի աղբյուր, կոմպլեմենտար մետաղ-օքսիդ-կիսահաղորդիչ (ԿՄՕԿ):

Г.Д. ГРИГОРЯН, Т.Д. ГРИГОРЯН

РАЗРАБОТКА ВЫСОКОЭФФЕКТИВНОГО И ВЫСОКОСКОРОСТНОГО ЧУВСТВИТЕЛЬНОГО УСИЛИТЕЛЯ С НАНОРАЗМЕРНОЙ ТЕХНОЛОГИЕЙ КМОП

В настоящее время процесс проектирования интегральных схем (ИС) направлен на снижение энергопотребления и уменьшение занимаемой площади. Снижение энергопотребления требует применения методов проектирования с низким энергопотреблением. Последнее вызывает необходимость снижения значения напряжения питания, что отрицательно сказывается на стабильности чувствительных узлов аналоговых и смешанных сигнальных ИС. Чувствительные усилители широко используются в современных ИС. Они играют ключевую роль в схемах памяти, являются наиболее сложной частью с точки зрения проектирования. В статье предлагается метод повышения стабильности чувствительных усилителей в нанометровых интегральных схемах. В предлагаемой архитектуре эффективность энергопотребления чувствительного усилителя была увеличена за счет управления значением тока, обеспечивая в то же время более низкую зависимость значения отклонения напряжения от напряжения питания.

Ключевые слова: чувствительный усилитель, синхронный компаратор, чувствительность, источник тока, комплементарный металл-оксид-полупроводник (КМОП).