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THE LOW POWER RESISTANCE CALIBRATION METHOD WITH THE EXTERNAL CAPACITOR

Companies are continuing to push the boundaries on new features and functionality all packed into portable and battery powered devices. For this kind of products, improving the battery life by minimizing power consumption is very important to user applications.

SERDES systems are wildly used for communications with low power consumption. Transmitter output and receiver input resistance calibration is one of the main problems in SERDES systems. Calibration with an external resistor is widely used in modern SERDES IPs.

The calibration method with an external capacitor is presented. The proposed method has up to 3 times lower power consumption compared with calibration with the external resistor. The solution can be used in low power designs.

Keywords: calibration, external resistor, capacitor, reflection.

Introduction. SERDES is the most fundamental building block of a physical layer for chip-to-chip interconnect systems. To have a robust link, a careful design of all building blocks is required.

With increasing the operating frequency, new problem appear during the design process. One of these problems is the distortion of the signal during transmission. To have a reliable data transmission, a robust link must be established. One of the limiting factors to increase the operating frequency is signal reflection. Because of reflections, the transmitted data can be unrecoverable by the receiver. To avoid reflection during transmission, the resistance calibration of the transmitter and receiver is performed.

For signal reflection minimization, the Tx output stage, the transmission line and the receiver input stage impedances should be equalized:

$$\Gamma = \frac{z_{rx} - z_0}{z_{rx} + z_0}. \quad (1)$$

As the SERDES systems are becoming more advanced, the complexity and speed of circuitry is increasing resulting in high power consumption.

The power equation (2) contains components for dynamic and static power [1] (Fig. 1). The value of each power component is related to the peak current, leakage current, transition time, supply voltage, etc.

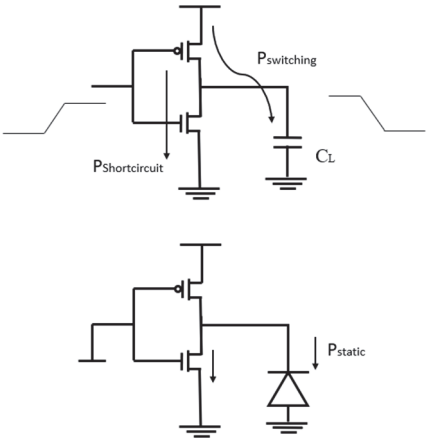

Fig. 1. Power consumption components

$$P_{total} = \alpha f C_L V_{DD}^2 + V_{DD} I_{leakage} + t\, V_{DD} I_{peak}, \quad (2)$$

where f is the switching frequency of the gate and C_L is the load capacitance driven by the inverter. In circuit design, engineers attempt to design high-performance circuits that dissipate low power. However, high-speed implies a large frequency and requires large transistors with a large capacitance. This unfortunately increases the overall power dissipation. α is the factor showing the switching activity. As most gates do not switch with every clock cycle, α parameter is used to include the switching activity of the CMOS gate. During transition there is a t interval where both gates of the inverter are open. The power dissipated in this period is calculated by multiplying the peak current (I_{peak}) with supply voltage and time interval t.

Available architectures. In modern SERDES IPs, impedance calibration is performed with precise external resistor usage [2]. The block diagram of the available calibration method is presented in Fig. 2.

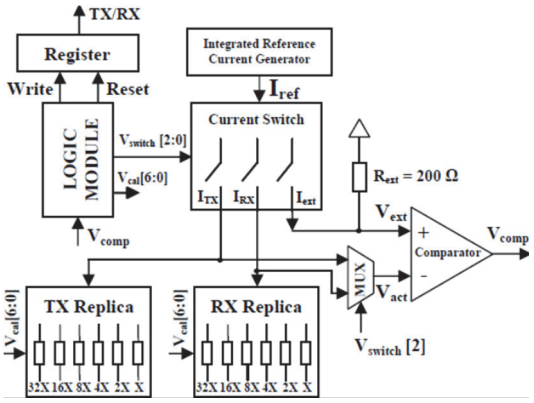

Fig. 2. The impedance calibration method with the external resistor

The working principal of this architecture is as follows. Logic module is changing the code for replica blocks. With increasing the code amount the parallelly connected resistors are rising in replica, resulting in overall smaller resistance. The positive input of the comparator is connected to the external resistor. With increasing the code, Vact voltage decreases. When Vact becomes smaller than the Vext output, the comparator is switching from 1 to 0 and logic module saves the calibration word. Power consumption of this circuit for the typical corner is 12 *mW*. One of the main contributors is the external resistor.

The proposed method. The circuit of the proposed method is shown in Fig. 3. The vref voltage is generated via bandgap reference [3] and has ~1% variation considering a wide range of PVT corners.

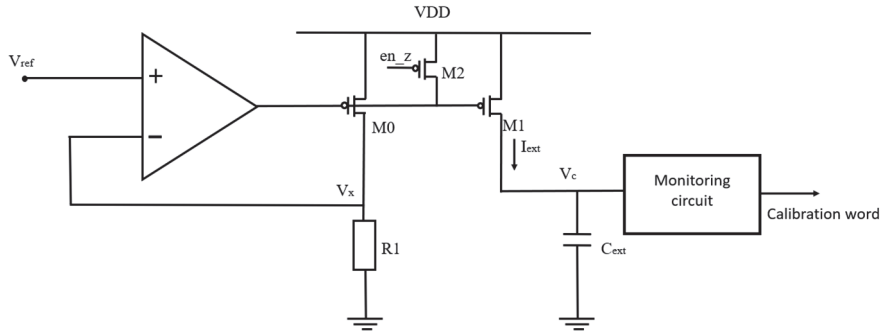

Fig.3. The proposed method circuit

During the design of the proposed circuit, several things must be considered. Feedback point must be as close to the resistor as possible to minimize the routing resistance impact on the overall results. The capacitor is disconnected via transistor M2. The designed circuit also provides information about the resistor type. This information can be used to do manual adjustments after fabrication.

The vref voltage is 400 *mV*. One of the main components of the proposed circuit is the operational amplifier. Vx voltage must be as close to 400 as possible. For that the amplifier must have a gain bigger than 40 *DB* with over corner simulation. HSPICE simulation shows [4] dc gain for typical best and worst corners presented in Fig. 4.

The simulation of the amplifier confirms that the voltage of Vx has ~2% variation. So Iext current mostly depends on the R1 resistor. If after fabrication tests show that Iext current is lower than 200 *uA* it becomes obvious that the resistance is bigger than it is in the typical case.

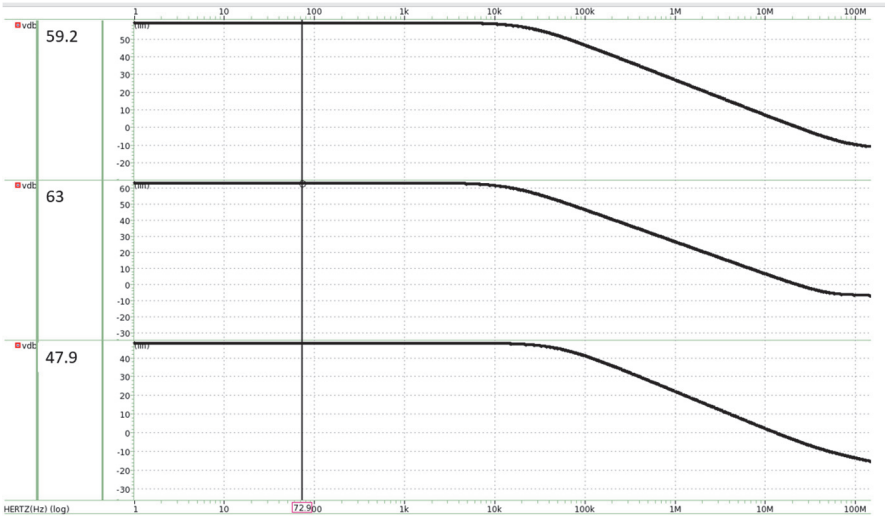

Fig. 4. AC simulation results for the amplifier

The working principle is as follows. With amplifier Vx set to 400 *mV,* the external capacitor is charged with Iext current. The counter from monitoring the circuit counts until the capacitor is charged up to 95% of VDD. By using the counter value, the digital logic adjusts the calibration word. The block diagram in Fig. 5 shows the steps of the proposed architecture.

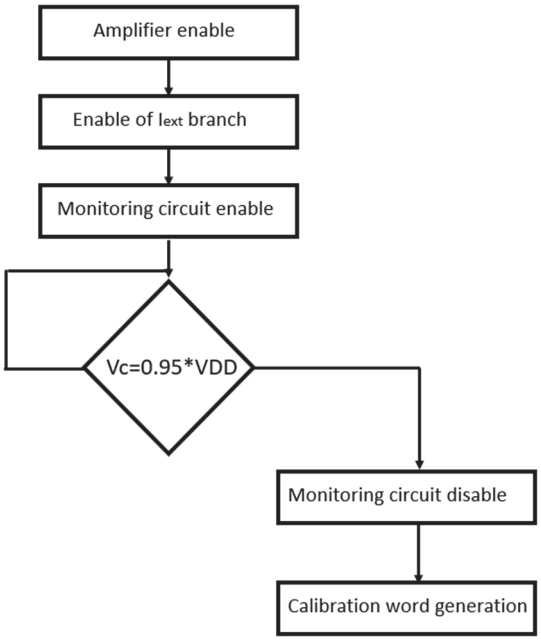

Fig. 5. A block diagram of the proposed circuit

The table below shows the calibrated resistance value for the proposed and available methods. In modern IP, the acceptable variation of calibrated resistance varies from 40 to 60 *Ohm*. Power consumption for typical corner is 4 *mW*.

Table

Comparison with available architecture

Value	The proposed method, *Ohm*	The available method, *Ohm*
Typical	49.4	50.1
Min	45.3	47.7
Max	53.6	51.2

Conclusion. Resistance calibration is an essential part of the SERDES system. It is a power consuming process. By using the proposed method, the usage of the external resistor is omitted. By using the proposed method, power consumption is lower ~3 times. The calibrated resistance values are more shifted than in the external resistor case. But this is not a problem because the calibrated resistance value is in the defined range. The method can be used in modern SERDES systems.

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Ռ.Հ. ՄՈՒՍԱՅԵԼՅԱՆ

ՑԱԾՐ ԷՆԵՐԳԱՍՊԱՌՄԱՄԲ ԴԻՄԱԴՐՈՒԹՅԱՆ ԿԱՐԳԱԲԵՐՄԱՆ ՄԵԹՈԴ ԱՐՏԱՔԻՆ ՈՒՆԱԿՈՒԹՅԱՄԲ

Կազմակերպությունները շարունակում են ավելացնել շարժական, մարտկոցով աշխատող սարքավորումների նոր գործառույթի և հնարավորությունների սահմանները: Այդ տեսակի արտադրանքների համար մարտկոցի կյանքի տևողության լավացումը՝ հզորության ծախսի նվազեցման հաշվին, շատ կարևոր է օգտատերերի տարբեր կիրառություններում:

SERDES համակարգերը լայնորեն օգտագործվում են ցածր էներգասպառմամբ հաղորդակցության մեջ: Հաղորդչի ելքային դիմադրության և ընդունիչի մուտքային դիմադրության կարգաբերումը SERDES համակարգերի գլխավոր խնդիրներից մեկն է: Արտաքին դիմադրության կիրառմամբ կարգաբերումը լայնորեն կիրառվում է ժամանակակից SERD-ES մտավոր սեփականություններում:

Ներկայացված է կարգաբերման մեթոդ՝ արտաքին ունակության կիրառմամբ: Առաջարկվող մեթոդն ունի մինչև 3 անգամ ավելի ցածր էներգասպառում՝ համեմատած արտաքին դիմադրության կիրառմամբ կարգաբերման հետ: Լուծումը կարող է կիրառվել ժամանակակից ցածր հզորություն սպառող նախագծերում:

Առանցքային բառեր. կարգաբերում, արտաքին դիմադրություն, ունակություն, անդրադարձ:

Р.О. МУСАЕЛЯН

МАЛОМОЩНЫЙ МЕТОД КАЛИБРОВКИ СОПРОТИВЛЕНИЯ С ВНЕШНИМ КОНДЕНСАТОРОМ

Компании продолжают расширять границы возможностей и функциональности портативных устройств и устройств с батарейным питанием. Для продуктов такого типа увеличение срока службы батареи за счет минимизации энергопотребления очень важно для пользовательских приложений.

Системы SERDES широко используются для связи с низким энергопотреблением. Калибровка выходного сопротивления передатчика и входного сопротивления приемника - одна из основных проблем в системах SERDES. Калибровка с помощью внешнего резистора широко используется в современных SERDES системах.

Представлен метод калибровки с внешним конденсатором. Предлагаемый метод потребляет до трех раз меньше энергии по сравнению с калибровкой с внешним резистором. Решение может быть использовано в маломощных конструкциях.

Ключевые слова: калибровка, внешний резистор, конденсатор, отражение.