ISSN 0002-306X. Proc. of the RA NAS and NPUA Ser. of tech. sc. 2021. V. LXXIV, N1

UDC 621.382 **MOCROELECTRONICS**

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A REAL NUMBER MODELING FLOW OF AN ANALOG-TO-DIGITAL CONVERTER

The process of real number modeling of an ADC converter in SystemVerilog environment is introduced. The analog macros which are described in digital environment usually cause problems during verification as they are not properly described. The digital models are not able to show analog signals; hence they are not able to have a high verification coverage. The real number modeling (RNM) suggests a solution which significantly increases the analog verification coverage and keeps the simulation time lower compared to the existing alternatives like Co-simulation. The RNM simulation runs 2 or more times faster than the equivalent Spice simulation.

Keywords: analog-to-digital converter, SystemVerilog, Universal Verification Methodology (UVM), Real Number Modeling (RNM), Co-simulation.

Introduction. The moder digital cells which are described in Verilog/VHDL languages are usually verified in reusable digital environments (for example, universal verification methodology [1] or UVM). The verification cannot have full functional coverage as the checked systems are usually very big and the computational resources are not able to run all possible signal combinations in a reasonable amount of time. So, in order to soften the lack of resources, the testbenches in such environments are usually randomized, meaning that the input signals are getting initiated and change randomly during every simulation. Such approach helps to achieve as high functional coverage as possible.

The problems start to pop when analog macros are introduced into a digital environment. The digital description of an analog cell is just a patch in the environment, which does not have any functionality of the original and is just installed, so the rest of the environment can continue working. Verification of such environment does not cover the analog functionality of the macro, as well as the interfacing errors connected with macro-neighboring digital cells.

In order to solve problems mentioned above, the Co-simulation methodology is usually used. In Co-simulation, the analog part of the design is instantiated as a Spice cell and the digital part - as Verilog/VHDL cell [2]. The whole environment then is driven by a mixed-mode simulator [3] which allows to combine two conceptually different models in one simulation. Thus, the analog functionality of

the cell is described properly and the errors which are missed in the digital environment can be caught here.

However, the Co-simulation also has several disadvantages. The main problem with it is that the Co-simulation cannot afford a big number of simulations, because the analog part of the environment is very resource consuming, hence the simulation time is a lot bigger compared to a fully digital environment. So, the Co-simulation can significantly reduce the number of errors connected with analog functionality, however due to the lack of regression-based runs, its overall functional coverage remains low.

To avoid the mentioned problems, the real number modeling is used instead of Co-simulation [4]. The concept is to describe the required analog models in the SystemVerilog language and use them during UVM environment verification instead of Spice models [5]. The SystemVerilog language is not intended for real number modeling, however due to its flexibility it fits all the requirements. The SystemVerilog is used as a base for RNM because the most widespread digital environment verification tool is the UVM. It is also written in SystemVerilog and is easily compatible with the Verilog language. The user can replace the digital models with RNM without additional tuning.

Real number model-based environment runs much faster than the one based on Co-simulation, hence allowing to keep the randomized regressions in place which greatly increases the verification coverage compared to the fully digital UVM environment. Additionally, the verification coverage is increased even more by the fact that the suggested real number models also provide PVT randomization.

Problem description. There are several common submodules which were implemented and used during the ADC design:

- bit-to-analog signal converter;
- resistance ladder;
- analog comparator.

The presented RNM ADC is based on the flash ADC circuit [6] which is initially described in HSPICE [7] circuit simulation tool. The main advantage of such ADC is the high speed and simple circuitry. The main disadvantage is the number of comparators resulting in more occupied area and offsets. The voltage buffer connected to the output can be accounted while it is not mandatory in terms of RNM vs HSPICE verification.

The architecture of a 16-bit flash ADC which is shown in Fig.1 has been implemented for both SystemVerilog and Spice formats for further research.

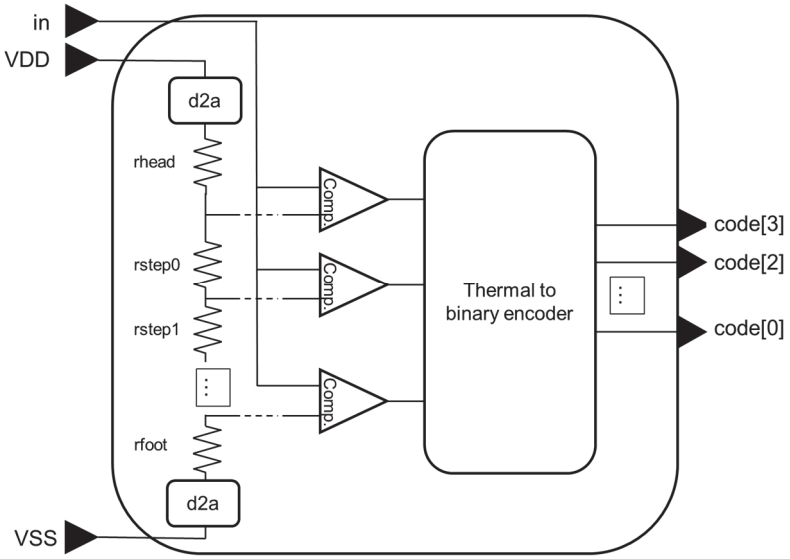

Fig. 1. ADC RNM model block scheme

The target is the creation of a functional RNM ADC model and its verification with comparison of RNM ADC signals against the equivalent HSPICE model's signals. Several suggested RNM milestones should be met during model creation (described in detail below). The RNM and Spice models should be simulated using the same SystemVerilog testbench.

Submodule descriptions. The first RNM submodule is the bit-to-analog signal converter, which acts as an interface cell between RTL and RNM functionalities. It converts a digital signal to an analog voltage dictated by conversion laws. The laws are described by the group of variables listed below:

"rise_time" – shows the duration of the rising edge;

"fall_time" – shows the duration of the falling edge;

"high_volt" – shows the voltage level of logical 1 value;

"low_volt" – shows the voltage level of logical 0 value;

"x_state" – shows the voltage level of logical X state;

"z_state" – shows the voltage level of logical Z state.

As shown in Figures 2 and 3, configuration can be changed during the simulation and their effects (rise/fall edge durations, high/low voltage levels, etc.) will be applied to the output signal immediately.

The second RNM submodule is the resistance ladder with 16 analog outputs. They are resoluted based on the VDD value. There are 18 resistors in the ladder – the "rhead" and "rfoot" limit the analog signal's conversion range from up and down. The "rstep" resistors are responsible for the reference voltage levels.

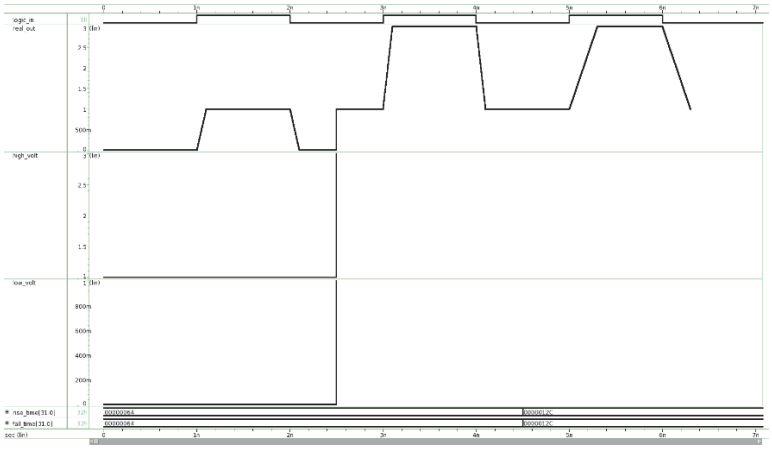

Fig. 2. The ADC "rise_time", "fall_time", "high_volt", "low volt" configuration variables and their effects on the output signal in SystemVerilog simulator

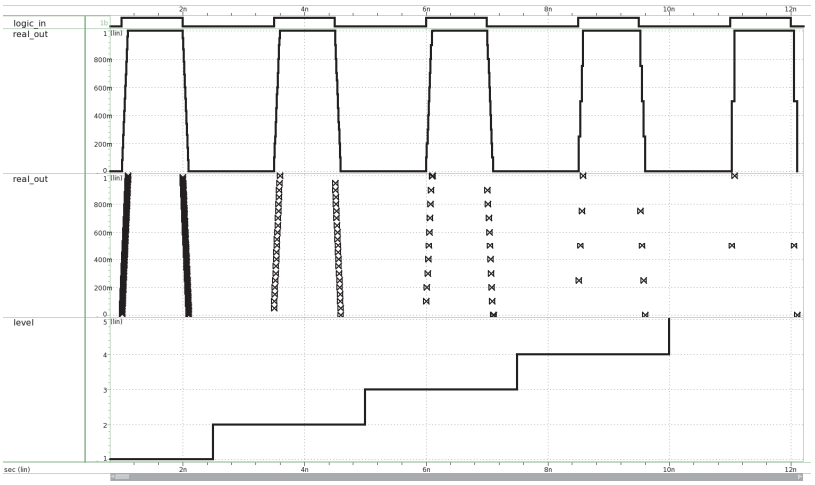

Fig. 3. The ADC "level" variable effect on the output

Also, in the real circuit, there is a PVT factor. The PVT factor is represented as a "res_scale" variable. During the verification, the "res_scale" variable should be randomized in the range of (-1, 1), where 0 provides the nominal resistance values, -1 – (nominal – 10%) and +1 – (nominal + 10%). The user can also exceed the range if there is a need.

The resistance ladder's analog model has two analog inputs – VDD, VSS and a sixteen real bus outputs. Each of the outputs then goes into an appropriate comparator and is compared against the input signal. The resistance ladder's analog outputs depend on internal resistor values and are calculated by using simple voltage divider equations as shown in Fig. 4.

```
assign rstep   = (res_scale > 0 ) ? 220   - res_scale * 22   : 220   - res_scale * 22    ;
assign rfoot   = (res_scale > 0 ) ? 12600 - res_scale * 1260 : 12600 - res_scale * 1260  ;
assign rhead   = (res_scale > 0 ) ? 2730  - res_scale * 273  : 2730  - res_scale * 273   ;

real vmax, vmin, vstep;
assign vmax  = VSS + ( 128 * rstep + rfoot)  * (VDD - VSS)  / (rhead + 128 * rstep + rfoot);
assign vmin  = VSS + ( rfoot * (VDD - VSS) ) / (rhead + 128 * rstep + rfoot);
assign vstep = ( vmax - vmin ) / 128 ;

genvar i;

generate
for (i = 0 ; i < 128 ; i = i + 1 ) begin
  assign n[i] = (i + 1) * vstep + vmin ;
end
endgenerate
```

Fig. 4. The resistance ladder module

The analog comparator RNM submodule compares 2 analog signals and outputs a digital result. Besides, in order to simulate a real circuit behavior, the comparator has additional variables responsible for offset and hysteresis effects. They can be set from the top cells by cross-module reference.

Offset and hysteresis effects are important in real comparators and may affect the output significantly, especially if the comparators are used for sensitive applications like duty cycle correction or delay calibration. At the same time, the offset is usually hard to predict as it changes not only from circuit to circuit but also from corner to corner. Hence it is a good thing to have a settable offset inside the RNM comparator model. An example of offset and hysteresis effects in the model is shown in Fig. 5.

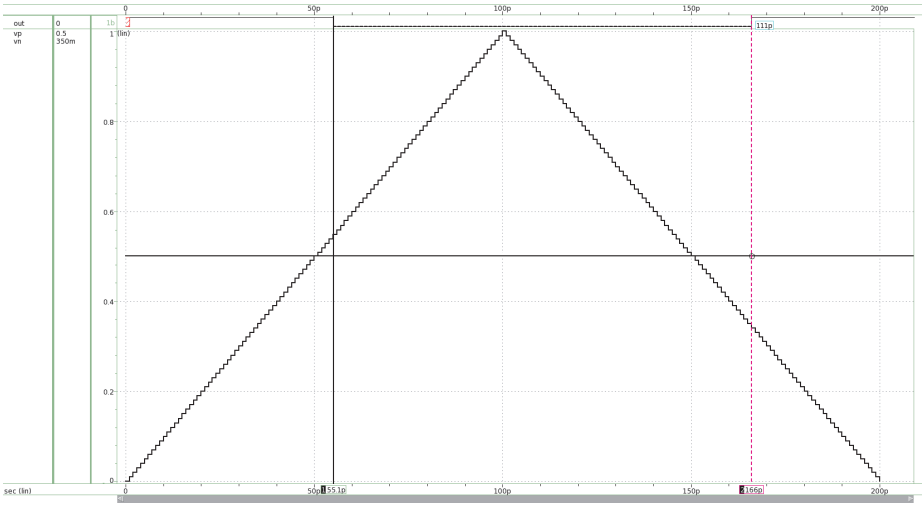

Fig. 5. The RNM comparator offset and hysteresis

There is also a “fat-tree” logic thermometer to the binary encoder which converts the thermal codes (outputs of the sixteen comparators) into a binary output. The cell is fully digital; however, it also contains analog delays which are PVT-dependent. The delay dependency is linear and is controlled by the “delay_scale” variable. During the verification, the “delay_scale” variable should be randomized in the range of (-1, 1), where 0 provides the nominal delay values, -1 – (nominal – 10%) and +1 – (nominal + 10%). The user can also exceed the range if there is a need. The current delays were taken from real standard cells with the14nm technology.

There were several RNM milestones which this project was meant to achieve during the model creation. The milestones are general and do not consider only the ADC model. Those are the following:

1. Have as many digital ports as possible.
2. Keep as much internal logic digital as possible.
3. Make the model PVT-dependent.
4. Model hierarchy and elements (like resistances and nodes) should be similar to the Spice model.
5. Use real-type variables instead of parameters for model configuration.

Milestones №1 and №2 ensure minimal effort during model integration into the already existing digital environments. №3 increases functional verification coverage. №4 simplifies node-to-node equivalency checks and makes the overall verification methodology stronger. №5 makes it possible for the user to change the model configuration at any time during the simulation. Such approach allows to create interesting testcases with dynamic configuration for example checking jitter effects by applying noises on supply.

The ADC model has 3 inputs – “VDD”, “VSS”, “in”, and 1 output bus – “code”.

- “VDD”, “VSS” are the source nodes and are digital;
- “in” is an analog input signal which should be converted into an appropriate code;
- “code” is an output bus.

RNM ADC contains 3 different analog submodules. d2a converters (mentioned as bit-to-analog signal converters), a resistance ladder, and analog comparators.

According to the mentioned milestones the input source ports – VDD, VSS are digital. However, the resistance ladder expects analog VDD and VSS inputs. To convert the signals, there are two “d2a” converters.

The resistance ladder creates reference voltages which are later compared against the input signal via analog comparators. The output thermal code is then converted into a binary code by the “fat-tree” thermometer to binary encoder.

Also, there are several variables which should be configured from the top cells through a cross-module references. At the same time, the configuration variables are passed to the internal submodules.

"initial" block passes configuration variable values to the internal submodules.

The "VDD_value" variable is passed to the VDD converters and affects the VDD signal's high level. In general, it is recommended to randomize this signal too as the voltage is also part of the "PVT". The "VSS_value" variable is similar to the "VDD_value" except it is responsible for the VSS signal. "simulation_level" is passed to the d2a converters. The effects of this variables are described in appropriate paragraphs.

Model verification. To have a reliable verification, the RNM model must be compared with Spice model in exactly by same conditions. To execute such a comparison, a Co-simulation environment with a SystemVerilog top testbench was created. The testbench is common between Spice and RNM models and calls them in parallel.

The RTL testbench is also responsible for passing the RNM configuration variables to the RNM model. It calls the RNM model and Spice model with appropriate interfacing and passes the same inputs to them. If the interfacing and the configurations are done properly the outputs of two models should match in terms of functionality. The environment block scheme is presented. Fig. 6 shows an abstract scheme of Mixed-Signal verification environment.

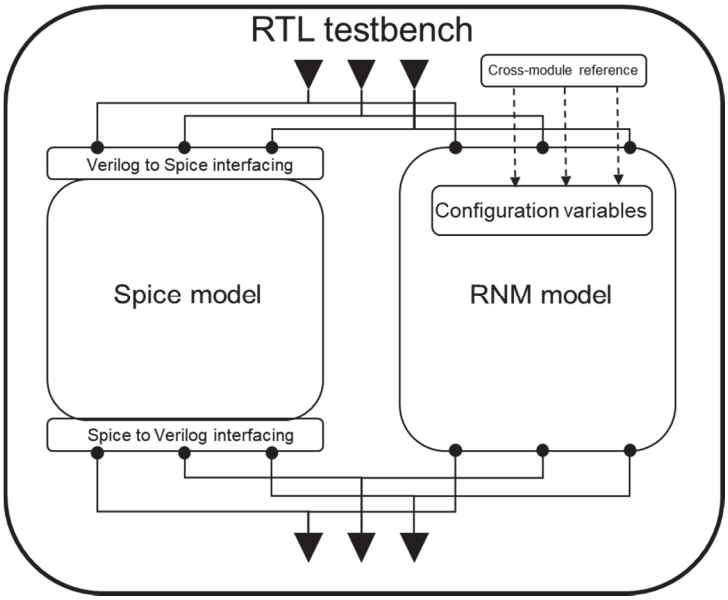

Fig. 6. DAC RNM model verification environment

The Spice model's scheme (Fig.7) includes a resistance ladder, comparators and a thermometer to binary encoder logic. All RNM resistors are matched with the Spice resistors.

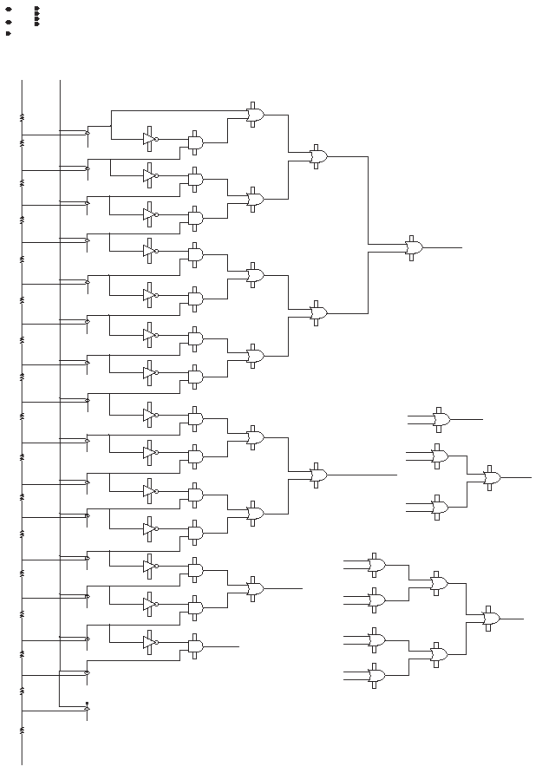

Fig. 7. The spice TG based DAC model

Simulation Results. Simulation checks all possible output code combinations, while the input is gradually changing from 0 to VDD.

The gradually rising ADC input "in" is common between the two models and the appropriate RNM and Spice code outputs (shown in Fig. 8) are compared one with the other. The resistance ladder output voltage difference between RNM and Spice at nominal conditions is less than 1 *mV*. The output codes' edge difference between RNM and Spice models is less than 10 *ps*.

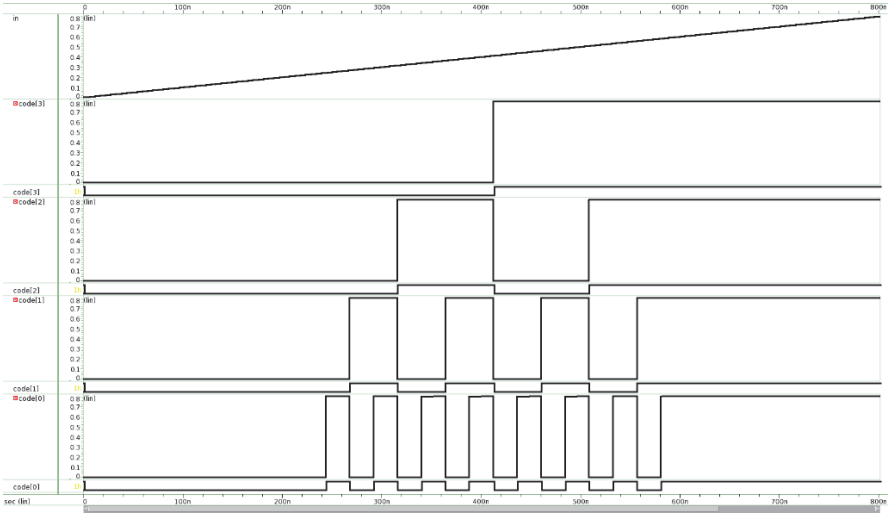

Fig. 8. The spice vs Verilog wave-to-wave comparison

Table

Simulation results

	Simulation duration in seconds	Resulting wave file (fsdb) size in megabytes
Spice model	616.93	395
RNM level 1	327.35	1480
RNM level 2	78.21	384.4
RNM level 3	50.27	234.5
RNM level 4	30.42	142.5
RNM level 5	25.96	114.8
RNM level 6	23.78	101.2

The table above presents the results of several Co-simulations. The first line shows the run time and the resulting wave file size of the Spice model. The rest of the lines show the RNM model usage with different simulation level parameters.

Conclusion. An RNM ADC was implemented and verified against a similar Spice model. Despite the introduced 7 *ps* across PVT mean error, the RNM ADC provides 2-300 times higher simulation speed (depending on the level) compared to the Spice. At the same time, the RNM model exists only in the SystemVerilog domain which greatly simplifies its integration into the already existing digital environments.

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National Polytechnic University of Armenia. The material is received on 03.15.2021.

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ԱՆԱԼՈԳԱԹՎԱՅԻՆ ԿԵՐՊԱՓՈԽԻՉԻ ԻՐԱԿԱՆ ԹՎԵՐՈՎ ՄՈԴԵԼԱՎՈՐՄԱՆ ԵՐԹՈՒՂՈՒ ՆԿԱՐԱԳՐՈՒԹՅՈՒՆԸ

Նկարագրված է անալոգաթվային կերպափոխիչի իրական թվերով մոդելավորման գործընթացը SystemVerilog միջավայրում: Անալոգային բջիջները, որոնք նկարագրված են լինում թվային միջավայրում, սովորաբար թեստավորման ընթացքում խնդիրներ են առաջացնում ոչ պատշաճ նկարագրված լինելու պատճառով: Թվային մոդելները ունակ չեն ցուցադրելու անալոգային ազդանշաններ. հետևաբար՝ դրանք ի վիճակի չեն ունենալու ստուգման լայն ծածկույթ: Իրական թվերով մոդելավորմամբ առաջարկվում է լուծում, որը զգալիորեն մեծացնում է անալոգային ստուգման ծածկույթը և թույլ է տալիս ունենալ ավելի կարճ նմանարկման ժամանակ՝ համեմատած գոյություն ունեցող այլընտրանքներին, որոնցից է, օրինակ՝ համանմանարկումը: Իրական թվերով մոդելավորված կերպափոխիչի նմանարկումը ընթանում է 2 կամ ավելի անգամ արագ՝ համարժեք Spice մոդելավորման համեմատ:

Առանցքային բառեր. անալոգաթվային կերպափոխիչ, SystemVerilog, իրական թվերով մոդելավորում, համանմանարկում:

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МАРШРУТ МОДЕЛИРОВАНИЯ АНАЛОГО-ЦИФРОВОГО ПРЕОБРАЗОВАТЕЛЯ НА ДЕЙСТВИТЕЛЬНЫХ ЧИСЛАХ

Представлен маршрут моделирования аналого-цифрового преобразователя на действительных цифрах в среде SystemVerilog. Аналоговые цепи, которые описываются в цифровой среде, обычно приводят к проблемам во время тестирований, поскольку не описываются должным образом. Цифровые модели не способны описывать аналоговые сигналы, следовательно, они не способны иметь высокий охват проверки. Моделирование на действительных числах предлагает решение, которое значительно увеличивает охват аналогового тестирования и сохраняет время моделирования ниже, чем существующие альтернативы, такие как совместное моделирование. Моделирование на действительных числах работает в два или более раз быстрее, чем эквивалентное моделирование Spice.

Ключевые слова: аналогово-цифровой преобразователь, SystemVerilog, моделирование на действительных числах, совместное моделирование.