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UDC 621.382 **MICROELECTRONICS**

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A HIGH SPEED SERIAL - TO - PARALLEL CONVERTOR WITH OUTPUT WORD LENGTH CONTROL

Serial data transmission in high-speed transceivers is widely used to minimize the number of input/output pins of integrated circuits. In modern serializer-deserializer (SerDes) applications different types of data encoding mechanisms are used.

A serial – to - parallel converter with controll data packet length is presented in this paper. This converter is applicable in solutions where data can be transferred with or without encoding. HSPICE verification in 4.5 sigma Monte Carlo range have confirmed the usability of the proposed solution in modern SerDes systems.

Keywords: SERDES, transmitter, receiver, serial - to - parallel conversion.

Introduction. CMOS technology is developing at high speed. With improvement of modern Integral circuits various problems appear during the design process. The operating frequency and power consumption are the main concerns for nowadays ICs. The usage of high speed SERDES systems are very common now. With advancement this SERDES systems are getting more complicated and functional. The main building blocks of these systems as its name suggests are the serializer and the deserializer.

To have a robust link between the transmitter and the receiver, the careful design of these blocks is mandatory. Input parallel data is serialized with the serializer block. To have good transmission without reflections TX/RX termination calibration process should be performed [1]. The final stage is deserilization which is performed via the deserializer block. In this paper, the deserilizer circuit is presented which has a function to change the output word length. This feature is very handy in protocols where both raw data transmission and transmission after encoding is available. If the SERDES system is source synchronous it can transmit raw data but if the clock is transmitted with data, encoding usage is preferable. That brings to the main idea of this paper. The system must have functionality to work properly in both scenarios.

Available architectures. Various structures have been used to design deserializer circuits. More commonly used architectures are based on shift registers and the tree structure. One of the benefits of using a shift register architecture is the small number of the required circuitry. The main used component is D flip-flop. In Fig. 1, a 1:4 deserializer with a shift register architecture is presented [2]. In this

architecture, the clock is not divided, and the same clock signal is used for all flip-flops.

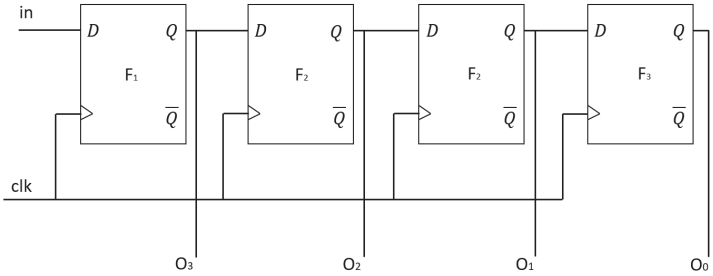

Fig. 1. A deserializer with a shift register architecture

Downside of this architecture is the usage of a high frequency clock. Power consumption is higher compared with the architecture when a divided clock is used. Also, with increasing the frequency the design of flip-flops with the required setup and hold time margins become challenging. It is also not convenient when the output word length is 8 or more. Parallel data will be available after 4 clock cycles for 1 to 4 deserializers. With bigger output word length, the waiting time rises correspondingly.

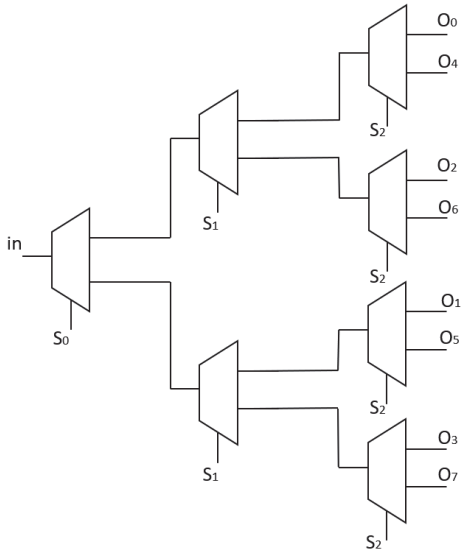

Fig. 2. A deserializer with a tree architecture

The tree structure is designed using several 1:2 demultiplexers. In Fig.2, a 1:8 deserializer with a tree structure is presented [3]. For selecting signal generation, a frequency divider must be used. Three frequency dividers are required for this case.

Problem description. Modern SERDES systems work with protocols where both raw data transmission and transmission after encoding is available. In Fig. 3, SERDES system components with an option to transmit encoded data are presented.

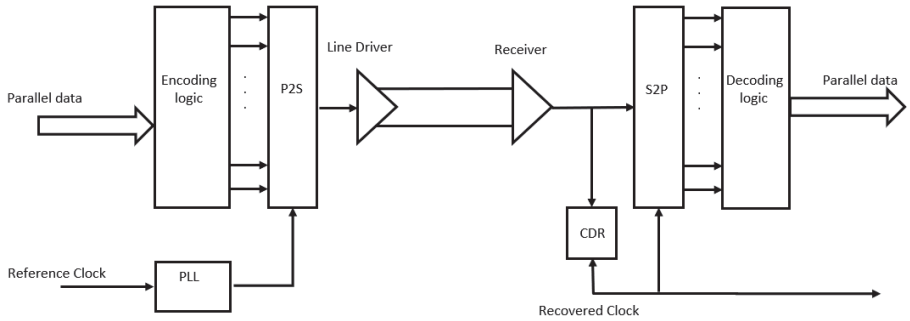

Fig. 3. A SERDES system with encoding

Different encoding algorithms can be used. In systems with Clock and Data Recovery 8b10b, encoding is very convenient. It provides enough state changes to allow reasonable clock recovery. Encoding for these systems is optional, so the parallel data length could vary, depending on application. A serial-to-parallel converter should have an option to work with both cases.

The method explanation. To have a serial-to-parallel converter with an option to change the output word length, a divider should be designed with a variable division ratio. In Fig. 4, the block diagram of the proposed divider is presented.

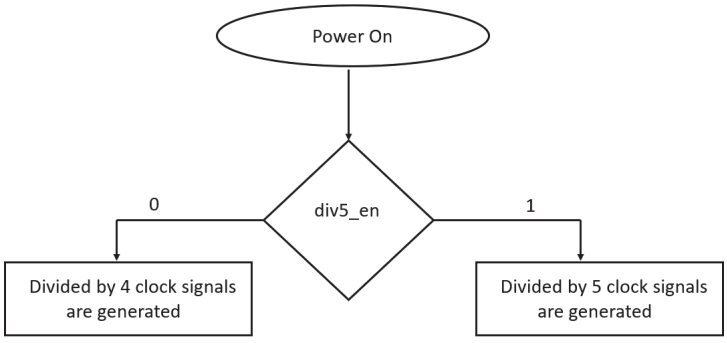

Fig. 4. The block diagram of the divider

There are special constraints on the frequency divider for this architecture. It should be able to generate a divided by 4 clock signals with a 90° phase shift. It should also have a function to divide by 5 when bigger word length mode is activated. A divider circuit is constructed using D latches, D flip-flops, NAND logic cells. In Fig. 5, D flip-flop is presented which is constructed using D latches.

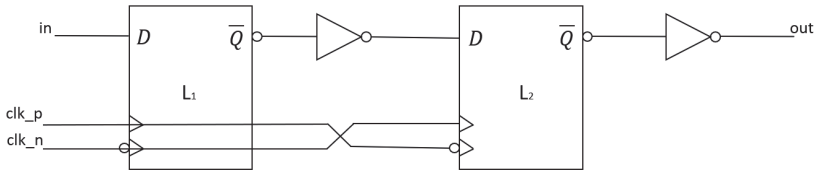

Fig. 5. A D Flip-Flop

A divider can operate in 2 modes - divided by 4 and divided by 5. When div5_en signal is 0 divider, it is divided by 4 modes. It generates divided by 4 clock signals with 25% duty cycle. These signals are shifted by 90 degree. clk_div signal is divided a clock signal for the output stage flip flops with 50% duty cycle. When div5_en signal is logic 1, sig<4:0> signals are generated for latches and divided by a 5 clock signal for the output flip flops. The structural block diagram of the divider is presented in Fig. 6.

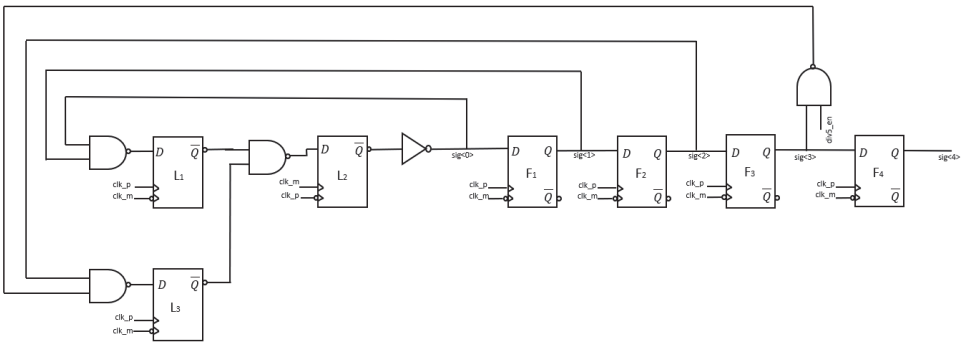

Fig. 6. The structural block diagram of the divider

The divided and shifted sig<4:0> signals are available on the output of latches as presented in Fig. 7.

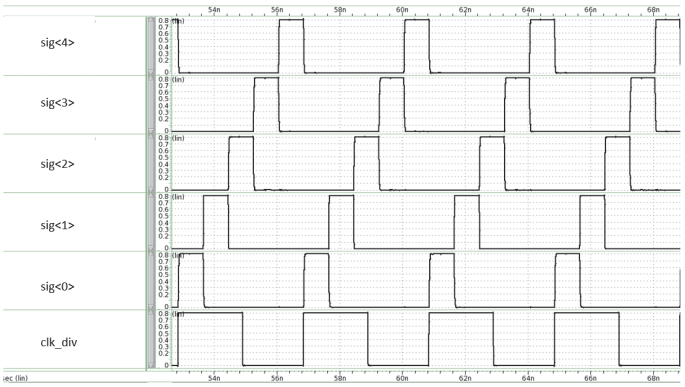

Fig. 7. The divided by 5 signals

The clk_div signal is generated using SR latch. If the corresponding sig<4:0> signals are used for set and reset operations, the frequency divided by 4 or 5 with a 50% duty cycle can be obtained. In this simulation 1.25 *Ghz* clock is used. One of the difficulties during the design of a divider is the clock skew. With variation of the process, voltage and temperature skew between the clk_p and clk_m signals can vary and cause a divided clock duty cycle distortion. To bypass this problem, one solution is the design of latches and flip-flops with big setup and hold margins.

When div5_en=0, sig<4> is pulled up to 0.8*V*. In Fig. 8, the division to 4 case is presented.

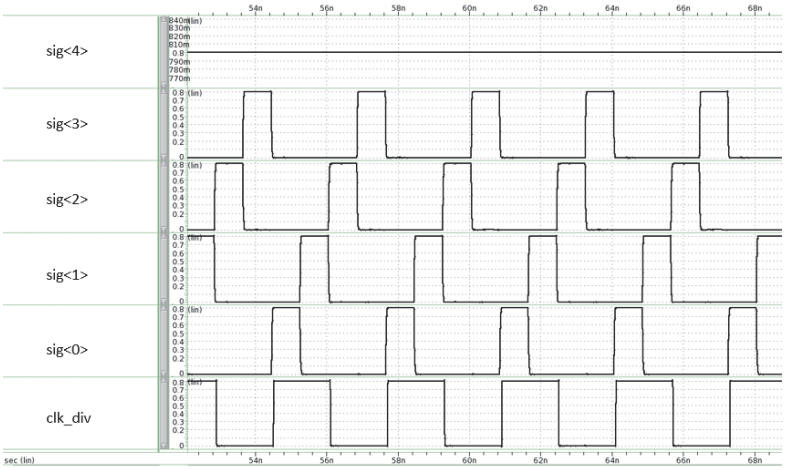

Fig. 8. Divided by 4 signals

Simulation Results. In Fig 9, a 1:4 deserializer is presented, which has a capability to change output word length from 4 to 5. A deserilizer is constructed with latches and flip-flops. With sig<4:0> signals, serial data is latched and with the rising edge of div_clk ,it is latched to output.

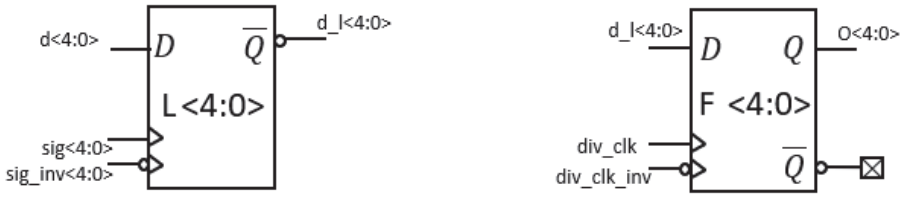

Fig. 9. A 1:4 deserializer

The timing of clock signals is crucial. It must be ensured that the rising edge of clk_div signal will occur after the serial data have been latched. Otherwise it can result in data errors. For the sig<4:0>, signal generation frequency divider is used.

Below are presented the HSPICE [4] simulation results of serial - to - parallel converter designed by SAED14*nm* FinFet technology [5].

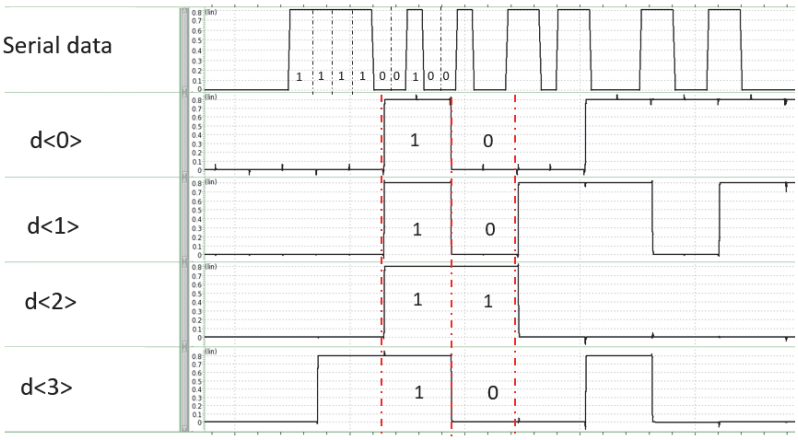

Fig. 10. Serial-to-parallel input and output plots

The top plot of Fig. 10 is the input serial data. After a 1 clock cycle, deserilized data is available. To be sure that the designed circuit is operating without data errors, Monte Carlo simulation was also performed. In Fig. 11, the plot showing the data error spread considering 4.5 sigma variation and 0.95 confidence interval is presented.

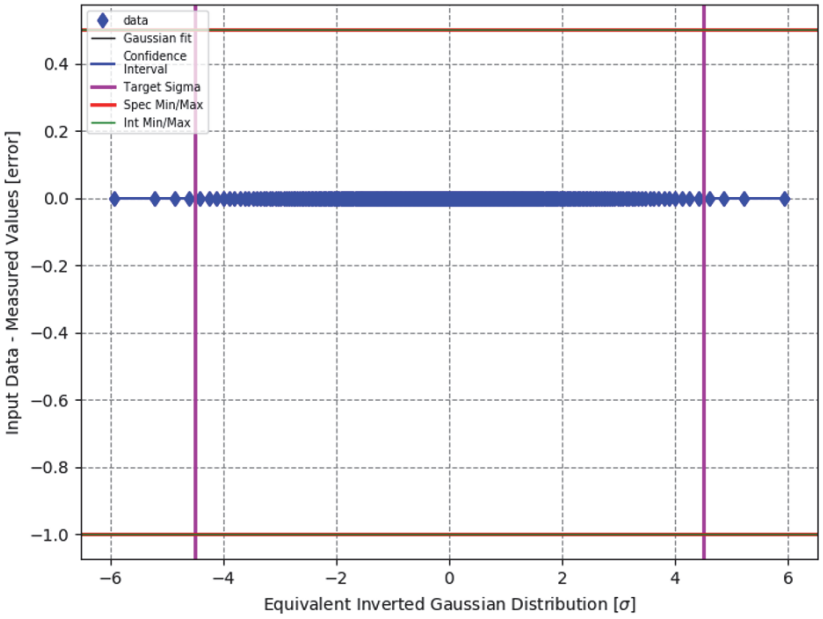

Fig. 11. Monte Carlo simulation results

In the table below, information about area and power consumption is presented. The results are for typical PVT conditions.

Table

Power consumption and area

Block	Power consumption	Area
Deserializer	220uA	50.7um^2
Divider	65uA(div 5 mode)	42.4um^2

Conclusion. A serial-to-parallel converter with a variable output word length is designed. It can be used in modern SERDES systems. For simulations, SAED 14nm FinFet technology is used. The block is functional up to 2.5Ghz frequency. For higher frequencies, division and data errors occur. Several of these devices can be used to obtain 8bit, 10bit or a bigger output word length.

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National Polytechnical Univercity of Armenia. The material is received on 23.10.2020.

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ԲԱՐՁՐ ԱՐԱԳԱԳՈՐԾՈՒԹՅԱՄԲ ՀԱՋՈՐԴԱԿԱՆ-ԶՈՒԳԱՀԵՌ ԿԵՐՊԱՓՈԽԻՉ՝ ԵԼՔԻ ԱԶԴԱՆՇԱՆԻ ԵՐԿԱՐՈՒԹՅԱՆ ԿԱՌԱՎԱՐՄԱՄԲ

Տվյալի հաջորդական փոխանցումն արագագործ ընդունիչ-հաղորդիչ հանգույցներում լայնորեն կիրառվում է ինտեգրալ սխեմաներում՝ մուտք-ելք հանգույցների քանակը նվազեցնելու համար: Ներկայումս կիրառվում են տվյալի կոդավորման տարբեր մեխանիզմներ:

Աշխատանքում ներկայացված է հաջորդական-զուգահեռ փոխակերպիչ՝ տվյալի փաթեթի երկարության կառավարման հնարավորությամբ: Այս փոխակերպիչը կիրառելի է այնպիսի լուծումներում, որտեղ տվյալը կարող է փոխանցվել ինչպես կոդավորված, այնպես էլ առանց կոդավորման: Մոնտե Կառլո նմանակումները՝ HSPICE ծրագրային գործիքի միջոցով, հաստատում են առաջարկվող լուծման կիրառելիությունը ժամանակակից հաջորդական կապով համակարգերում:

Առանցքային բառեր. SERDES, հաղորդիչ հանգույց, ընդունիչ հանգույց, հաջորդական զուգահեռ փոխակերպում:

А.Т. ГРИГОРЯН, М.Т. ГРИГОРЯН, В.Д. ОГАННИСЯН

ВЫСОКОЧАСТОТНЫЙ ПОСЛЕДОВАТЕЛЬНО-ПАРАЛЛЕЛЬНЫЙ КОНВЕРТЕР С КОНТРОЛЕМ ДЛИНЫ ВЫХОДНОГО СИГНАЛА

Последовательная передача данных в узлах высокочастотных приемопередатчиков широко используется для уменьшения количества узлов ввода-вывода в интегральных схемах. В современных приложениях сериализатора-десериализатора применяются различные типы механизмов кодирования данных.

В работе представлена возможность управления длиной пакета данных при его параллельном преобразовании. Этот преобразователъ применяется в решениях, где данные могут передаваться и с кодировкой, и без кодировки. Моделирование методом Монте-Карло с использованием программного инструмента HSPICE подтверждает применимость предложенного решения в современных системах последовательного соединения.

Ключевые слова: SEDRES, узел передатчика, узел приемника, последовательно-параллельное преобразование.