ISSN 0002-306X. Proc. of the RA NAS and NPUA Ser. of tech. sc. 2020. V. LXXIII, №2

UDC 004.08:621.382.3 MICROELECTRONICS

V.SH. MELIKYAN, E.R. KAGRAMANYAN, H.A. BABAJANYAN, K.O. PETROSYAN

A FREQUENCY-TO-VOLTAGE CONVERTER WITH A REDUCED DELAY TIME RANGE OF THE OUTPUT SIGNAL

A new method for optimizing the frequency-to-voltage converter (FVC) circuit is presented. In some FVC designs the delay time range of the output signal is very big in case of high input frequencies. By the new method of optimization, the output signal of FVC gets its stability during a short delay time in case of any frequency of the input signal. Using this method, the design obtains a higher area by 81%. The optimized FVC is preferable to be used in voltage-controlled oscillator (VCO), phase-locked loop (PLL) and small electronic projects. In the optimized FVC and the primary circuit designed in the 32 nanometer technology in case of the 0.02 *GHz* input frequency, the delay time range is 700 *ns*. In case of 0.2 *GHz* frequency, the delay time range in the primary circuit is 1700 *ns* and in the optimized FVC- 700 *ns*.

Keywords: transistor pump frequency discriminator, staircase generator, Schmitt trigger, invertor, circuit for the first period (CFFP).

Introduction. The new design of FVC is based on the transistor pump frequency discriminator (Fig.1) [1]

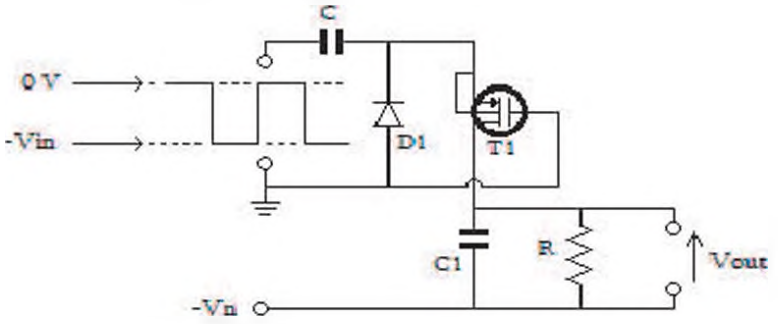

Fig.1. Transistor pump frequency discriminator

The output signal of the transistor pump frequency discriminator is formed by the C1 capacitor and R resistor. In the half-periods when the T1 transistor is opened, the C1 capacitor charges from the C capacitor. During the period, the C1 capacitor loses some charge. The stability of the output signal forms when during the period, the C1 capacitor charges and discharges by the same charge (Fig.2). So,

the output signal starts from the minimal voltage and increases to a value appropriate to the input frequency.

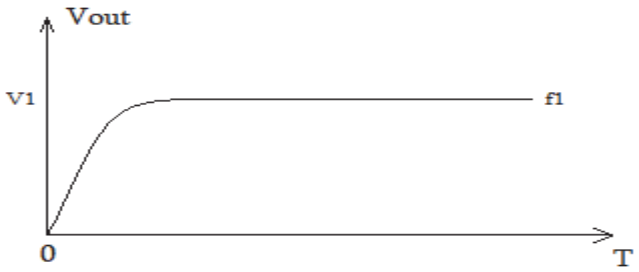

Fig.2. The output characteristics of the transistor pump frequency discriminator

The purpose of the optimization method is to make the output signal more stable whose value, during the first period of the input signal, will get close to a value of appropriate frequency. By this, the delay time range will be short.

In the newly designed FVC, a staircase generator is also used (Fig.3) [1].

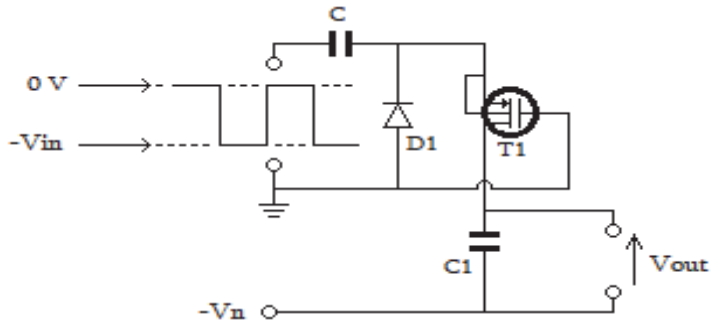

Fig.3. A transistor pump staircase generator

FVC is very important in the circuits with feedback connection (like VCO, or PLL) and it is preferable to have accurate input and output signals for it. If the output voltage of FVC starts at 0 and obtains its accurate value much later, it can disturb the right working process of all the circuit in which the FVC is to be used. If the output voltage starts at the right value after the first half-period, the work of the circuit will be secured.

There are several methods of creating accurate FVC, for example:

- using a differentiator and an RMS-DC converter [2],
- using a charging/discharging switch [3],
- using a current-controlled oscillator (ICO) [4],
- using an R-C network, an amplifier, a rectifier and a filter [5].

By the new method of optimization, the output characteristics of the FVC are very accurate.

A method for improving the output characteristics of FVC. The circuit that is used for optimization is working with non-negative supply voltages (Fig.4). The only difference of Fig.4 and Fig.1 circuits is that all negative voltages are turned to 0, and 0s to positive voltages, but the method of working is the same in both circuits.

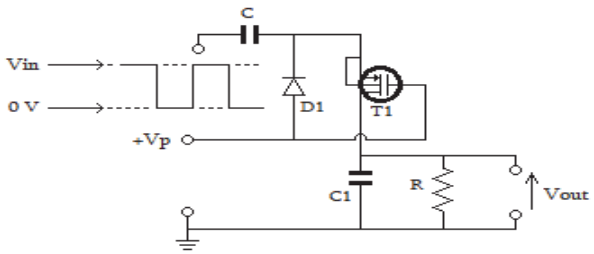

Fig.4. The transistor pump frequency discriminator (with positive voltages)

Let's assume that the input voltage is changing from 0 to Vdd. In this case, the formula of the accurate Vout will be (1):

$$Vout = C*R*f*(Vdd - Vd1 - Vth). \quad (1)$$

As, at the beginning of the input signal Vout=0, we get the constant value of the output voltage by some delay time range (ΔT). The output characteristics of the circuit are shown in Fig.5.

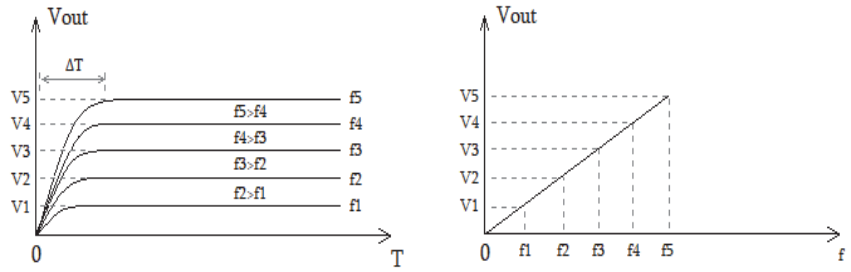

Fig.5. The output characteristics of the transistor pump frequency discriminator in case of different input signals

The higher is the frequency, the more time is spent to obtain the constant value of the output voltage. So, we use some other circuits to solve this problem. The essence of the method is to provide the output with a voltage near to the appropriate value in the first period, during which, the output voltage will be formed with the help of other circuits and after the second period, it will keep its

value only by FVC. A circuit should be added by which the output voltage will be low in a long period and will be high in a short period. The option of the method is to have high Vout in the first half-period, and in the second half-period, it starts to discharge. As the period time is long, the Vout will go to a low voltage.

So, the lower is the input frequency, the lower is Vout in the first period and is near to the right output value of the appropriate frequency. By that, the delay time range (ΔT) will be short for any frequency. For that, we use a circuit which will repeat only the first period of the input signal and then, it will keep a constant value. The circuit consists of a staircase generator, Schmitt trigger and inverters (Fig.6).

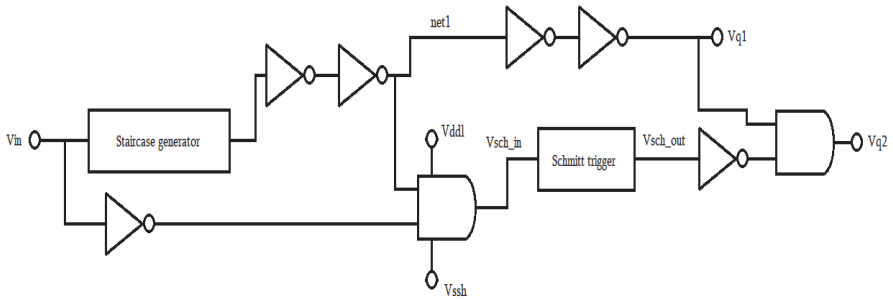

Fig.6. A circuit for the first period of the input signal (CFFP)

The staircase generator is designed in the way in which its output will get to Vdd during the first period. If the first period starts with a low half-period, in the high half-period it will immediately increase to Vdd. If the first period starts with a high half-period than in the low half-period it will be 0 and, at the beginning of the second period, when the input gets to Vdd, the output will also increase to Vdd immediately. Two invertors are connected to the output of the staircase generator to have a more accurate signal. AND cell connected to the input of the Schmitt trigger uses Vddl and Vssh supply voltages. Vddl is chosen less than Vdd and Vssl is higher than Vss to have more accurate Vsch_out. Two inverters after net1 are used to equalize the delays for two input signals of AND of the Vq2 output. All signals are shown in Fig.7 for two variants of the input signal.

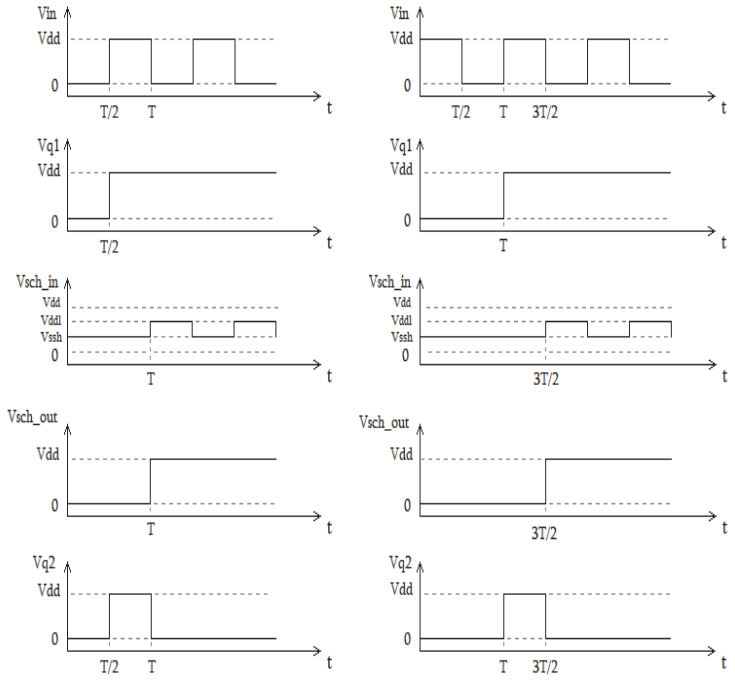

Fig.7. Signals of CFFP

In Fig.8, we see the circuit of the optimized FVC. It consists of CFFP, a transistor pump frequency discriminator, T2 and T3 transistors. The sizes of the T2 and T3 transistors are chosen so, that the R resistor should get much more resistance than the T2 and T3 transistors in the triode region. T3 is n-type and its base is connected with Vq2, T2 is p-type and its base is connected with Vq1. In the first half-period, when Vq1 and Vq2 are 0, T2 is in the triode region and T3 is cut-off and as the R resistor has much more resistance than T2 when it is opened, then Vout will be close to Vdd. In the second half-period, when Vq1 and Vq2 are Vdd, T2 will be in cut-off and T3 in the triode region, and Vout will start to decrease. The higher is the input frequency, the shorter is the half-period and the sooner will decreasing be over stopping at a high voltage. In the second period, Vq1 will be Vdd and Vq2 will be 0, and both transistors will be in the cut-off region, so Vout will depend only on the work of the transistor pump frequency discriminator.

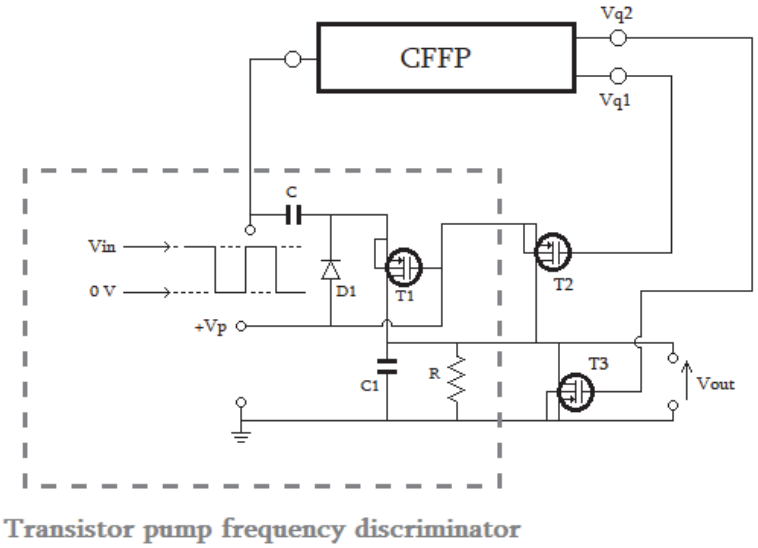

Fig.8. An optimized FVC

As at the end of the first period, Vout will be close to the expected value, the transistor pump frequency discriminator will change it to a little lower or a little higher value. The output characteristics of an optimized FVC are shown in Fig.9.

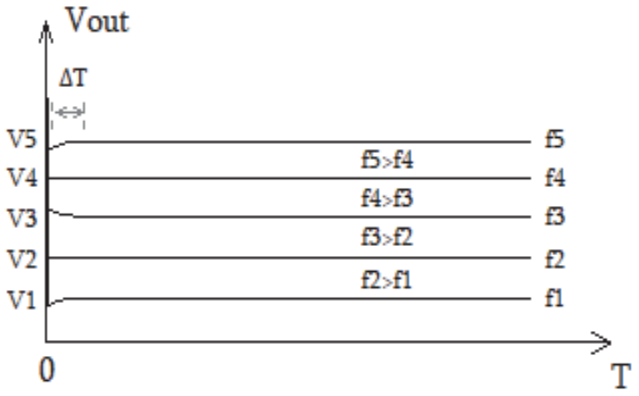

Fig.9. The output characteristics of the full FVC

Simulation results. Here are presented the circuits and simulation results for the 32 *nm* technology. The transistor pump frequency discriminator designed in the 32 *nm* technology is shown in Fig.10.

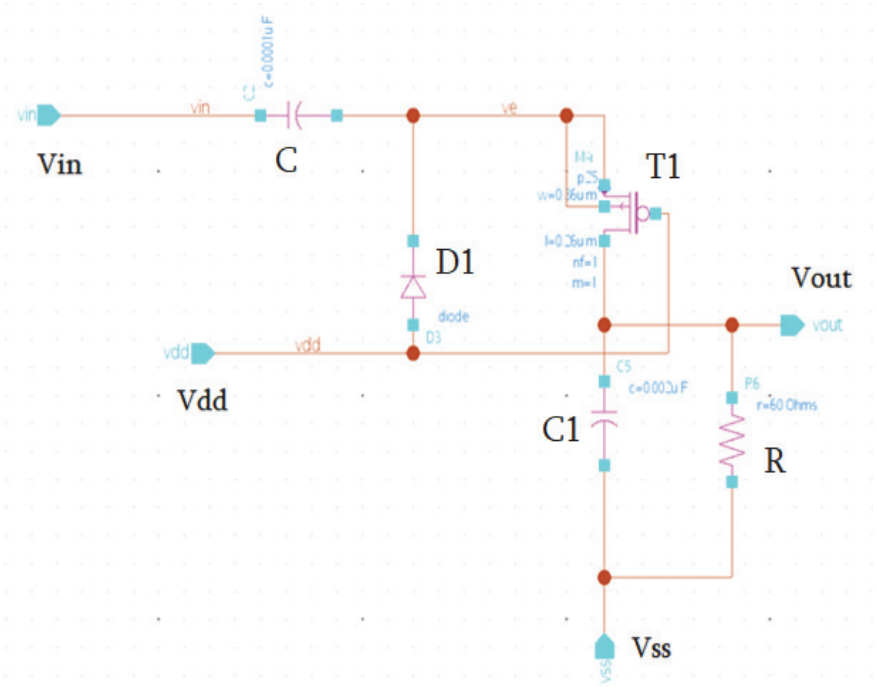

Fig.10. The transistor pump frequency discriminator

The staircase generator designed in the 32 *nm* technology is shown in Fig.11.

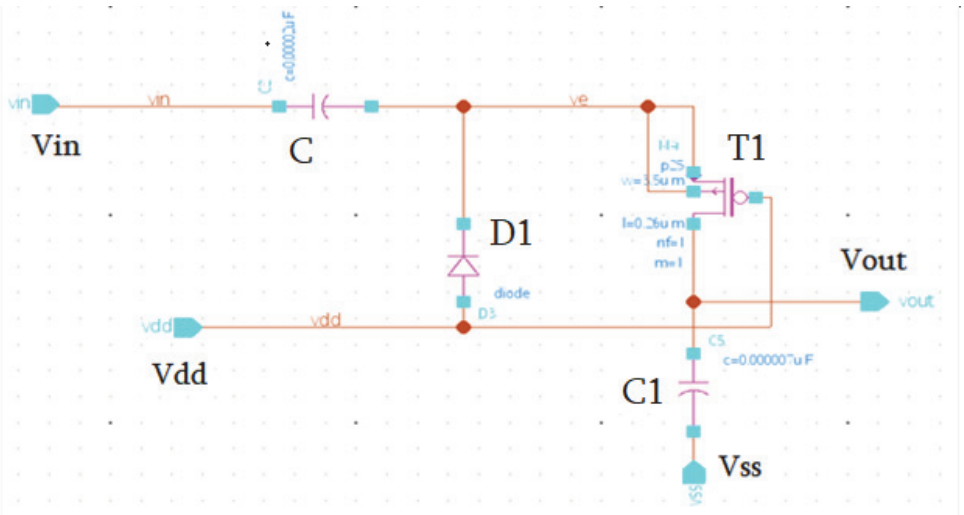

Fig.11. The staircase generator

The CFFP circuit designed in the 32 *nm* technology is shown in Fig.12.

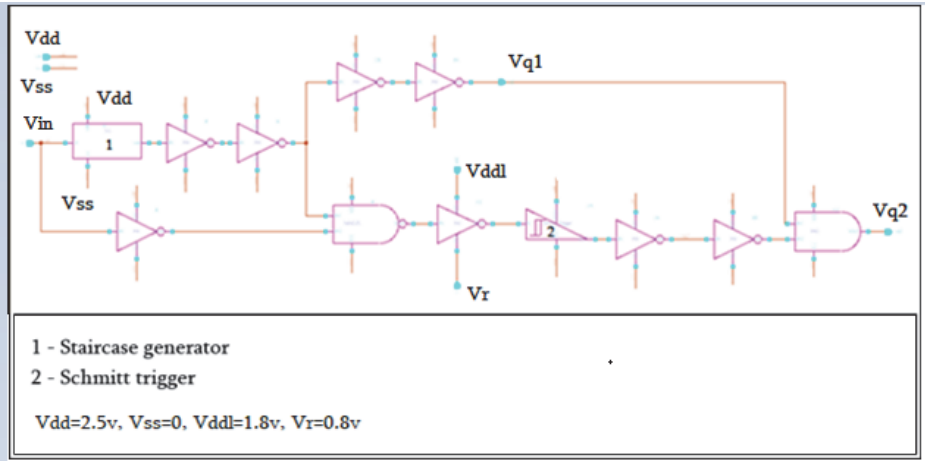

Fig.12. CFFP (Circuit for first period)

An optimized FVC designed in the 32 *nm* technology is shown in Fig.13.

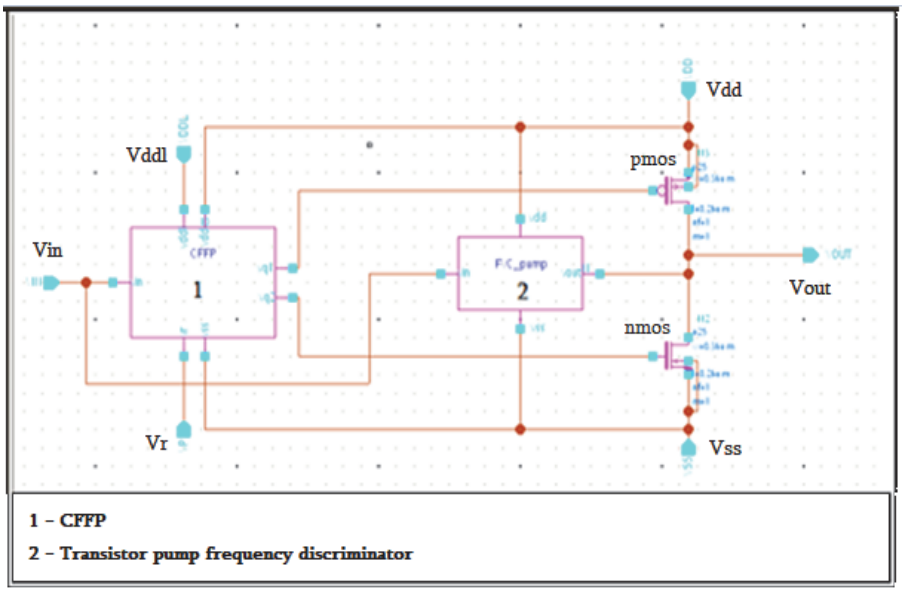

Fig.13. An optimized FVC

The frequency range is from 0.02 *GHz* to 0.2 *GHz* with a 0.02 *GHz* step. The supply voltage and the input signal amplitude are 2.5 *v*.

All characteristics are created by the HSPICE simulator. The output characteristics of the transistor pump frequency discriminator designed in the 32 *nm* technology are shown in Fig.14.

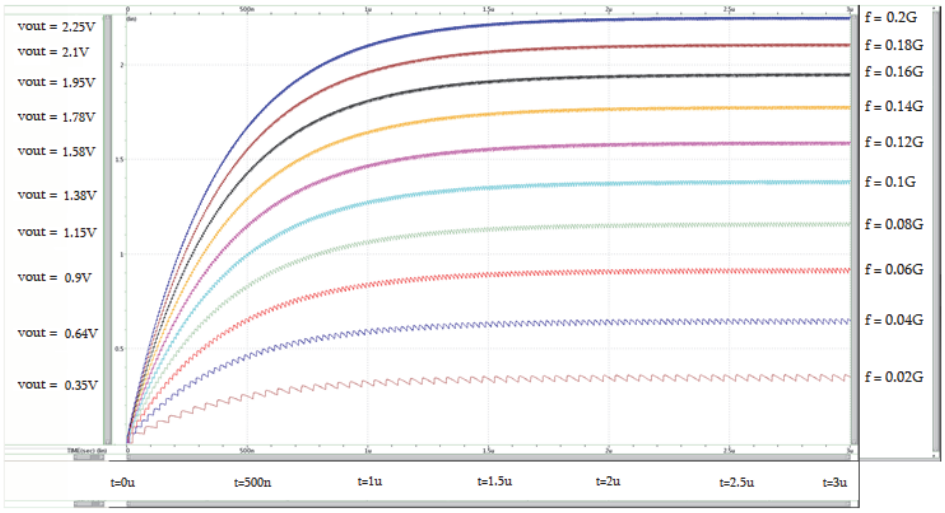

Fig.14. The output characteristics of the transistor pump frequency discriminator

The output characteristics of an optimized FVC designed in the 32 *nm* technology are shown in Fig.15.

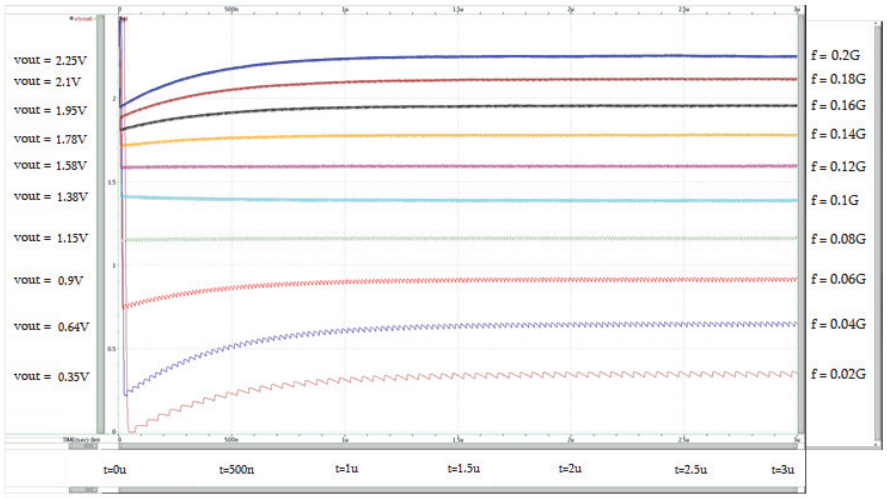

Fig.15. The output characteristics of an optimized FVC

The dependence of the output voltage on the input frequency of an optimized FVC is shown in Fig.16.

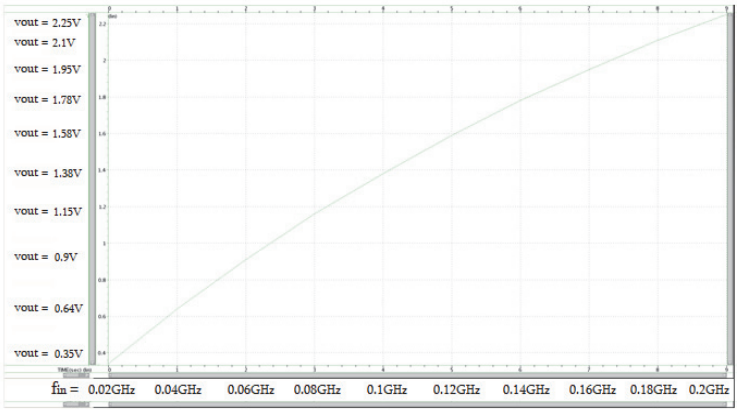

Fig.16. Linearity characteristics of an optimized FVC (dependence of output voltage on frequency). Frequency is changed from 0.02 GHz to 0.2 GHz with a 0.02GHz step

Fig.17 presents output characteristics in which the input frequency is becoming twice less at the end of every 2000 *n* time range. At the [0 - 2 *u*] range, the input frequency is 0.2 *GHz*, at [2 *u* - 4 *u*], it is 0.1 *GHz*, ([4 *u* – 6 *u*] - 0.05 *GHz*, [6 *u* - 8 *u*] - 0.025 *GHz*, [8 *u* – 10 *u*] – 0.0125 *GHz*). In the picture, we can see that the decreasing range of the output voltage also becomes nearly two times less during every 2 *u* time range.

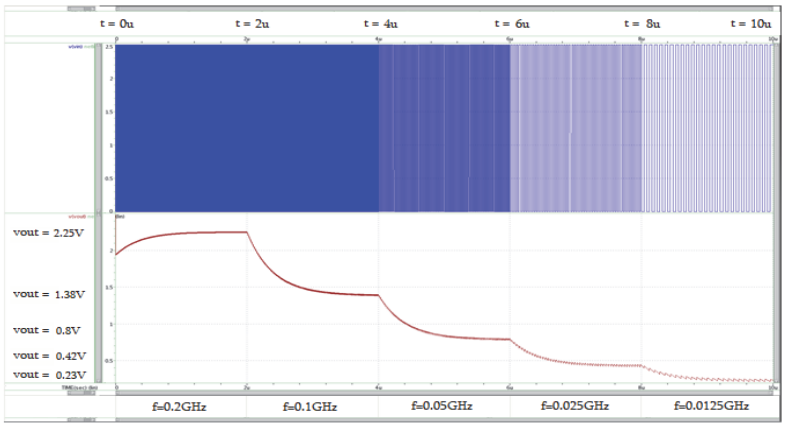

Fig.17. The output characteristics with different frequencies in different time ranges.

Conclusion. The main advantage of the full FVC is that it has not got a problem of delay time range. In the transistor pump frequency discriminator, the delay time range is as big as the frequency of the input signal. In a full FVC, the delay time range is very small for any frequency. In the transistor pump frequency discriminator designed in the 32 *nm* technology, in case of the 0.02 *GHz* frequency

of the input signal, the delay time range is 700 *ns*, and in case of 0.2 *GHz*- 1700 *ns*. In the optimized FVC, in case of the 0.02 *GHz* input frequency, the delay time range is 700 *ns*, and in case of 0.2 *GHz*, it is also 700 *ns*.

REFERENCES

1. **Hemingway T.K.** Electronic Designer's Handbook.- London, Business Books,.1970. – 296 p.
2. Simple and accurate frequency to voltage converter / **A. Lorsawatsiri, W. Kiranon, V. Silaruam, W. Sangpisit,** et al // IEEE publisher.- Chiang Mai, Thailand, 24 June, 2010. -P.1-3.
3. **Bui H.T., Savaria Y.** High-Speed Differential Frequency-to-Voltage Converter. // IEEE-publisher. Montreal. Canada. July. 2005. -P.1-3.
4. **Bui H.T., Savaria Y.** Design of a High-Speed Differential Frequency-to-Voltage Converter and Its Application in a 5-GHz Frequency-Locked Loop //IEEE-publisher.- Montreal, Canada, April, 2008. -P.1-8.
5. **Singh M., Sahu P.P.** A Wideband Linear Sinusoidal Frequency to Voltage Converter With Fast Response Time //IEEE publisher.- Tezpur, Assam, December, 2013. -P.27-35.

National Polytechnical University of Armenia. The materials is received on 20.02.2020.

Վ.Շ. ՄԵԼԻՔՅԱՆ, Է.Ռ. ԿԱԳՐԱՄԱՆՅԱՆ, Հ.Ա. ԲԱԲԱՋԱՆՅԱՆ, Կ.Օ. ՊԵՏՐՈՍՅԱՆ

ԵԼՔԱՅԻՆ ԱԶԴԱՆՇԱՆԻ ԿԱՐՃ ՈՒՇԱՑՄԱՆ ՏԻՐՈՒՅԹՈՎ ՀԱՃԱԽՈՒԹՅՈՒՆ-ԼԱՐՈՒՄ-ՓՈԽԱԿԵՐՊԻՉ

Ներկայացված է հաճախություն-լարում-փոխակերպիչի (ՀԼՓ) օպտիմալացման նոր մեթոդ։ Որոշ ՀԼՓ սխեմաներում ելքային ազդանշանի ուշացումը շատ մեծ է մուտքային ազդանշանի մեծ հաճախության դեպքում։ Ըստ այս օպտիմալացման մեթոդի՝ ՀԼՓ-ի ելքային լարումը հասնում է իր ճշգրիտ արժեքին կարճ ժամանակային տիրույթում մուտքային ազդանշանի ցանկացած հաճախության դեպքում։ Այս մեթոդի օգտագործմամբ սխեմայի մակերեսը մեծանում է 81% -ով։ Օպտիմալացված ՀԼՓ-ն նախընտրելի է օգտագործել փուլահաճախականային հանգույցներում, լարումով ղեկավարվող գեներատորում և փոքր էլեկտրոնային նախագծերում։ 32- նանոմետրանոց տեխնոլոգիայում նախագծված օպտիմալացված ՀԼՓ – ի և հաճախականային դիսկրիմինատորի ելքային լարման ուշացման տիրույթը 0.02 *ԳՀց* մուտքային ազդանշանի հաճախության դեպքում 700 *նվ* է։ 0.2 *ԳՀց* – մուտքային ազդանշանի հաճախության դեպքում հաճախանային դիսկրիմինատորում ուշացման տիրույթը 1700 *նվ* է, իսկ օպտիմացված ՀԼՓ-ում ՝ 700 *նվ*։

Առանցքային բառեր. տրանզիստորային պոմպի հաճախականային դիսկրիմինատոր, աստիճանային գեներատոր, Շմիտի տրիգեր, շրջիչ, առաջին պարբերության սխեմա։

В.Ш. МЕЛИКЯН, Э.Р. КАГРАМАНЯН, А.А. БАБАДЖАНЯН, К.О. ПЕТРОСЯН

ПРЕОБРАЗОВАТЕЛЬ ЧАСТОТЫ В НАПРЯЖЕНИЕ С КОРОТКИМ ДИАПАЗОНОМ ВРЕМЕНИ ЗАДЕРЖКИ ВЫХОДНОГО СИГНАЛА

Представлен новый метод оптимизации схемы преобразователя частоты в напряжение (ПЧН). В некоторых конструкциях ПЧН диапазон времени задержки выходного сигнала очень большой в случае высоких входных частот. Согласно новому методу оптимизации, выходной сигнал ПЧН приобретает стабильность в течение короткого времени задержки при каждой частоте входного сигнала. При использовании этого метода площадь схемы повышается на 81%. Оптимизированный ПЧН предпочтительнее использовать в генераторе, управляемом напряжением, в фазовой автоподстройке частоты и в небольших электронных проектах. В оптимизированном ПЧН и в частотном дискриминаторе, проектированном в 32- нанометровой технологии, при частоте входного сигнала 0,02 *ГГц* диапазон времени задержки выходного сигнала составляет 700 *нс*. При частоте входного сигнала 0,2 *ГГц* диапазон времени задержки в частотном дискриминаторе составляет 1700 *нс*, а в оптимизированном ПЧН - 700 *нс*.

Ключевые слова: частотный дискриминатор транзисторной помпы, лестничный генератор, триггер Шмитта, инвертор, схема для первого периода.