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MICROELECTRONICS

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THE NOVEL RECEIVER ARCHITECTURE FOR HIGH-SPEED INPUT/OUTPUT CIRCUITS

A significant increase of data transfer in Input/output devices results in reducing the circuit reliability and significant degradation in performance. The existing solutions do not meet modern requirements and in some cases, they are not even functionally operable. So, there is a need to design a new architecture for reliable data transfer. A new architecture of the receiver is proposed. This architecture allows to receive data at data-rates of 6.4 *GB/s* and above and contains DFE with kick back cancelation. The receiver with the proposed architecture can be used in special propose input/output circuits such as the LPDDR5 protocol.

Keywords: receiver, sense amplifier, decision feedback equalizer (DFE).

Introduction. The speed of many systems increases year by year. One of such systems is the LPDDR protocol [1]. The high bit-rate LPDDR5 protocol has various supply voltages and different termination conditions (Fig 1). In high speed LPDDR5 systems, receiving data signal becomes more critical as the eye height of the input signal can be 60...200 mV with different common modes (75...200 mV). Receiving such amplitudes with 6.4 *Gpbs* data-rate is not possible with known solutions such as differential amplifiers in the input stage of RX. Differential amplifiers have big input pairs which causes a bandwidth limitation [2]. This limitation does not allow to receive a high speed data signal. Also, channel and PCB noises become critical for higher data-rates.



Fig. 1. The DDR driver and transmission line

In this frequency, the gain of differential amplifiers is less than 1 and it is not possible to receive a correct data signal. Besides deserialization in the RX part, it needs to meet the half-cycle timing requirement which is difficult with the known structure of the receiver [3].

Architecture and circuit design. In the paper, a new architecture of the receiver for high speed LPDDR systems is presented. Instead of a differential amplifier, the proposed architecture uses a sampler on the PAD.

The macro contains:

- Two negative edge sense amp samplers at PAD;
- Four channel DAC circuit for VREF generation;

• 1-tap DFE to select two level of VREF based on the previous sampled bi-t. The structure of the proposed Sampler is presented in Fig. 2.



Half-Rate Rx with 1-Tap DFE

Fig. 2. The proposed architecture

Data signal is sampled in PAD with a clock signal and in the output of the sampler data is already deserialized. So, jitter which is the most critical parameter in the receiver design in the proposed architecture is not critical. In sampler design, the important parameter is the sampler propagation delay and the setup/hold aperture. DAC needed to generate VREF signal for the sampler as in the LPDDR system data signal is single ended. DAC generates 4 independent VREF signals which are used for DFE [4].

1 Tap DFE is implemented in the proposed architecture. The 1 tap DFE function allows comparing the current input against one of two values for the VREF based on the previously received bit value. This is accomplished by having a programmable VrefDac generator. DFE logic will determine which VREF is selected by the sampler.

This architecture allows to have better performance out of the receiver, due to the DFE and the high-speed voltage mode sense amplifier (CVSA) (Fig. 3). The

sampler input stage is a PMOS differential pair. The data signal is applied to the positive input, and the reference voltage from VrefDac is applied to the negative input. The clock signal connected to PMOS is sampling the data signal on the negative edge [5]. In the first stage of latch, the analog signal is transferred to digital and applied to the second stage. In the outputs of the second stage, deserialization of the data signal is completed. As the sense amplifier samples the data signal with a clock, there can be a kick back due to coupling from the clock signal to the VREF signal, which is critical as reference voltage can change and cause functional failure. The kick back cancelation feature is added in the sampler architecture. The PMOS transistor is added with a gate connected to the VREF signal (the negative input of the sampler) and the source/drain is connected to the clock signal. In this case PMOS operates as a coupling capacitor. The PMOS transistor will cancel the coupling from the clock signal as it also has a coupling to VREF but with a negative phase. A huge kick back noise can be reduced to a couple of $2...5 \, mV$ which does not affect the sampler performance.



Fig.3. A High speed sense amplifier

The DFE equalizes and improves the jitter and the vertical eye width and has a feedback with slices. DAC includes a ladder with resistors [6]. The circuit contains CDM on the inputs for the ESD protection.

VrefDac generates 4 independent VREF signals, which are connected to the inputs of multiplexers (MUX) in each slice. The MUX is providing a reference voltage for samplers for receiving data. The MUX output VREF levels select the DFE logic. Based on the previously received bit value, the DFE logic selects the appropriate VREF.

Samplers operate with differential half rate clock DQS_T and DQS_C.

Fig.4 shows the DFE timing diagram. For 6400 *Mpbs* the data rate delay should not be more than 312 *ps* (one period of the data signal) for DFE timing loop

proper operation. DFE based on the previously received bit value selects the appropriate VREF.



Fig.4. A high speed sense amplifier

Simulations. Simulation has been performed using the 14 *nm* SAED FinFet process technology [7], including TT (typical- typical), FF (fast-fast) SS (slow slow) corners, with the supply voltage and temperature variations, with data-rate up to 6400 *Mbps*.

In Fig.5, the sampler propagation delay for 60mV input eye height with different common modes over PVT [8] is shown. The sampler delay remains almost the same when the common mode is changed from 75 mV to 200 mV. This is an important parameter for the DFE timing loop correct operation.



Fig.5. The sampler delay for 60mV input eye height signal with different common modes

The Receiver simulation was carried out with a 40 *Ohms* DRAM driver including the 50 *Ohms* transition line for TT/FF/SS/FS/SF corners, the temperature range is from -40° C to 125° C with supply voltage level variation. Input eye height is 75mV.

In Fig. 6, simulation results without kick back cancelation are shown. In this case, the VREF kick back peak to peak noise amplitude is 140 mV. This noise can lead to functional failures as the 2 outputs of the receiver (even and odd) signals can contain incorrect data.



Fig.6. The RX simulation results without kick-back cancelation

With this high noise propagation, the delay of samplers increases significantly which causes a DFE timing loop failure. DFE selects incorrect VREF for the input signals and gets wrong data.

Fig. 7 shows the simulation results for SS -40° C VDD=0.675 V with a kick back cancelation for 6400 *Mbps*. As it is shown, the kick back noise amplitude is 20 *mV* and it is stabilized. Even and odd output signals, which are deserialization outputs (half rate signals), are correct.



Fig.7. The RX simulation results with kick-back cancelation

In the Table below the simulation results for the aperture and the setup/hold for the sampler over PVT are shown. It is shown that the worst aperture is $4.12 \ ps$, which means that the invalid time between the data signal and the clock signal is $4.12 \ ps$.

Table

	Aperture (ps)	Setup (ps)	Hold (ps)
Max	4.12	-8.82	4.70
Min	0.31	-4.13	3.82

Simulation results

Conclusion. A new receiver architecture is designed for the LPDDR5 protocol. In the proposed architecture, a sampler on the PAD is used. The data signal deserialization is done on the PAD. It has a smaller area and less power constipation compared with other solutions. The setup/hold aperture is $4.12 \ ps$ which allows to receive a high-speed 6400 *Mbps* signal without any functional problems. The proposed kick back cancelation feature shows that the VREF noise improves significantly. The 140 *mV* peak to peak noise after cancelation becomes 20 *mV*. The main disadvantage of the proposed architecture is the complicated design and tough timing specification.

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ԸՆԴՈՒՆԻՉ ՀԱՆԳՈՒՅՑԻ ՆՈՐ ՃԱՐՏԱՐԱՊԵՏՈՒԹՈՒՆԸ ԱՐԱԳԱԳՈՐԾ ՄՈՒՏՔ/ԵԼՔ ՏԱՐՐԵՐՈՒՄ

Տվյալների փոխանցման զգալի արագացումը մոտք/ելք հանգույցներում առաջացրել է սխեմաների հուսալիության նվազում, քանի որ նվազում է արտադրողականությունը։ Առկա լուծումները չեն բավարարում արդի պահանջները, և որոշ դեպքերում նույնիսկ ֆունկցիոնալ չեն գործում։ Այդ պատձառով անհրաժեշտություն է առաջաացել մշակել նոր ձարտարապետություն՝ տվյալների հուսալի փոխանցման համար։ Հոդվածում ներկայացված է մուտք/ելք հանգույցներում օգտագործվող ընդունիչի նոր ձարտարապետություն, որը թույլ է տալիս ընդունել առավել հուսալի տվյալները՝ 6,4Գ*բիթ/վ* և ավելի հաձախությունների դեպքում և միացնել որոշումով հետադարձ կապը հավասարեցնող սարքը։

Առանցքային բառեր ընդունիչ, զգայուն օպերատիվ ուժեղարար, հետադարձ կապը հավասարեցնող սարք, հենակային լարման աղբյուր։

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НОВАЯ АРХИТЕКТУРА ПРИЕМНИКА ДЛЯ ВЫСОКОСКОРОСТНЫХ УЗЛОВ ВХОД/ВЫХОД

Значительное увеличение скорости передачи данных в устройствах входа/ выхода приводит к снижению надежности схемы и значительному понижению продуктивности. Существующие решения не соответствуют современным требованиям, а в некоторых случаях приводят к функциональным ошибкам. Учитывая эти факторы, разработка новой архитектуры для надежной передачи данных является актуальной задачей. В статье представлена новая архитектура приемника, используемая в специальных схемах входа/выхода, таких как новый протокол LPDDR5, что позволяет получать данные более надежно при скоростях передачи данных 6,4 *ГБит/с* и выше. Основной особенностью решения является включение эквалайзера с обратной связью по решению (ЭОСР).

Ключевые слова: приемник, чувствительный операционный усилитель, эквалайзер с обратной связью по решению (ЭОСР), источник опорного напряжения (ИОН).