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TIMING EVALUATION MODEL FOR D FLIP-FLOPS CONSIDERING RADIATION EFFECT

An analytical model for calculating the timing parameters of D flip-flop taking into account the radiation impact is proposed in this paper. The main idea of this work is to eliminate the limitations in the IC design process using logic level simulations. Analytical expressions for evaluating the timing parameters are derived using pre-simulation results and polynomial fitting methods. The experimental results prove the effectiveness of the proposed model. The comparison to the SPICE simulation shows that setup and hold time evaluation errors are within 7% and 5,6% correspondingly and the clock to output delay calculation difference is 3%, which proves that this model is efficient and can be used to simulate the timing dependencies of the radiation impact in logic level design without running time-consuming circuit-level simulations.

Keywords: radiation effect, setup/hold-time, clock to output delay, linear energy transfer (LET), soft error, analytical equations, complementary metal-oxide-semiconductor (CMOS).

Introduction. Electron-hole pairs generated due to the influence of radiation, result in soft errors and threshold voltage shifts of the transistors. Such effects change the timing parameters of logic gates used in the design of digital and mixed-signal integrated circuits (IC). Experimental results (Fig. 1) show the significance of the influence [1].

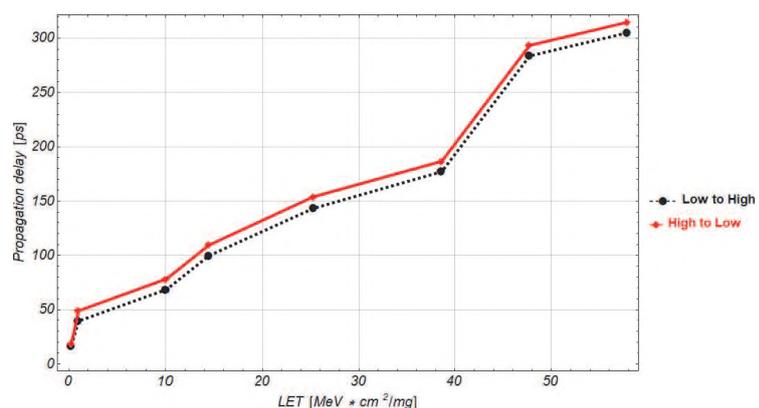


Fig. 1. Two input NAND gate propagation delay dependency on linear energy transfer (LET)

The timing analysis of ICs considering the radiation impact (RI) are crucial because of their usage in applications where high reliability is needed. Due to the complexity of modern ICs, the accuracy requirements to the tools performing timing analysis have been significantly increased. The most accurate simulation methods of soft errors are SPICE simulators (HSPICE, FINESIM, CUSTOMSIM) [2-4]. However, with the technology scaling and increase of the number of transistors in the design, the simulations become slower [5]. Therefore, new analytical models are required in higher abstraction levels to accelerate the design and verification process.

Many researches have been done for efficient estimation of the timing parameters [5-8]. In the mentioned works, analytical equations are derived based on solving differential formulas only for inverter gate. Whereas, similar methods are also required for timing analysis of the memory elements.

In memory elements, the RI leads to setup/hold-time degradation and can cause the cell to change state to another value. Despite that fact, RI on timing parameters of the circuits such as D flip-flops (DFF) is not considered in the existing analytical methods. Thus, accurate analytical methods consisting of analytical formulas for DFF setup/hold-time and clock to output delay calculations are required.

Radiation influence on setup/hold-time and clock to output delay.

Violations of the timing parameters of DFFs can cause unexpected behaviors including forcing DFF to enter metastable state. As an example, a DFF circuit (Fig.2) was designed in the Custom Compiler environment considering RI using SAED32nm technology [9].

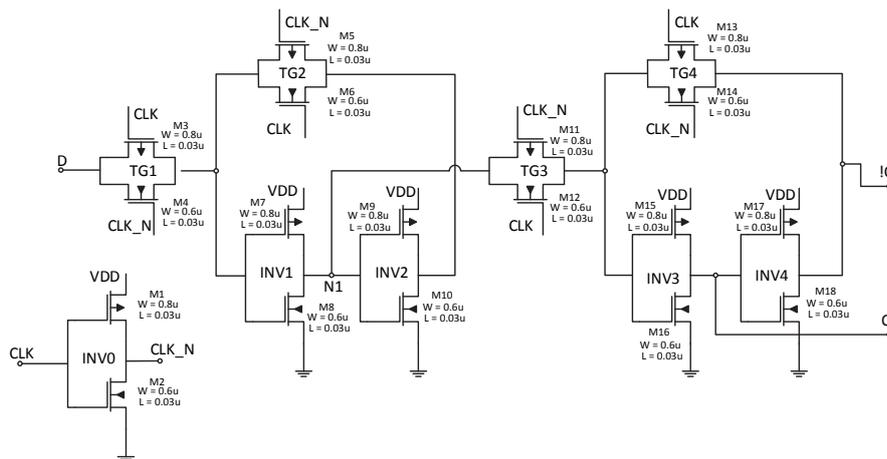


Fig.2. The D Flip-Flop circuit schematic

RI is modeled by a double exponential current pulse [10] using parameters such as current pulse duration τ_{RI_dur} and current pulse amplitude I_{RI} values (Table 1) formed after the generation of the electron-hole pairs. The parameters are based on TCAD simulation data [11,12].

The setup time depends on the “TG1” and “INV1” components [13]. Thus, radiation effects on these components influences the setup time. Therefore, the simulations were performed by modeling RI on “TG1” and “INV1” components. The analysis showed that the setup time is more sensitive when RI occurs on “INV1” gate.

An example of such an impact with $LET = 6 \text{ MeV cm}^2/\text{mg}$ on “INV1” inverter changes the setup time from $40,042\text{ps}$ (when there is no RI) to $83,263\text{ps}$ (Fig.3).

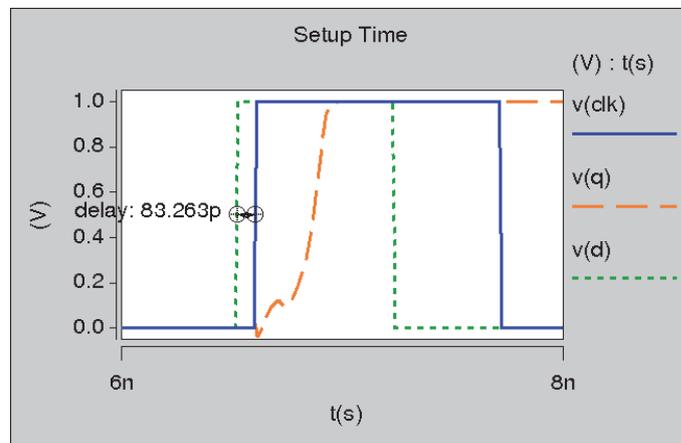


Fig.3. The DFF setup time dependency on $LET = 6 \text{ MeV cm}^2/\text{mg}$

The analysis of hold time has been carried out by applying the RI on “INV0” gate since, the hold time depends on the data signal stability before the inverse clock reaches “TG1”, “TG2” and “TG3”. Measurements before the RI show that the hold time is negative ($-11,7\text{ps}$) which means that the propagation delay from the “D” to node “N1” is enough to transfer the input signal. Whereas, the negative hold time becomes positive and increases with RI on the “INV0” inverter. The hold time of DFF reaches $7,5235\text{ps}$ when there is RI with $LET = 6 \text{ MeV cm}^2/\text{mg}$ on the “INV0” inverter (Fig.4).

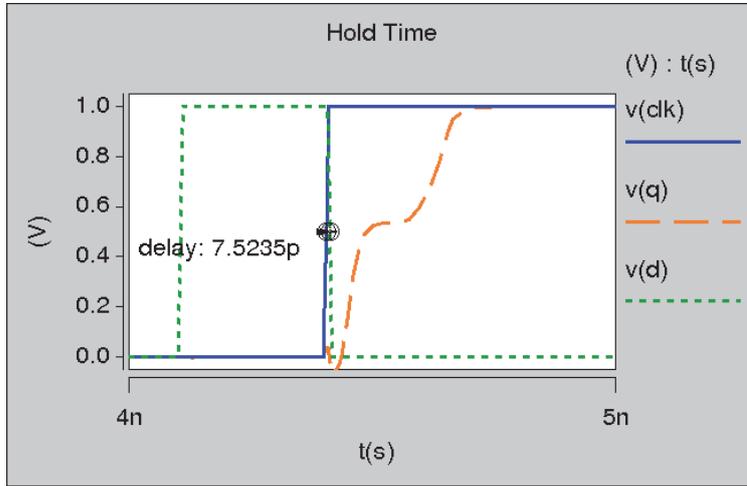


Fig.4. The DFF hold time dependency on $LET = 6 \text{ MeV cm}^2/\text{mg}$

The clock to output delay is formed with the “TG3”, “INV3” components. Without RI the clock to output delay is 186,58ps. However, simulations considering RI show that the clock to output delay is more sensitive to the RI on “TG3”. HSPICE simulation has been done to calculate the delay increase when DFF is exposed to radiation with $LET = 6 \text{ MeV cm}^2/\text{mg}$ (Fig.5).

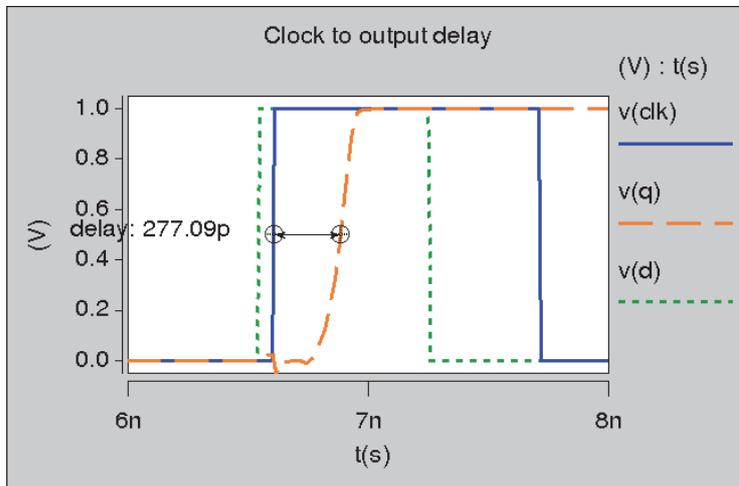


Fig.5. The DFF clock to output delay dependency on $LET = 6 \text{ MeV cm}^2/\text{mg}$

The RI analyses with different LET values were performed using the HSPICE simulator [2] in typical TT, slow SS, and fast FF corner cases. The simulation results show that DFF characteristics are highly sensitive to RI (Table 1).

Table 1

HSPICE Simulation results for D Flip-Flop setup/hold-time and clock to output delay dependency on different radiation-induced LET

LET [MeV * cm^2/mg]	I_{RI} [μA]	τ_{RI_dur} [ps]	T_{setup} [ps]	T_{hold} [ps]	$T_{clock\ to\ output\ delay}$ [ps]
2	55	20	50,49	-7,27	219,62
4	150	80	71,99	1,06	273,01
6	190	150	83,26	7,33	277,09
8	205	180	91,50	11,5	278,87
10	215	190	11,74	13,7	304,54

The proposed analytical model for evaluation of the timing parameters of D Flip-Flops. An alternative solution to setup/hold-time and clock to output delay measurements by SPICE simulation is developed. The method provides a simple and fast calculation of DFF timing parameters without running SPICE simulations.

Polynomial regression analysis [14] is performed for finding the best coefficients for calculating the setup/hold-time and the clock to output timing parameters based on the pre-simulation results.

Assume that $I_n = (I_1, I_2, \dots, I_n)$ is the vector of the current pulse values after the RI, $\tau_n = (\tau_1, \tau_2, \dots, \tau_n)$ is the vector of the current pulse duration and $T_n = (T_1, T_2, \dots, T_n)$ is the vector of each DFF timing parameter. To find the best analytical equation for the timing parameter linear function, quadratic function, cubic functions have been tested. As a result, the desired fitting coefficients for setup time and clock to output delay have been obtained by the quadratic function presented in equation (1), and for hold time the best-fit parameters are found using the cubic function shown in equation (2):

$$T_i = a_1 I_i^2 + a_2 \tau_i^2 + a_3 I_i \tau_i + a_4 I_i + a_5 \tau_i + a_6, \quad (1)$$

$$T_i = a_1 I_i^3 + a_2 I_i \tau_i^2 + a_3 I_i^2 \tau_i + a_4 \tau_i^3 + a_5 I_i^2 + a_6 I_i \tau_i + a_7 \tau_i^2 + a_8 I_i + a_9 \tau_i, \quad (2)$$

where $a_1, a_2, a_3, a_4, a_5, a_6, a_7, a_8, a_9$ are the coefficient variables, I_i and τ_i – the independent variables and T_i is the dependent variable.

To solve the values of coefficient vectors (Table 2) $a_n = (a_1, a_2, \dots, a_n)$ for each parameter, the “NonlinearModelFit” method was chosen in the Wolfram Mathematica tool [15].

Table 2

Coefficient values for setup/hold-time and clock to output delay equations

Parameters	a_{setup}	a_{hold}	$a_{clock\ to\ output}$
a_1	0,00147103	-1,68111	0,000566985
a_2	-0,000161075	-0,0021703	-0,00118727
a_3	-0,214416	-7,18160	0,180444
a_4	0,000547898	0,000408834	-0,000326101
a_5	0,0566388	0,26448	0,426327
a_6	58,8732	4,15321	204,189
a_7	0	-0,00109745	0
a_8	0	0,13157	0
a_9	0	-19,0414	0

Experimental Results. To validate the accuracy of the proposed model, comparisons between the proposed model results and the HSPICE simulation results are performed. The simulations are done with different LET values (Table 1).

A comparison of the setup time evaluation using the proposed model and SPICE simulation results is presented in Fig. 6. Calculations of the setup time are obtained using equation (1) with the corresponding coefficient values (Table 2).

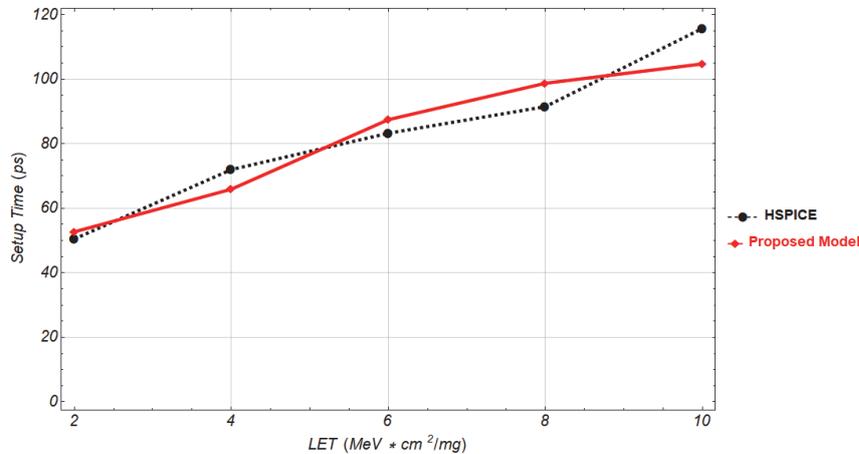


Fig.6. The D Flip-Flop setup time dependency on different energy levels of RI

The comparison is carried out (Fig. 7) for hold time dependency on the radiation effects observed with SPICE simulations and analytical equations using hold time coefficient values (Table 2).

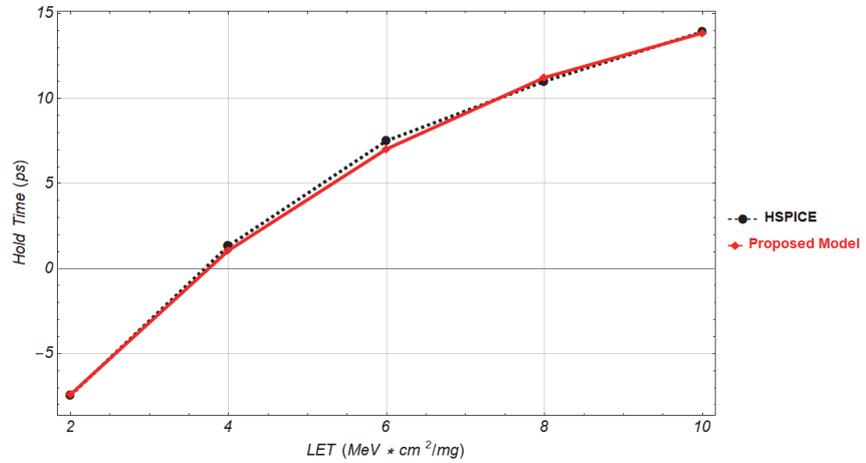


Fig.7. The D Flip-Flop hold time dependency on different energy levels of RI

The clock to output delay measurement comparison is performed (Fig.8) between the results of the HSPICE simulator and the proposed equation (1).

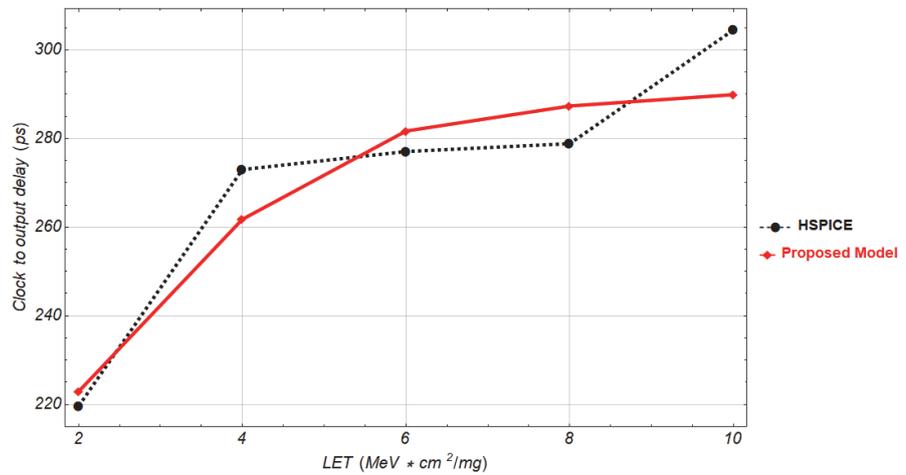


Fig.8. The D Flip-Flop clock to output delay dependency on different energy levels of RI

The comparison shows that the average errors of the proposed model versus the SPICE simulations are 7%, 5.6%, 3%, for setup/hold-time and clock to output delay parameters respectively.

As an example of the model usage in higher abstraction levels of ICs design, the ISCAS89 benchmark S27 circuit [16] was implemented in Verilog and tested in VCS environment [17] considering RI. Simulations are performed using the calculated setup/hold and clock to output delay by equations (1), (2), (3) in case of

LET = 6 MeV cm²/mg irradiation, and the outputs are observed to determine whether there is setup/hold time or clock to output delay violation or not (Fig. 9).

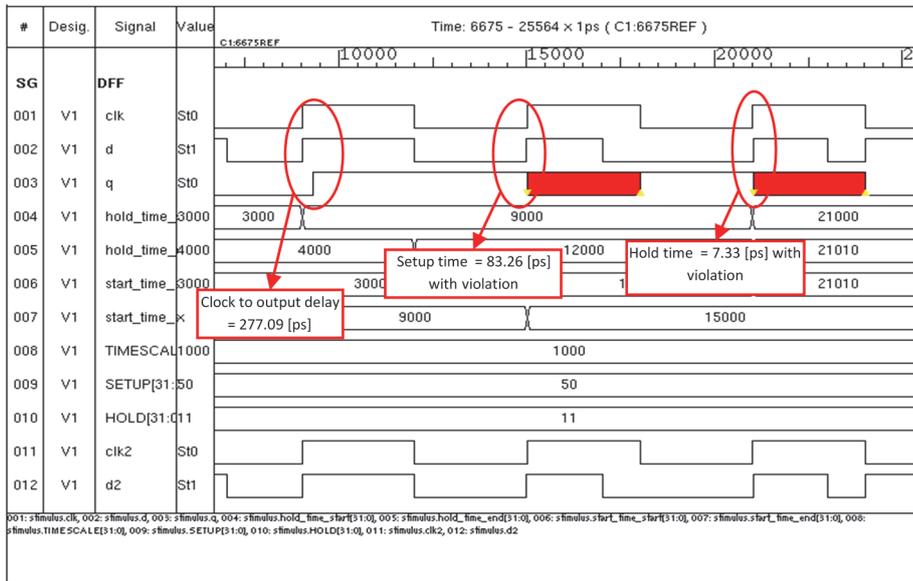


Fig.9. The VCS simulation results of setup/hold time violations and clock to output delay increase in ISCAS89 benchmark S27 circuit

Conclusion. An analytical model of radiation impact on the setup/hold-time and clock to output delay parameters of D flip-flop is proposed. This model was tested using ISCAS89 benchmark circuits in the VCS environment. The experimental results demonstrate the accuracy of the model with evaluation error for setup time 7%, for hold time 5,6%, and for clock to output delay for 3% compared to HSPICE simulator results. The results prove that the proposed analytical model accelerates the design process by providing equations to calculate the timing parameters, which allows estimation of the issues caused by irradiation at the early stage of the development.

REFERENCES

1. **Petrosyan A.A., Petrosyan G.A.** A model for calculating the propagation delay of digital elements considering the radiation impact // Proc. of the RA NAS and NPUA. Ser. of Tech. sc. – 2019. – V. LXXII, N2. – P. 253–263.
2. HSPICE Application Manual, Synopsys Inc. – 2018. – 878p.
3. Mixed-Signal Simulation User Guide, Synopsys Inc. – 2019. – 415p.
4. CustomSim™ User Guide, Synopsys Inc. – 2019. – 313p.

5. **David Dietz.** Stochastic Propagation Delay Through a CMOS Inverter as a Consequence of Stochastic Power Supply Voltage // IEEE Transactions on Electromagnetic Compatibility. – 2019. – V. 61, N1. – P. 226 – 232.
6. Output remapping technique for critical paths soft-error rate reduction / **Q. Ding, Y. Wang, H. Wang, et al** // Computers & Digital Techniques, IET. – 2009. – P. 325-333.
7. A model for transient fault propagation considering glitch amplitude and rise-fall time mismatch / **F. Firouzi, S. Kiamehr, P. Monshizadeh, M. Saremi, et al** // 2nd Asia Symposium on Quality Electronic Design (ASQED). – 2010. – P. 89-92.
8. **Wang Y., Zwolinski M.** Analytical Transient Response and Propagation Delay Model for Nanoscale CMOS Inverter // Proceedings - IEEE International Symposium on Circuits and Systems. – 2009. – P. 2998 - 3001.
9. Custom Compiler™ Simulation and Analysis Environment User Guide, Synopsys Inc. – 2019. – 761p.
10. The Single Event Upset Forecasting in Digital and Analog Integrated Circuits in SAED 14nm FinFet Technology / **V. Melikyan, A. Petrosyan, A. Mkhitarian, A.K. Hayrapetyan, et al** // Problems of Advanced Micro- and Nanoelectronic Systems Development. – Moscow, Russia, 2018. – P. 76–81.
11. **Wang Q., Liu H., Wang S., Chen S.** TCAD Simulation of Single-Event-Transient Effects in L-Shaped Channel Tunneling Field-Effect Transistors // IEEE Transactions on Nuclear Science. – 2018. – P. 99-109.
12. **Gaillard R.** Single Event Effects: Mechanisms and Classification // Soft errors in modern electronic systems. – 2010. – P. 39-48.
13. **Jacob Baker R.** CMOS: Circuit Design, Layout, and Simulation – 3rd edition // John Wiley & Sons. – 2010. – 1214p.
14. **Ambrosius F.** Interpolation of 3D Surfaces for Contact Modeling // B.Sc. report, University of Twente. – 2005. – P. 9 - 11.
15. **Mangano S.,** Mathematica Cookbook: Building Blocks for Science, Engineering // O'Reilly Media, Inc. – 2010. – 827p.
16. **Brglez E., Bryan D., Kouninski K.** Combinational profiles of sequential benchmark circuits // IEEE International Symposium on Circuits and Systems. –1989.–P. 1929–1934.
17. VCS® User Guide, Synopsys Inc. – 2019. – 2106p.

National Polytechnic University of Armenia. The material is received on 18.12.2019.

Ա.Ա. ՊԵՏՐՈՍՅԱՆ

ՌԱԴԻԱՑԻՈՆ ԸԱՌԱԳԱՅԹՄԱՆ ԱԶԴԵՑՈՒԹՅՈՒՆԸ ՀԱՇՎԻ ԱՌՆՈՂ D ՏՐԻԳԵՐԻ ԺԱՄԱՆԱԿԱՅԻՆ ՊԱՐԱՄԵՏՐԵՐԻ ՀԱՇՎԱՐԿՄԱՆ ՄԵԹՈԴ

Առաջարկվում է ռադիացիոն ճառագայթման ազդեցությունը հաշվի առնող D տրիգերի ժամանակային պարամետրերի հաշվարկման մեթոդ: Աշխատանքի նպատակն է տրամաբանական մակարդակի մոդելավորման միջոցներում նվազեցնել ռադիացիոն ճառագայթման մոդելավորման սահմանափակումները: Ժամանակային պարամետրերի որոշման նպատակով դուրս են բերվել վերլուծական բանաձևեր՝ օգտագործելով բազմանդամային մոտարկման մեթոդը: Առաջարկվող մոդելի և HSPICE տրանզիստորների մակարդակի մոդելավորման միջոցի արդյունքների համեմատությունը ցույց է տվել, որ տեղակայման և պահպանման ժամանակների հաշվարկման սխալները համապատասխանաբար կազմում են 7% -ից մինչև 5.6%, իսկ հապաղման ժամանակի տարբերությունը՝ 3%, որը ցույց է տալիս, որ մոդելը արդյունավետ է և կարող է կիրառվել տրամաբանական մակարդակի նախագծման միջոցներում՝ ճառագայթման ազդեցության մոդելավորման նպատակով, առանց ժամանակատար HSPICE մոդելավորման:

Առանցքային բառեր. ռադիացիոն ճառագայթման երևույթ, տեղակայման ժամանակ, պահպանման ժամանակ, հապաղման ժամանակ, էներգիայի գծային փոխանցում, անցողիկ սխալներ, վերլուծական բանաձև, կոմպլիմենտար մետաղ-օքսիդ կիսահաղորդիչ (ԿՄՕԿ):

А.А. ПЕТРОСЯН

МОДЕЛЬ РАСЧЕТА ВРЕМЕННЫХ ПАРАМЕТРОВ D-ТРИГГЕРА С УЧЕТОМ ВОЗДЕЙСТВИЯ РАДИАЦИОННОГО ИЗЛУЧЕНИЯ

Представлена модель расчета временных параметров D-триггера с учетом радиационного воздействия. Основная идея работы заключается в устранении ограничений в процессе проектирования ИС с использованием моделирования на логическом уровне. Получены аналитические выражения для оценки временных параметров с использованием результатов предварительного моделирования и полиномиальной регрессии. Результаты экспериментов подтверждают эффективность предложенной модели. Сравнение с результатами SPICE моделирования показывает, что ошибки оценки времени предустановки и удержания находятся в пределах от 7% до 5,6% соответственно, а разница в установке данных относительно тактового импульса составляет 3%. Это доказывает, что модель эффективна и может быть использована для моделирования временных зависимостей от радиационных воздействий при проектировании логического уровня, без выполнения трудоемких SPICE симуляций.

Ключевые слова: радиационный эффект, время предустановки, время удержания, время установки данных, линейная передачи энергии (ЛПЭ), восстанавливаемые нарушения, аналитические уравнения, комплементарная структура металл-оксид-полупроводник (КМОП).