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Arithmetic Operators Introducing Full Swing High Speed Current-Mode BiCMOS Technology

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Abstract

In this paper we present some multiple valued arithmetic operators introducing high-speed current mode circuits. By applying simple and efficient methods we have reduced the number of transistors and power dissipation. Besides we have achieved a significant improvement in terms of speed and chip area. We have eliminated some parts of circuits and simulated their function with other parts, which results in so many improvements already mentioned.

1. Introduction.

BiCMOS technology offers enhanced performance compared to CMOS. Many high-speed BiCMOS circuits have been fabricated and published in the VLSI literature. Current mode circuits have been always considered as the serious alternative to voltage mode ones.In VLSI literature there are so many reports and publications conceiving the improvements in terms of speed and the number of transistors used. But one of the drawbacks of current mode circuits is the low drive capability when applying large capacitive loads. Current mode circuits demonstrate low performance in this case. For overcoming this problem we have proposed the contribution of bipolar transistors resulting in Current mode BiCMOS circuits. As in the case of voltage mode circuits, the combination of CMOS and Bipolar transistors can improve the overall performance of digital circuits. Multiple valued logic is one of the key technologies for overcoming problems such as wiring and delay.

2. MVL current mode circuits.

Referring to transmission function theory and considering the features of current-mode CMOS multivalued circuits, we distinguish the following two kinds of variables and discuss related basic operations.

(a) switching variables $\alpha,\beta,\gamma : \alpha,\beta,\gamma \in \{T,F\}$, which are used to denote the switching state of a MOS transistor. Their basic operations are NOT(~), AND($\wedge$) and OR($\vee$), and their properties are well known.

(b) Signal variables x,y,z : with values from the set $\{0,1,\ldots,r-1\}$, which are comparable with each other. The values of a signal variable are represented by using current values, such as 0, 10μA,

20μA,...,(r-1)×10μA. If it denotes the detection threshold of current-mode CMOS circuits: t ∈ {0.5,1.5,2.5,...,r-1.5}, the corresponding current values for t are 5μA, 15μA, ..., (r-1.5) ×10μA under the above given condition. Their basic operations are as follows:

Complement operation: $\bar{x} = r - 1 - x$
Minimum operation: $x \wedge y = \min(x,y)$
Maximum operation: $x \vee y = \max(x,y)$

Literal operation:

$$\begin{cases} x^{(i,j)} = r-1, \text{ if } i \le x \le j \\ 0, \text{ otherwise} \end{cases}$$

Sum operation: $x + y$

Note that the same symbols ∧ and ∨ are used to denote different operations: AND and OR operations for switching variables, and Minimum and Maximum operations for signal variables, respectively.

In current-mode CMOS multivalued circuits, the switching state of a pass transistyor is defined by its gate signal, which is usually taken from the output of a current comparator. On the other hand, the switching state of a pass transistor decides whether or not the current signal at the source is transmitted to the drain. In order to describe the link between two kinds of variables, we introduce the following operations:

1. Threshold comparison operations

High-threshold comparison operation

$$x^t = \begin{cases} T, \text{if } x \ge t; \\ F, \text{if } x < t; \end{cases} \quad (1)$$

Low-threshold comparison operation

$$x^t = \begin{cases} T, \text{if } x < t; \\ F, \text{if } x \ge t; \end{cases} \quad (2)$$

The above operations can be realized by using a current comparator and a suitable MOS transistor.

Dual threshold comparison

$$t1_x t2 = {}^{t1}x \wedge x^{t2} = \begin{cases} T, \text{if } t1 \le x < t2; \\ F, \text{otherwise} \end{cases} \quad (3)$$

It can be proved that there exist the following relations in various threshold comparison operations.

(a) NOT relation

$$\neg(x^t) = {}^t x \quad , \quad \sim({}^t x) = x^t \quad (4)$$

(b) AND relation

$$x^{t1} \wedge x^{t2} = x^{t1 \wedge t2} \quad , \quad {}^{t1}x \wedge {}^{t2}x = {}^{t1 \vee t2}x \quad (5)$$

(c) OR relation

$$x^{t1} \vee x^{t2} = x^{t1 \vee t2} \quad , \quad {}^{t1}x \vee {}^{t2}x = {}^{t1 \wedge t2}x \quad (6)$$

(d) Complement relation

$$(\bar{x})^t = {}^{r-1-t}x \quad , \quad {}^t(\bar{x}) = x^{r-1-t} \quad (7)$$

(e) Minimum relation

$${}^t(x \wedge y) = {}^t x \wedge {}^t y \quad , \quad (x \wedge y)^t = x^t \vee y^t \quad (8)$$

(f) Maximum relation

$${}^t(x \vee y) = {}^t x \vee {}^t y \quad , \quad (x \vee y)^t = x^t \wedge y^t \quad (9)$$

2. Transmission operation

$$x^{*}\alpha = \begin{cases} x, & \text{if } \alpha = T; \\ 0, & \text{if } \alpha = F. \end{cases} \quad (10)$$

The following properties can be easily proved.

(a) Repetition Law

$$(x^{*}\alpha)^{*}\alpha = x^{*}\alpha \quad (11)$$

(b) Serial transmission law

$$(x^{*}\alpha_1)^{*}\alpha_2 = x^{*}(\alpha_1 \wedge \alpha_2) \quad (12)$$

(c) Parallel transmission law

$$x^{*}\alpha_1 + x^{*}\alpha_2 = x^{*}(\alpha_1 \vee \alpha_2) + x^{*}(\alpha_1 \wedge \alpha_2) \quad (13)$$

If $\alpha_1 \wedge \alpha_2 = F$, then

$$x^{*}\alpha_1 + x^{*}\alpha_2 = x^{*}(\alpha_1 \vee \alpha_2) \quad (14)$$

(d) Commutative law

$$x_1^{*}\alpha_1 + x_2^{*}\alpha_2 = x_2^{*}\alpha_2 + x_1^{*}\alpha_1 \quad (15)$$

(e) Associative law

$$(x_1^{*}\alpha_1 + x_2^{*}\alpha_2) + x_3^{*}\alpha_3 = x_1^{*}\alpha_1 + (x_2^{*}\alpha_2 + x_3^{*}\alpha_3) = x_1^{*}\alpha_1 + x_2^{*}\alpha_2 + x_3^{*}\alpha_3 \quad (16)$$

(f) Distributive law

$$(x_1^{*}\alpha_1 + x_2^{*}\alpha_2)^{*}\alpha_3 = x_1^{*}(\alpha_1 \wedge \alpha_3) + x_2^{*}(\alpha_2 \wedge \alpha_3) \quad (17)$$

In the above equations the transmission operation * is assumed to take precedence over the sum operation +.

By using the above operations, we can obtain the expression for any multivalued function. Taking quaternary logic as an example, an arbitrary two-variable quaternary function may be expressed as

$$F(x,y) = c_0^{*}(x^{0.5} \wedge y^{0.5}) + c_1^{*}(x^{0.5} \wedge y^{1.5}) + c_2^{*}(x^{0.5} \wedge y^{2.5}) + c_3^{*}(x^{0.5} \wedge 2^{.5}y) + c_4^{*}(^{0.5}x^{1.5} \wedge y^{0.5}) + \quad (18)$$
$$c_5^{*}(^{0.5}x^{1.5} \wedge y^{1.5}) + c_6^{*}(^{0.5}x^{1.5} \wedge y^{2.5}) + c_7^{*}(^{0.5}x^{1.5} \wedge 2^{.5}y) + c_8^{*}(^{1.5}x^{2.5} \wedge y^{0.5}) + c_9^{*}(^{1.5}x^{2.5} \wedge y^{1.5}) +$$
$$c_{10}^{*}(^{1.5}x^{2.5} \wedge y^{2.5}) + c_{11}^{*}(^{1.5}x^{2.5} \wedge 2^{.5}y) + c_{12}^{*}(^{2.5}x \wedge y^{0.5}) + c_{13}^{*}(^{2.5}x \wedge y^{1.5}) + c_{14}^{*}(^{2.5}x \wedge y^{2.5}) +$$
$$c_{15}^{*}(^{2.5}x \wedge 2^{.5}y)$$

According to the definition of threshold comparison operations, any quaternary function can also be expressed as

$$F = 1^{*0.5}f^{1.5} + 2^{*1.5}f^{2.5} + 3^{*2.5}f \quad (19)$$

Synthesis of multivalued function based on the algebraic method and cost comparison

Since circuit realization of a multivalued function based on the algebraic system for current-mode CMOS multivalued circuits corresponds directly to its algebraic expression, the circuit simplification can be reduced to the simplification of its algebraic form. For the convenience of simplification, we give the following useful equations, which may easily be proved by means of the properties and laws in section 2.

$$(x+y)^{*}\alpha = x^{*}\alpha + y^{*}\alpha \quad (20)$$

$$\left.\begin{aligned} x^{*a}y^{b} &= x^{*a}y - x^{*b}y \\ x^{*a}y &= x^{*a}y^{b} + x^{*b}y \end{aligned}\right\} \quad (21)$$

$$\left.\begin{aligned} x^{*a}y + x^{*}y^{a} &= x^{*} \\ x^{*a}y &= x - x^{*}y^{a} \end{aligned}\right\} \quad (22)$$

$$(a+c^{*}by)y^{d} = {}^{a}y^{b} \vee {}^{a+c}y^{d} \qquad (a<b<(a+c)<d) \quad (23)$$

According to eq.(21), eq.(19) can be written as

$$F = 1^{*0.5}f - 1^{*1.5}f + 2^{*1.5}f - 2^{*2.5}f + 3^{*2.5}f = 1^{*0.5}f + 1^{*1.5}f + 1^{*2.5}f \quad (24)$$

Taking a unary quaternary function shown in 2(a) as an example [4]. From the truth table, we have

$$U(y) = 2^{*0.5}y^{*1.5}+1^{*1.5}y^{*2.5}+3^{*2.5}y \quad (25)$$

$$U(y) = 2^{*0.5}y-2^{*1.5}y+1^{*1.5}y-1^{*2.5}y+3^{*2.5}y=2^{*0.5}y-1^{*1.5}y+2^{*2.5}y \quad (26)$$

From eq.(22), the above equation can be changed to

$$U(y)=2^{*0.5}y-(1-1^{*}y^{1.5})+^{2.5}y=2^{*0.5}y+1^{*}y^{1.5}+2^{*2.5}y-1 \quad (27)$$

According to eq.(24), u(y) can be written as

$$U(y)=1^{*0.5}y+1^{*}(^{0.5}y^{1.5}\vee^{2.5}y)+1^{*2.5}y \quad (28)$$

By using eq.(21), eq.(25) can be expressed as

$$U(y) = 2^{*0.5}y^{1.5}+1^{*1.5}y^{2.5}+3^{*2.5}y=2^{*0.5}y^{1.5}+1^{*1.5}y-1^{*2.5}y+3^{*2.5}y=1^{*1.5}y+2^{*0.5}y^{1.5}+2^{*2.5}y$$

From eq.(14), we have

$$U(y) = 1^{*1.5}y+2^{*}(^{0.5}y^{1.5}\vee^{2.5}y) \quad (29)$$

We can get other forms of expression by algebraic means, and it is possible to derive an even simpler circuit construction. Note that 3-y=(3 2 1 0). Moreover, u(y) can be demonstrated into

$$\begin{aligned} U(y) &= (0\ 2\ 1\ 3) \\ &= (0\ 2\ 1\ 0) + (0\ 0\ 0\ 3) \\ &= (3\text{-}y)^{*0.5}y+3^{*2.5}y \end{aligned} \quad (30)$$

If we decompose u(y) into

$$\begin{aligned} U(y) &= (0\ 2\ 1\ 3) \\ &= (0\ 2\ 0\ 2) + (0\ 0\ 1\ 1), \end{aligned}$$

From eq.(23), we have

$$U(y) = 2^{*(0.5+2^{*}1.5y)}y+1^{*1.5}y \quad (31)$$

The assertion follows directly.

Figure 1 demonstrates the realization of G1 function. G1 function is defined as below:

$$\begin{aligned} &X^j \in (0, 1), X \in (0,1,2,\ldots,m\text{-}1) \\ &X^j = 1 \ \text{IF}\ X = j,\ X^j = 0 \ \text{IF}\ X \neq j \\ &G_j, L_j \in (0,1)\ \ ,X \in (0,1,2,\ldots,m\text{-}1) \\ &G_j(x) = 1 \ \text{IF}\ X > j \ \text{else} = 0 \\ &L_j(x) = 1 \ \text{IF}\ X \leq j \ \text{else} = 0 \end{aligned} \quad (32)$$

Without stepping into the details, through studying the simulations of the different designs [4-10], it can be generally concluded that, with changing the (W/L)pu to (W/L)pd ratio in CMOS inverter gates and using a PMOS transistor as a current source or NMOS as its sink, we can apply threshold detector operation and convert voltage to current. This is the main function of the current mode circuit operations.

NPN		
	Ft (GHz)	55
	Fmax (GHz)	110
	Gm/Gee @We-min	1200
CMOS		
	Vdd (V)	3.3 / 1
	Lmin (nm)	65
Resistors	Rs (ohm/sq)	100
Capacitor	C (fF/mm2)	3
Routing	# Layers	6
Top Metal	Thickness (um)	2.5

Table (1) : 0.065 μm technology parameters

In these circuits the threshold detectors are used, which have the duty of specifying different levels of current and different levels of logic will be specified as well. Threshold detectors are used in all of these circuits, they specify, different levels of current and consequently different levels of logic. Fig. (1) shows a threshold detector. The output of this detector is connected to a PMOS transistor gate for converting the output voltage to current.

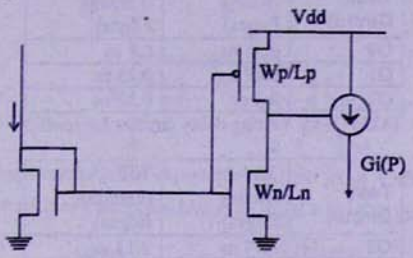

Fig. (1): Circuits test for G1 delay publish

Tables (2-a) to (2-c) specify the different levels of current and the W/L ratio in transistors.

	Threshold 0-1	Threshold 1-2	Threshold 2-3
W_n / L_n	0.065 / 0.065	0.065 / 0.065	0.065 / 0.0975
W_p / L_p	0.065 / 0.065	0.065 / 0.065	0.065 / 0.065
Threshold current	10μA	30μA	50μA

Table (2-a): Sample of Detector for threshold (level 0) .

	Threshold 0-1	Threshold 1-2	Threshold 2-3
W_n / L_n	0.065 / 0.065	0.0975 / 0.065	0.065 / 0.065
W_p / L_p	0.065 / 0.0975	0.065 / 0.0975	0.39 / 0.065
Threshold current	21μA	40μA	62μA

Table (2-b): Sample of Detector for threshold (level 1)

	Threshold 0-1	Threshold 1-2	Threshold 2-3
W_n / L_n	0.0975 / 0.0975	0.0975 / 0.065	0.065 / 0.065
W_p / L_p	0.065 / 0.13	0.195 / 0.065	0.0.2925 / 0.065
Threshold current	10μA	19μA	29μA

Table (2-c): Sample of Detector for threshold (level 2)

Tables (3-a) to (3-c) show the delay in applying **G0** to **G2.**

Test Circuit	Tdr (Rising Edges)	Tdf (Fanning Edges)
G0	0.21 ns	0.1 ns
G1	0.17 ns	0.23 ns
G2	0.2 ns	0.37 ns

Table (3-a): Testing delay circuits for level 0

Test Circuit	Tdr (Rising Edges)	Tdf (Fanning Edges)
G0	0.14 ns	0.13 ns
G1	0.09 ns	0.09 ns
G2	0.09 ns	0.18 ns

Table (3-b): Testing delay circuits for level 1

Test Circuit	Tdr (Rising Edges)	Tdf (Fanning Edges)
G0	0.22 ns	0.065 ns
G1	0.11 ns	0.13 ns
G2	0.08 ns	0.13 ns

Table (3-c): Testing delay circuits for level 2

3. Current mode CMOS circuits.

In voltage mode logic circuits, the variable element is voltage. For example, to show the logic zero, zero volt is used and to show the logic one, 5, 3.3, 2.1 or 1.2 volt or any other voltage can be used. Also, current can be used as a variable. The main advantage of current mode over the voltage mode is that, the summation in current mode is a free operation. If some wires with different currents are connected together, the output current is the algebraic sum of these currents. But in voltage mode, short circuit of the outputs in CMOS circuits must be avoided. As we pointed, it is possible to use current instead of voltage as a variable quantity. Of course, it is obvious that, in current mode circuits the design must be presented in the other way [11-15].

The problem with current mode is that, it is generally more sensitive to noises. In this regard circuit design should change with change of the technology, or in some occasions it may need to be revolved totally. This rarely happens in voltage mode circuit, and with following the λ design rules due to manufacturer instructions major changes are not needed. In current mode every bit has its own sign and it makes this mode very fascinating. The current direction can be used to show the sign, and it eliminates the necessity of using additional bit to show the sign. Another interesting feature in current mode circuits is capability of creating various circuits only by changing the threshold detector, and sometimes by increasing or decreasing the number of inputs solely.

Iin, can be a factor of the unit current, this means that, it can represent the logic two, three, four, etc. For simplicity of understanding this subject, **Iin** can be broken down into different inputs. e.g. 2 or 3 or ... n inputs with unit current instead of one Iin with various currents.

Fig(2) shows the implementation of AND/OR gates. M1 transistor is used to make an algebraic sum of two In1, In2 inputs. The threshold detector unit is shown as an inverter with indication of TD (threshold detector), whenever the algebraic sum of inputs becomes more than the half logic, changes

from high to low happen, this activates the PMOS transistor, which results in having an OR gate. If this converter is set to change when the algebraic sum of inputs becomes the one and half logic, then we have an AND gate.

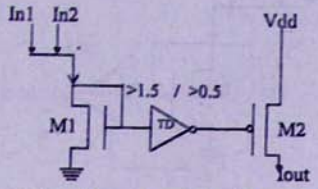

Fig. (2): Implementation of curent mode double input AND/OR gates

Table (4): Another presentation of current mode double input AND/OR gates accuracy

Σ_{in}	Gates		Input Current	Output Current	
	OR_2	AND_2		OR_2	AND_2
0	0	0	0	0	0
0.5	0	0	10μA	0	0
1	1	0	20μA	20μA	0
2	1	1	40μA	20μA	20μA

Table (4) shows the Truth Table of these gates.

Fig (3), shows implementation of Majority function and in the bellow shows the circuit output relationship:

In1In2 + In1In3 + In2In3

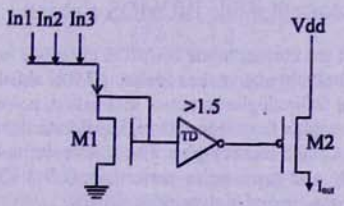

Fig. (3): Majority function

These capabilities in Current mode circuits, and decrease of the number of transistors are very important and crucial. As can be observe, the uniform structure of these designed circuits, easily allows increase of the number of inputs, while in the voltage mode circuits, this is possible only with the increase of the number of transistors. For example, in OR gates it is enough to increase the number of inputs to have ORs with more inputs. Fig. (4), shows a multi input OR circuit. As shown in the Figure, the only change in the circuit shown in Fig. (2), (TD>0.5) is increase of the number of circuit input. In fact there has been no particular changes and the designer with the mentioned capability can, submit the same circuit to the chip manufacturer. The input of the circuit is an aluminum or Polysilicon system; this allows the user to freely assign the number of inputs to the system.

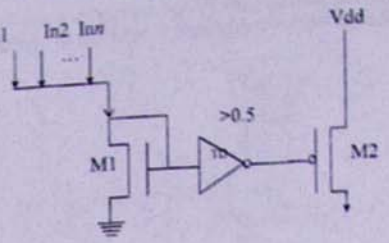

Fig. (4): n-input OR circuit without any change in 2-input OR circuit

The actual operation of these circuits is slightly different with the conventional and expected calculations, and sometimes unexpectedly, from the summation of two currents of a logic circuit, logic two does not result.
This difference increases as the number of inputs increases, but it is not important at all, because the OR circuit will change its condition as soon as it detect the first logic one. In regard to the logic zero, fortunately leakage currents are so small that it can be ignored. Table (5) shows the accuracy of this n-input circuit. For n>2, with incrementing number of inputs, the loss created by leakage of the algebraic sum of the input increases. As mentioned, the threshold detector changes its condition as soon as detecting the first one input. The error in logic zero is so small that it does not concede for analysis. The value for the threshold detector has been defined as logic 0.5, which equivalent current of it is 30 μA. The error from zero to input 7 that is practically used is equal to 5 μA. This can be totally ignored.

4. Design of Full Swing current mode BiCMOS circuits

To understand the behavior of the current mode BiCMOS circuits a brief discussion of conventional voltage mode BiCMOS digital circuits makes sense. CMOS technology provides performance superior to NMOS and bipolar technologies in power dissipation, noise margins, packing density and the ability to integrate large complex functions with high yield. As the name "BiCMOS" implies, it is a combination of Bipolar and CMOS technologies. The bipolar technology is used for high switching speed, high driving capability and good noise performance. But CMOS technology ensures low power dissipation, high noise margin and high packing density.

As it is seen clearly, increasing the number of inputs increases the number of transistors. Using current mode BiCMOS circuits, we are going to find a way in which the number of transistors will not increase, with increasing the number of inputs.
Fig (5) Shows a 2-input XOR circuit with the use of a threshold detector, (TD > 1.5)

Σ_{in}	OR_n	*Input Current*	*Output Current*
0	0	*0+Error(0)*	0
1	1	*μA* 20	*μA* 20
2	1	*μA* 40	*μA* 20
3	1	*μA* 60	*μA* 20
⋮	⋮	⋮	⋮
n	1	*n*20-error(n)*	*μA* 20

Table (5): Truth Table of n-input OR

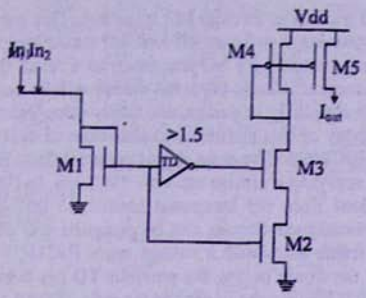

Fig. (5): The modified circuit of 2-input XOR gate

In " algebraic sum of In1 and In2 is greater than logic 1.5, then the output of the threshold detector nanges its state. If the algebraic sum of inputs equals to zero, there is no current at the output. If the mum of these inputs is one (1), since the output of TD is high, the M3 transistor is on. Then input rrent is copied through current mirror (M1, M2), finally input current exactly copies in output. This eans that we will have logic one at the output. When the sum of two inputs is greater than logic 1.5. o other words when two inputs are logic one, then the output of threshold detector changes its state nd becomes Low.M3 transistor switched off and no current will be copied into output. Table (6) ows the accuracy of 2-input XOR.

Σ_{in}	XOR_2	*Input Current*	*Output Current*
0	0	0	0
1	1	20 μA	20 μA
2	0	40 μA	0

Table (6): Truth Table of 2-input XOR

s mentioned previously by using a combination of one TD, one NMOS input transistor and a MOS output transistor, we can develop different circuits, such as multi-input OR, multi-input AND, ajority circuit and etc. It is important to drive current rapidly. Based on investigation done, the st choice is using BiCMOS circuits [16]. Fig. (6) shows a design based on BiCMOS technology r a set of different circuits.

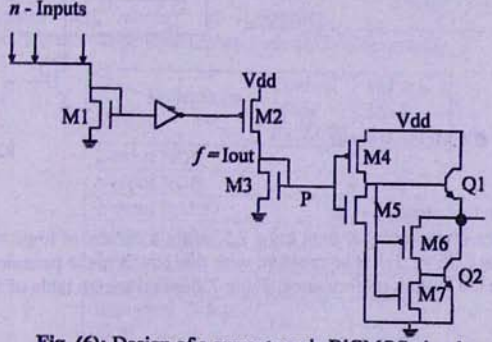

Fig. (6): Design of a current mode BiCMOS circuit

Iout current is applied to M3 transistor, through M2 transistor. This current, increases the voltage of the point P, as a result M4 transistor switches off and M5 transistor, is turned on This causes M6 transistor to be turned on, and switches off M7 transistor, as a result the output of this gate will be logic zero. Also when Iout current is logic zero, the output will be converted to the logic one. The advantage of this circuit is its simplicity in design, and easily using existing layout for BiCMOS part. It should be noted that the delay of this circuit is equal to sum of delays of one current mode logic gate and a standard inverter BiCMOS. The point in this regard is that, TD can be designed by using a standard CMOS inverter by applying a precise ratio of (W/L)pu, to (W/L)pd. Therefore a TD and a P transistor can be eliminated from the integrated circuit. In this case the circuit considerably becomes faster. All of the mentioned circuits can be designed and developed by using the above technique, and with a comparable delay with a voltage mode BiCMOS inverter. Fig. (7) shows this design. As it can be seen in the figure below, the previous TD has been eliminated and M2 and M3 transistors do their functions. It is adequate to choose the ratio of (W/L)pu to (W/L)pd accurately. In fact the combination of M2 and M3 transistors must simulate the TD function. Finally, the output will be presented as 7. R1 and R2 are used to make the circuits Full Swing.

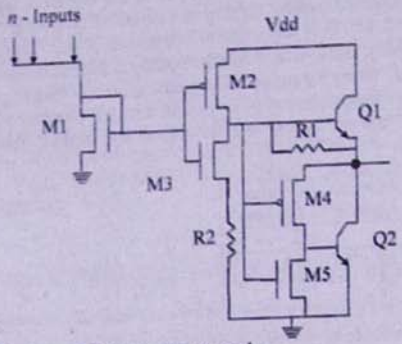

Fig. (7): The improved design of the given BiCMOS circuit.

Fig. (8) shows a 3-input current mode BiCMOS XOR circuit.

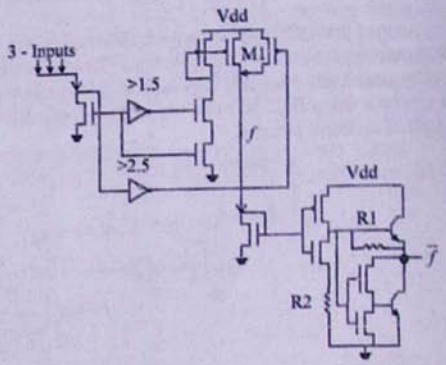

Fig. (8): Current mode BiCMOS, 3- input XOR

The difference between this circuit and 2-input XOR is that, if the input is higher than logic 2.5, again a current of logic one is applied to the system by M1 transistor (TD >1.5). The problem with this circuit is the presence of a lot of current mirrors that slow down the system performance. Table 7 shows the truth table of this circuit.

Input Logic	Input Current	Current f	Logic $\overline{f}$
0	0	0	1
1	µA 20	µA 20	0
2	µA 40	0	1
3	µA 60	µA 20	0

Table (7): Truth Table of the current mode BiCMOS, 3-input XOR Gate

Fig. (9) shows the improved circuit of the previous 3-input XOR Gate using the new logic.

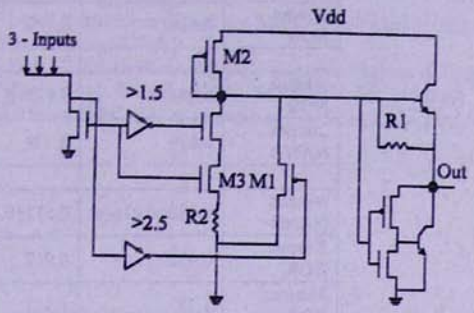

Fig. (9) The improved circuit of 3- input XOR

In the above design, two current mirrors and a CMOS inverter gate are eliminated, which caused a considerable decrease in delay. It should be noted that (W/L) of the M1 transistor is a lot less than (W/L) of M2 transistor, because in the case of $\sum in = 1$, the current passing through M2 is equal to a logic 1 (20 µA). But in the case of $\sum in = 3$ it is obvious that the maximum current which passes through M2 transistor will be 3 times the logic 1, and this current must be limited in some way. This problem by decreasing (W/L) of M1 transistor will be eliminated. In real mode if the BiCMOS designed is used in digital systems voltage mode, it is not necessary to decrement this current, since the output voltage is always equal to Vdd – Vbe. Table (8) compares the delay, in different voltage mode BiCMOS logic with current mode BiCMOS circuit.

Table (8) Amount of speed increase in current mode comparing to Voltage mode

Circuit / Speedup	*NOR*	*NAND*	*XOR*
Maximum Speedup	%15	%14	%6
Minimum Speedup	%12	%13	%17

Based on simulations and as it was discussed, the above ratios show a considerable speed increase in current mode comparing to voltage mode.

Table (9), compares the number of transistors used in different voltage and current mode BiCMOS circuits.

Technology / Circuit	*Current Mode BiCMOS*	*Voltage Mode BiCMOS*
2-input NOR	5	6
n-input NOR	5	$2n+2$
2-input NAND	5	6
n-input NAND	5	$2n+2$
2-input XOR	12	14
n-input XOR	15	24
Improved 3-input XOR	11	14

Table (9) display the number of MOS transistors in the current and Voltage mode BiCMOS circuits **Table (10)**, shows the area of different current and voltage mode gates and also the percentage of improvement of the current mode to the voltage mode area.

Technology / Circuit	*Current Mode BiCMOS* (μm^2)	*Voltage Mode BiCMOS* (μm^2)	Speedup Percent
2-input NOR	0.684	0.779	%12
⋮	⋮	⋮	⋮
n-input NOR	0.684	0.513+0.133(n)	$\%100_{n\to\infty}$
2-input NAND	0.699	0.779	%10
⋮	⋮	⋮	⋮
n-input NAND	0.668+0.016(n)	0.513+0.133(n)	$\%88_{n\to\infty}$
2-input XOR	0.453	0.912	%50
3-input XOR	1.13	1.311	%13

Table (10) Comparison of area of the current and Voltage mode BiCMOS circuits

Conclusion

We have verified the available current mode CMOS logic gates and then we have presented a new multi-valued current mode BiCMOS that is much faster than the similar BiCMOS voltage mode when applying high capacitive loads. In regard to multi-inputs NOR and multi-inputs NAND, comparing to their equivalent voltage mode circuits, increase in speed in the best case is 17% and 6% in the worst case. In the Logic Gates, in the worst case one MOS transistor and in the best condition 2n-3 MOS transistors are eliminated. It should be noted that in NOR and NAND gates, by increasing the number of inputs, the number of MOS transistors used in the circuit will not be changed.

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Appendix

roof of eq.(23)

$+(c*^{b}y))y^{d}={}^{a}y^{b}\vee{}^{(a+c)}y^{d}$

$< b < (a+c) < d$

$0 \le y < a$: eq.(23) reduces to ${}^{a}y^{d}$ and in the given interval its value is F.

$a \le y \le b$: eq.(23) is still equivalent to ${}^{a}y^{d}$, but since $b < d$, in the given interval its value is T.

$b < y < (a+c)$: eq.(23) may be expressed as ${}^{(a+c)}y^{d}$. Taking in account that $b < (a+c)$, it follows that in this interval eq.(23) takes the value F. Finally

$(a+c) \le y \le d$: eq.(23) takes the value T and for $y > d$, the value F.

Թվաբանական օպերատորների միջոցով լրիվ լայնույթով բարձր արագության ընթացքային տեսակի BiCMOS տեխնոլոգիայի ներմուծում

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Ամփոփում

Սույն հոդվածում մենք ներկայացնում ենք բազմանկի արժեքներով թվաբանական օպերատորներ՝ ներմուծելով բարձր արագության ընթացքային տեսակի շղթաներ: