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Compact Transcapacitance Model for Short-Channel DG FinFETs

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Ashkhen Yesayan

Institute of Radiophysics and Electronics, Alikhanian Brothers str. 1, 0203 Ashtarak, Armenia

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Abstract: A compact capacitance model is developed accounting for small-geometry effects in FinFETs. While decreasing the channel length, the transcapacitance model becomes very sensitive to all short channel effects, both in moderate and strong inversion regimes. In addition, for short channel devices, we need to take into account the inter-electrode capacitive coupling in the subthreshold regime, which is not significant for long channel devices. The quantum mechanical effects, which are very significant for thin Fins, are included in the model. The effect of mobility degradation on C-V characteristics is also demonstrated. The model was validated with numerical 3D Atlas simulations and a good accuracy of the model has been demonstrated in all operating regimes.

Keywords: MOSFET, short-channel devices, trans-capacitance, threshold voltage roll-off.

1. Introduction

During the last decade multi-gate MOSFETs become very popular and replace conventional MOSFETs for sub 100 nm CMOS technology [1]. The key factors that limit how far a multi-gate MOSFET can be scaled come from short-channel effects such as threshold voltage roll-off, drain-induced barrier lowering, velocity saturation. The choice of undoped channel is preferable for these devices because of the dopant fluctuation and associated improvement in mobility. Among the great variety of FinFETs the DG FinFET is recognized as the most stable to short channel effects. The progress in compact modeling of multi-gate MOSFET/FinFET is critically important for performing circuit simulations. Among the great variety of published works on this subject the outstanding is charge based compact model based on EKV formalism developed for long channel undoped DG MOSFET [2], which was further extended to short channels [3]. The above mentioned short channel model is based on the exact solution of potential profile along the channel [4] and is fully physics based, thus has no limitations for geometrical parameters of DG FinFET. The another advantage of this model is that it is fully explicit which is important for its implementation in hardware language. The static model developed in [3] includes all short channel effects including velocity saturation effect which is modeled by adopting the channel length modulation concept. However in the development of quasi-static model the velocity saturation effect was not included, instead the constant mobility was considered. In this work, the transcapacitance model including mobility degradation effect for short channel DG-FinFET will be discussed. The presented analytical model will be validated with 3D Atlas simulations.

2. Capacitances model for short channel DG FinFET

The trans-capacitance model we used here is based on the channel charge partition proposed by Ward [5]. Transcapacitances are defined as $C_{ij} = \pm dQ_i / dV_i$ where i, j are standing for gate, source and drain terminals and Q_i is the charge corresponding to the i-th terminal. Expressions for transcapacitances for DG FinFET were derived in [3, 6], considering constant mobility model. Here emphases will be done on quasi static effects arising from channel length reduction. The quantum mechanical effects are included in the model as it was discussed in [3]: where the

structural confinement is modeled as a shift of threshold voltage, and quantum correction to surface potential in high electric fields is accounted as an effective oxide capacitance.

a) Inter-electrode capacitive coupling

For short channel devices, we need to take into account the inter-electrode capacitive coupling [7]. According to Gauss' law, the inter-electrode coupling charge is given by the perpendicular electric field terminating on the chosen electrode. In our model, the normal electric field to the gates in subthreshold regime is calculated from the potential profile introduced in [4]. The inter-electrode coupling charge per channel length is calculated from Gauss' law and then by integrating it over the channel length, we compute the total gate charge. Then corresponding capacitances are calculated as charge derivatives to corresponding terminal voltages. It is worth to note that in sub-threshold regime inter-electrode capacitive coupling has no dependence on terminal voltages and depends only on device geometry. The calculations show that the inter-electrode charge coupling respectively on the drain and source electrodes are:

$$C_{dg\_in} = C_{sg\_in} = C_{gg\_in}/2.$$

We can assume that C_{gg_in} is concentrated in a part of the channel length that we define as:

$$L_p = \frac{C_{gg\_in}}{2HC_{ox}} .$$

Thus, to calculate the terminal mobile charge in moderate and inversion regimes and the capacitance associated with it, we should replace L by $(L - L_p)$.

From comparison with TCAD simulations we have seen that in the saturation region the coupling charge associated with the high transverse electric field near the drain has a significant influence on $C-V$ characteristics in saturation regime. This charge can be calculated from the first-order derivative of potential in this region. By neglecting the mobile charge in saturation region, the potential profile can be derived from Laplace equation. This capacitance (let's define it as C_{gg_in2}) depends on terminal voltages, it is significant in saturation region and vanishes in linear region, thus we add it in the model only in equation of L_p:

$$L_p = \frac{C_{gg\_in} + C_{gg\_in2}}{2HC_{ox}} .$$

The table below demonstrates the significans of inter-electrode capacitive coupling for differend channel lengths, by the means of L_p/L ratio. Calculation have been done for $V_g = 0.6V$ and $V_d = 1V$.

Channel length *L (nm)*	***L_p/L***
20	0.347
50	0.145
100	0.074
1000	0.007

b) Mobility degradation effect

The mobility dependence on the longitudinal electric field becomes significant while shrinking the channel length. In the development of static model, the mobility degradation in high electric field is modeled by the means of channel length modulation [3]. However, in the development of quasi-static model the mobility dependence on longitudinal electric field should

be accurately accounted while calculating charge derivatives. The mobility dependence on the longitudinal electric field can be presented as:

$$\mu_{eff} = -\frac{\mu_{\perp}}{1+\mathrm{E}_{\parallel}/\mathrm{E}_c},$$

where $\mathrm{E}_c = \frac{V_{sat}}{\mu_{\perp}}$ is the electric field at velocity saturation (V_{sat} is the carrier velocity saturation), $\mathrm{E}_{\parallel} = \frac{dV}{dx}$ is the longitudinal electric field, $\mu_{\perp}$ is the transverse effective mobility and is modeled by Mathias's rule. The transverse mobility reduction is due to scattering on acoustic and optical phonons and on surface roughness. The transverse mobility degradation becomes significant for thin body FinFETs. The dependence of mobility on longitudinal electric field is included in transcapacitance model as it was described in [8].

3. Discussion and model validation

The developed capacitance model for short channel DG FinFETs has been compared with 3D Atlas simulations. The mobility model used in Atlas simulations is the CVT model. The following parameters have been used for simulations: the side gate oxide thickness is equal to $1.5nm$, the top gate oxide thickness is of $50nm$, the silicon Fin doping is $N_a = 5\cdot10^{14}cm^{-3}$, the source and drain regions doping is $N_d = 5\cdot10^{21}cm^{-3}$. The Fin height that we simulated is $1\mu m$.

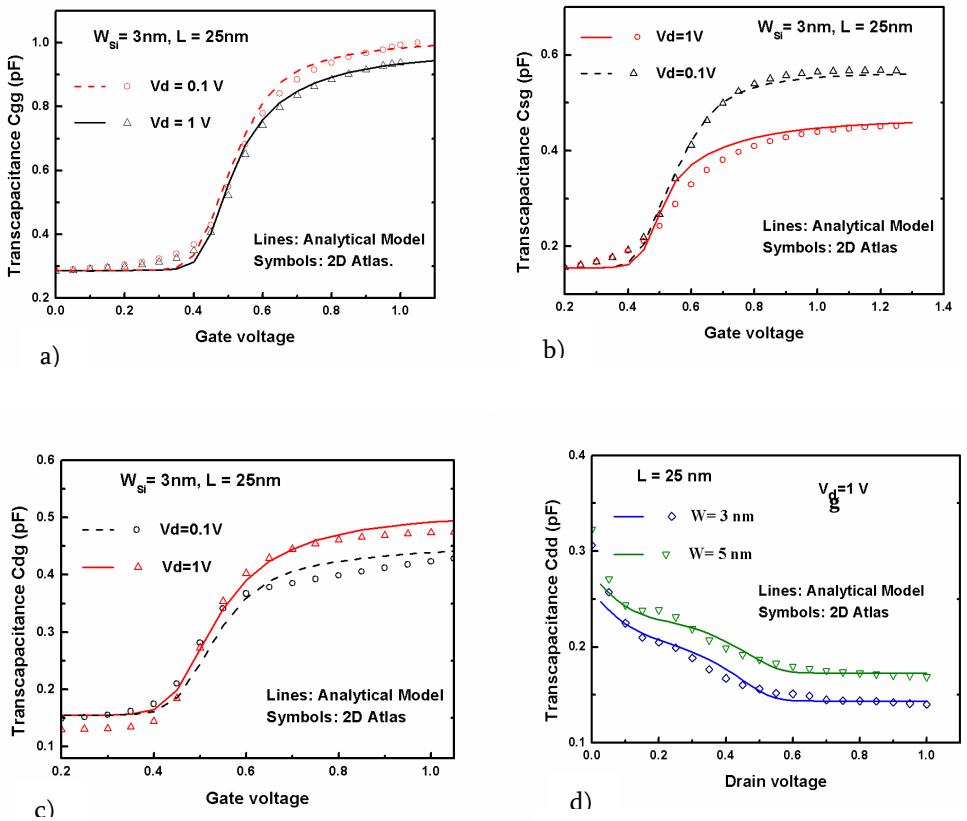

Fig. 1. Transcapacitances C_{gg}, C_{sg}, C_{dg}, C_{dd} obtained from model and simulations are respectively illustrated in figures a), b), c) and d).

Fig. 1 illustrates transcapacitances calculated from the model and Atlas simulations for an ultra-scaled device with channel length $25nm$, and Fin thickness $3nm$. From the good agreement of the model with 3D simulations, is clear that mobility model is well interpreted in the model. The effect of mobility degradation on $C(V)$ characteristics espacially is evident at saturation regime. This can be seen while comparing, e.g. the gate to gate transcapacitance C_{gg} shown in Fig. 1 a), and plots of C_{gg} presented in [3], where constant mobility was considered. Inter-electrode capacitive coupling near the drain at saturation regime is responsible for the specific curvature of C_{dd} plots in linear region (see Fig. 1 d)). The drain charge is very sensitive to all the effects n saturation region. The term C_{gg_in2} included in expression of L_p shapes the curvature of these plots and is sighnificant only for short channel FinFETs.

4. Conclusion

The mobility degradation effect has been introduced in the transcapacitance model for short channel DG FInFET. The extended model preserves the accuracy of previously developed model and is fully physics based. The presented analytical calculations have been validated with 3D Silvaco Atlas simulations as the reasonable replacement of experimental data.

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