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A PROOF OF PRINCIPLE STUDY OF A NOVEL SEMICONDUCTOR-BASED CHARGE PARTICLE IDENTIFICATION TELESCOPE

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Abstract–Charge particle telescopes are the primary equipment for charge particle identification spectroscopy applications in nuclear physics. It is proposed to fabricate the dE/dx detector over a conventional silicon PIN diode detector in a vertical fashion using standard bipolar technology available with Bharat Electronics Ltd (BEL), Bangalore. As a part of this development, the first batch of proto-type Composite Charge Particle Identification Telescope (CCPIT) detectors have been successfully realized. This paper presents a comprehensive perspective on the design, fabrication and characterization of the first proto- types of silicon based CCPITs. Process and Device simulations in Technology Computer Aided Design (TCAD) were employed to extract analytical values for its performance parameters. Dynamic characterization through Alpha particle spectroscopy measurements has been performed to extract the energy resolution of the CCPIT detector.

***Keywords*:** composite charge particle identification telescope, technology computer aided design, pulse height spectra

1. Introduction

Charge particle detector telescopes find wide application in nuclear physics experiments for identification of low and medium energy charged particles and measurement of their energy. Conventional dE/dx detectors are mechanically fragile making their handling very difficult. To attain uniformity of dE/dx detector thickness over a short range of a few microns is also quite a challenge. To circumvent these limitations, a novel integrated solid-state dE/dx particle telescope having both dE/dx and E detectors fabricated over the same semiconductor substrate is being proposed [1]. The proto-typing state development was carried out at the Bharat Electronics ltd. foundry. Prior to the actual fabrication of these devices, a thorough TCAD [2] process and device simulation study was conducted to arrive at feasible values of parameters to be able to fabricate these devices at BEL.

2. Detector Design

The Composite Charge Particle Identification Telescope consists of a dE/dx detector fabricated over a E detector (Fig. 1). These detectors are essentially back-to-back PIN structures. The top dE/dx detector and bottom E-detector share a common n-type buried layer as anode electrode formed by ion implantation of antimony. The E detector is formed within a high resistivity (3–5 kΩ cm) silicon substrate (with thickness 300 μm). The bulk of the dE/dx detector is then formed by an epitaxially grown layer of silicon over the high resistivity substrate after diffusing the

buried *n*-type layer. The contact to the buried layer is obtained by diffusing phosphorus from the topside. To reduce the out-diffusion of dopant from the buried layer, which reduces the active volume of the Δ*E* detector, antimony has been used as dopant for buried *n*-type layer. In order to optimize the critical process parameters for buried layer growth, contact to buried layer, dead layer of the entrance window, etc., extensive 2D process simulation study has been carried out and the optimized process for fabrication of the Composite Charge Particle Identification Telescope has been discussed in next section. Photograph of the CCPIT detector die packaged in transmission mount configuration is shown in Fig. 2.

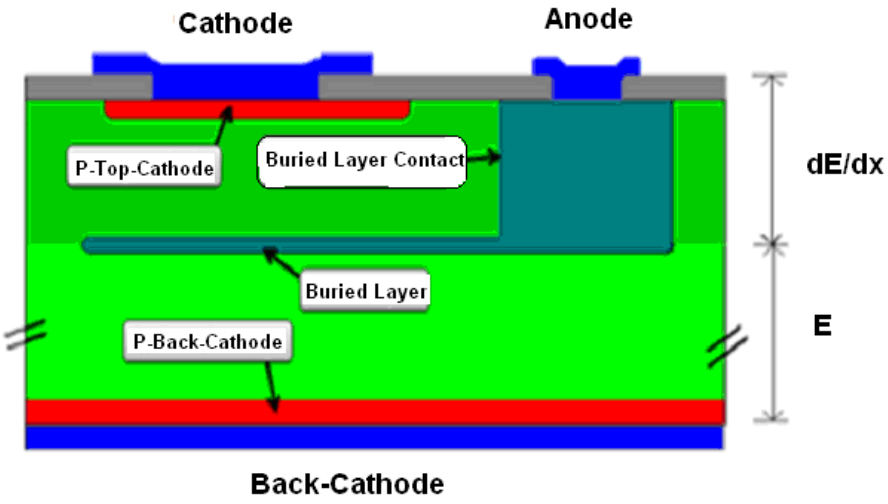

Fig. 1. 2-Dimensional cross-section of the designed Composite Charge Particle Identification Telescope.

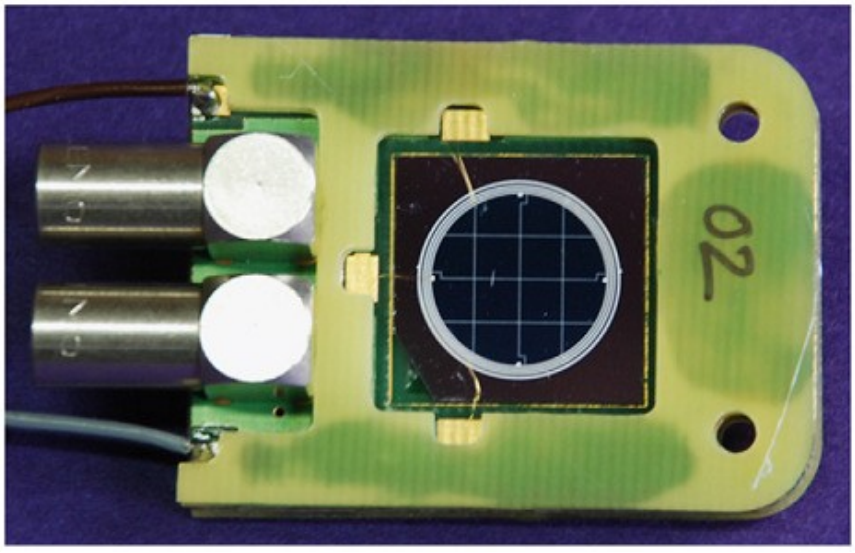

Fig. 2. Photograph of the CCPIT Detector die packaged in transmission mount configuration over a standard pcb.

3. Technology Development

The purpose behind performing process simulations was to arrive at an optimized process within the technological limitations of the BEL fabrication lab. The process was designed with a view to achieving a very low leakage current.

Starting with an *n*-type high resistivity (3–5 kΩ cm), <111>, double side polished silicon wafer, an initial oxide was grown employing the dry-wet-dry oxidation regime (temperature = 1050°, total time = 2 hours and 30 minutes). This was done to have a good quality (dry) oxide at the Si–SiO_2 interface whereas the bulk oxide was grown through wet regime to reduce oxidation time for growth of a 0.6 μm thick oxide.

An n^+ region around the buried layer was defined by a lithographic step (Mask-1), which was followed by an oxide etch step to expose the substrate to phosphorus implantation (energy = 80 keV; dose = 1×10^{16} cm^{-2}).

Subsequently, the *n*-buried layer was defined (Mask-2) and antimony implantation (energy = 80 keV; dose = 3.8×10^{15} cm^{-2}) was performed followed by a drive-in step to form the buried layer.

Next, an *n*-type epitaxy was performed to form the bulk for the dE/dx detector to a thickness of 15 μm. Further from this; the low resistance contact (Fig. 1, buried layer contact) to the buried layer region was defined (Mask-3). Phosphorus gas based diffusion was performed at a temperature of 1020°C for 20 minutes to form the n^+ contact to the buried layer region.

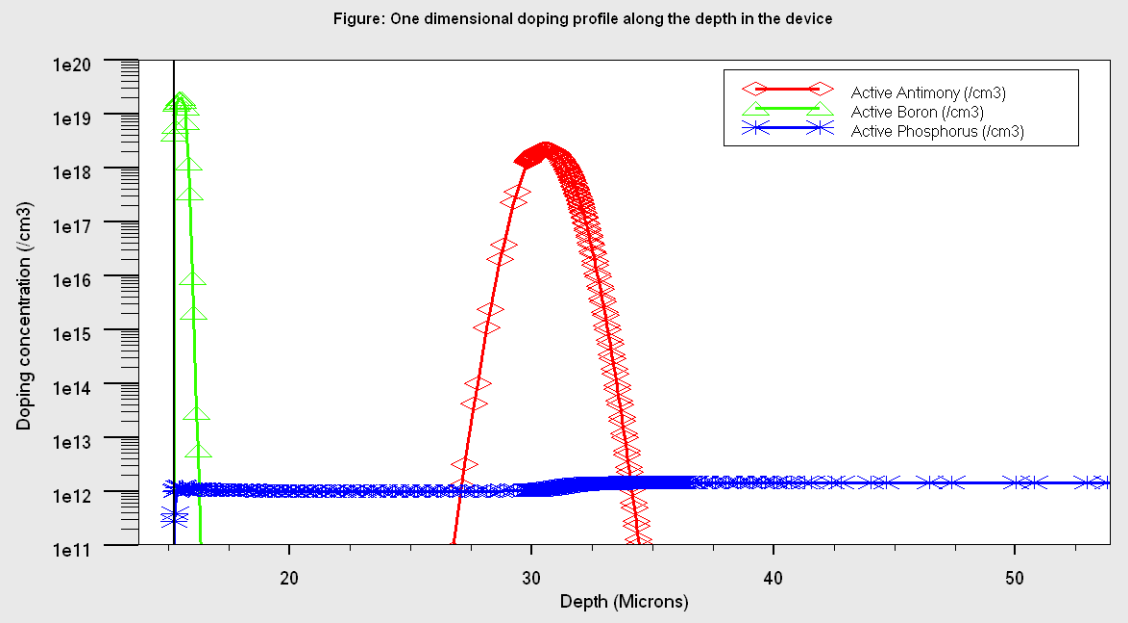

Fig. 3. One-dimensional doping profile along depth in the device.

The fourth and fifth lithographic steps were to define the p^+ cathode regions for both dE/dx and E detectors of the CCPIT. A boron implantation (energy = 80 keV; dose = 1×10^{15} cm^{-2}) followed by a drive-in diffusion cycle forms the cathode regions.

The next lithographic steps (Mask-6 to 9) for contact window definition and metal pattern definition on both front and back side followed by passivation opening step culminates the process for fabrication of the CCPIT detector. The one-dimensional doping profile across the p^+ cathode

along the depth is shown in Fig. 3. The virtual device obtained from the optimized process parameters was then ported to the device simulator. Parameters such as electric fields, potential distribution, etc. were obtained from device simulations as discussed in the next section.

4. Device simulations

A device simulation of the current–voltage characteristics (I–V characteristics) was performed for the CCPIT Detector employing a rectangular mesh in 2-dimensional geometry using Silvaco ATLAS Device Simulator. The virtual device was already constructed using the process simulator and was ported as input to the device simulator. An optimized mesh was generated with a maximum number of grid points (~20,000), which is the grid point limit in ATLAS device simulator. The grid density in this case worked out to be 0.282 grid-points / Unit Area, which is the maximum possible density for this structure. Appropriate voltages were applied to metal electrodes viz. Anode, top cathode and bottom cathode, guard-ring-1 (G1), guard-ring-2 (G2). The Poisson and continuity equations were solved at every grid point with appropriate initial guesses using Newton's method.

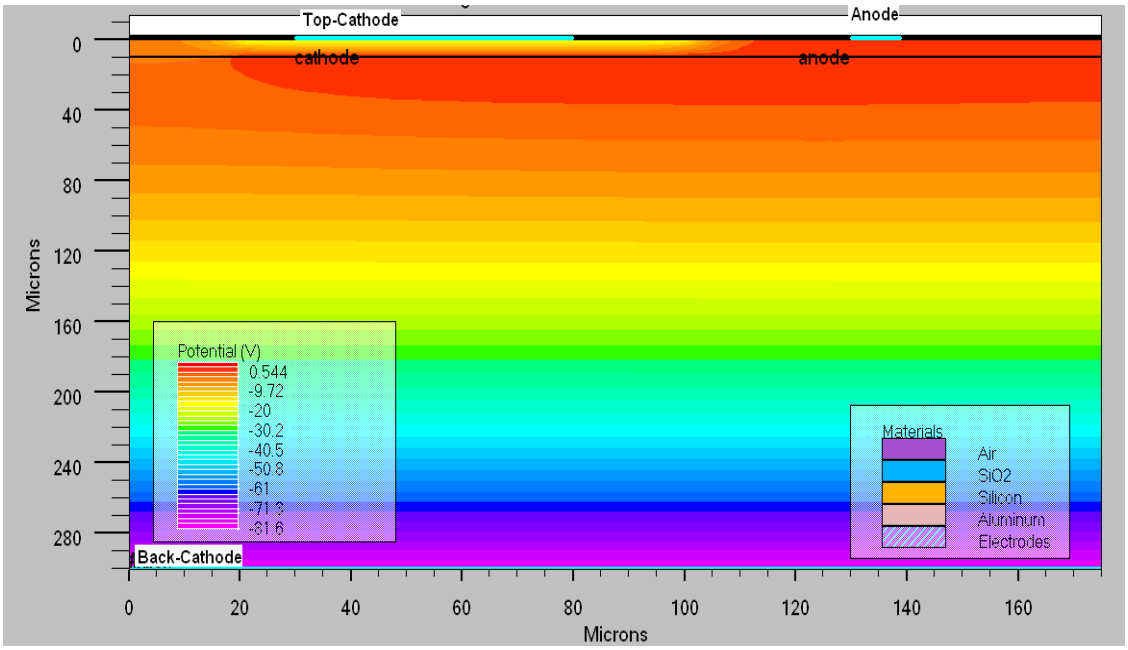

Fig. 4. Two-dimensional potential contour in the device.

The potential distribution in the CCPIT detector resulting from application of a dc reverse bias of –20 Volts on the top cathode and –80 Volts at the back-cathode w.r.t zero bias at the anode is shown in Fig. 4. The terminal currents were also extracted for anode, cathode and back-cathode electrodes. The I–V characteristics (Fig. 5) showed an increase of anode current from zero to -60 Volts, which is the full depletion voltage of the *E*-detector. The device structure was then subjected to a pulse of electromagnetic radiation and the resultant current pulse at the anode was also extracted (Fig. 6).

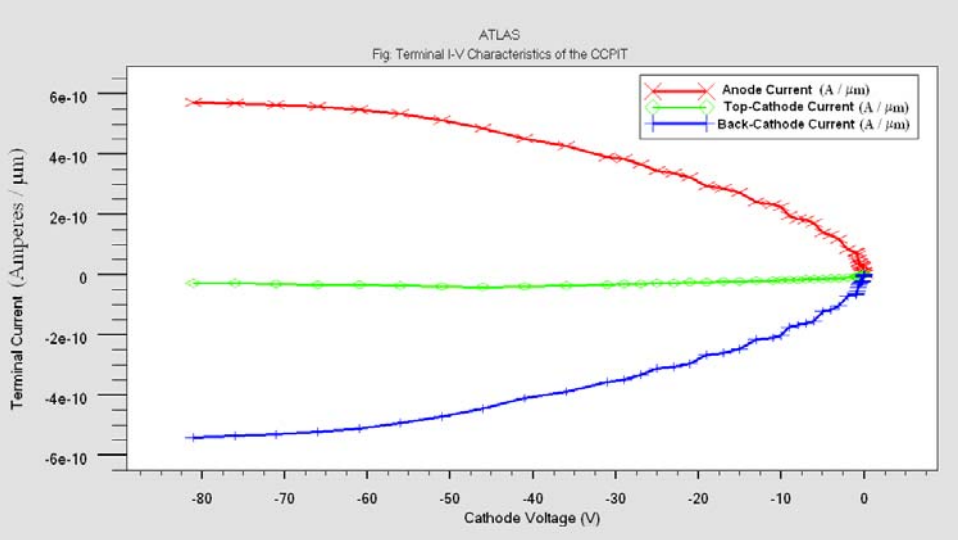

Fig. 5. Current–voltage characteristics of the CCPIT detector.

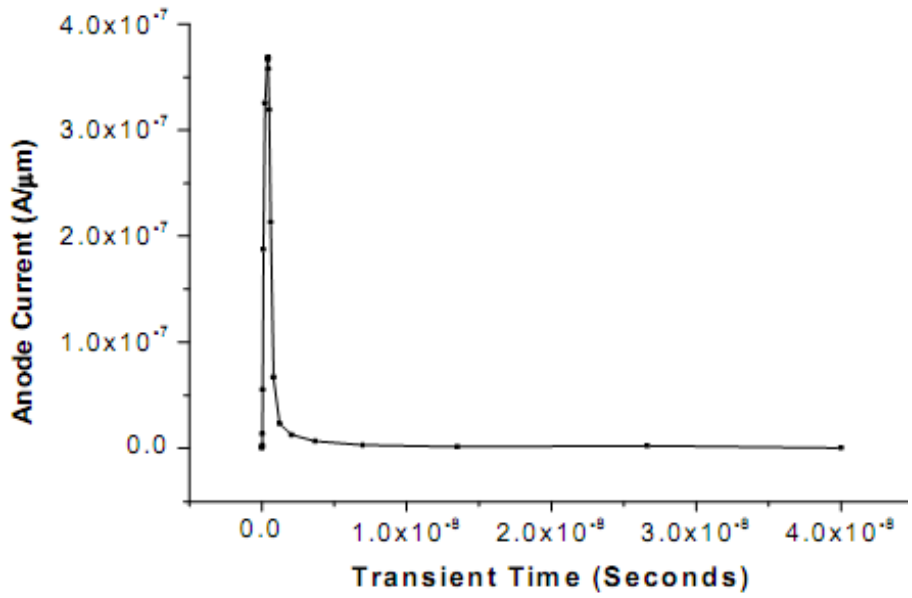

Fig. 6. Anode current pulse after exposure to radiation.

5. Mask Layout

The mask set for the CCPIT Detectors was designed considering the design rules applicable for fabrication of these detectors at Bharat Electronics Ltd. (BEL), Bangalore. The mask layout consisted of 10 mask layers applicable for definition of various regions within the detector. The mask set was designed considering a lithographic resolution of 4 microns, which is the minimum achievable resolution at BEL. The mask layout consists of various devices having different geometries (Circular and Square) and having different total active area (100mm2 and 50mm2), which have been incorporated to study the effect of a variation in geometry and area on the output parameters of the charge particle Detector. Apart from that, there were test devices which were solely meant to study the performance of the dE/dx detector and the E-detector separately with a

view to get an estimate of the output current, capacitances etc. in these devices. Lastly, there were test structures, which were meant to test the quality of fabrication run at BEL. These devices are essentially *p*-*i*-*n* diodes, four-probe structures, MOS capacitors and one special kind of structure, which was meant for evaluating the resistance of the buried layer. Figure 7 shows a pictorial view of the composite mask layout for the 4-inch wafer showing all layers. Figure 8 presents the mask layout for an individual CCPIT detector design (Circular-100mm^2).

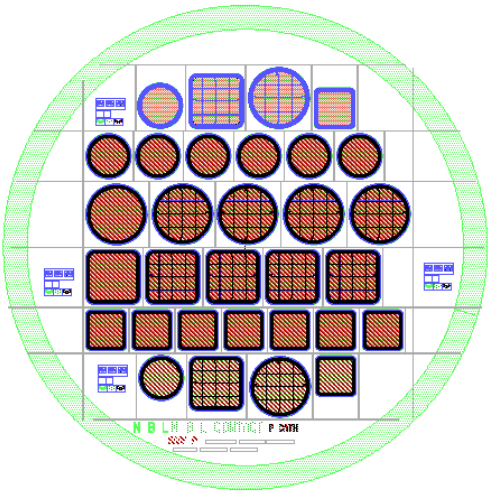

Fig. 7. Layout of 4-inch wafer showing all mask layers.

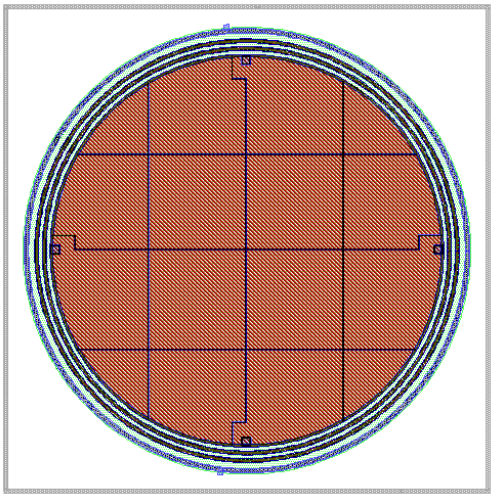

Fig. 8. Illustration showing the mask design of Circular-100mm^2 detector die.

Design Rules applicable at BEL

1) Minimum contact width equal to 5 μm.

2) Minimum distance of contact from p^+ or n^+ edge equal to 4 μm (from all sides).

3) Minimum metal overlaps over contact equal to 3 μm (from all sides).

4) Minimum distance of p^+ region edge with in n^+ region equal to 4 μm (from all sides)

5) Minimum metal-to-metal spacing greater than or equal to 6 μm (from all sides).

6) Minimum metal width greater than or equal to 8 μm.

6. Results and discussions

The CCPIT detector has been packaged in transmission mount configuration over a patterned pcb with wire bonding on both sides of the pcb (Fig. 2). The detector has been characterized for its dynamic performance using a 238 Pu and 239 Pu dual alpha sources. The test setup consisted of a preamplifier, shaping amplifier, high voltage source and a DAQ. The measurements were carried out in a vacuum chamber and the source to detector distance was optimized to get best energy resolution. The energy resolution of the E detector has been observed to be better than 30 keV while the dE/dx detector showed the energy resolution of about 120 keV (Figs. 9 and 10). This was expected, as the terminal capacitances of the dE/dx detector are quite large owing to large area and a thinner active volume.

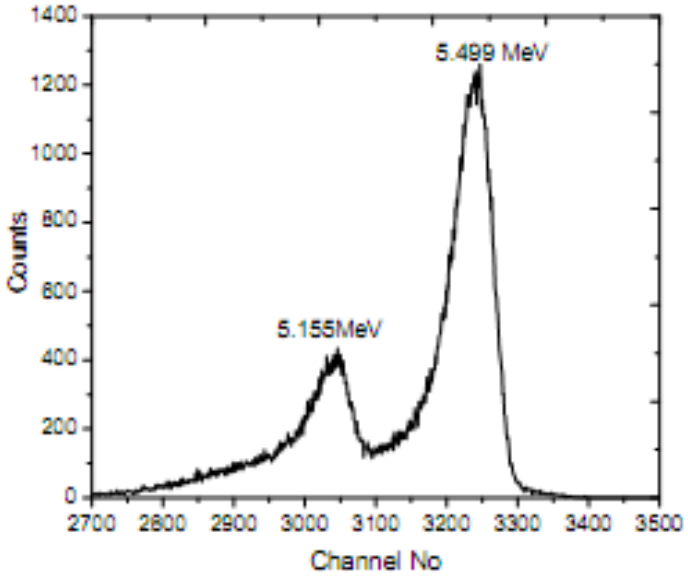

Fig. 9. Pulse height spectrum of dE/dx detector.

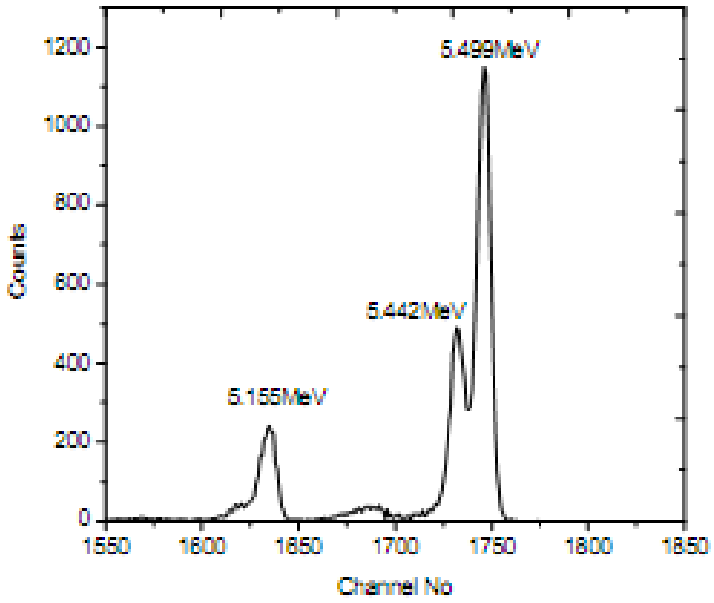

Fig. 10. Pulse height spectrum of *E*-detector.

7. Conclusions

First proto-types of silicon CCPIT detectors have been successfully fabricated at BEL, Bangalore. Process technology for fabrication of CCPITs at BEL has been developed employing simulation studies in TCAD. Analytical values of dc performance parameters have been derived from TCAD device simulations. Dynamic characterization of the CCPITs has been performed.

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