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ELABORATION AND INVESTIGATION OF SEMICONDUCTOR NANOSTRUCTURED OPTOELECTRONIC DEVICES

HABILITATION THESIS

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ACTUALITY OF THE PROBLEM

Today the development of information and high technologies, transition from microelectronics to nanoelectronics, as well as the realization of newly proposed demands of the characteristics of semiconductor optoelectronic devices is mainly conditioned not only by the improvement of optical, photoelectrical and other properties of devices, but their elaboration as well, based on artificial semiconductors and multilayer heterostructures.

Transition from microelectronic devices to the state-of-the-art nanoelectronic devices through epitaxial technologies from the point of view of research and industrial applications requires investigation of phenomena and regularities caused by the decrease of sizes. Conditioned by several atomic layers the influence of change of sizes on the characteristic parameters of semiconductor optoelectronic devices, such as tunnel junctions through quantum barriers and capture of charge carriers by quantum wells, can essentially change the density of states of the quasi-particles, the renormalization of forbidden band (as compared to bulk ones), the efficiency, threshold current, etc. of nanostructured devices.

Thus, knowledge of optical, photoelectrical and other properties of low-dimensional systems, their nanoscale investigation, observation of new quantum effects in nanostructures, as well as the design, elaboration and investigation of them is actual.

THE AIM

In order to obtain high-quality heterostructures and to design and elaborate new-generation high-quality and efficient nanostructured optoelectronic devices (monolithically integrated solar cells based on GaAs on silicon substrates with high crystallographic indices, heterostructure thermophotovoltaic cells, extremely broadband multiple-quantum-well semiconductor optical amplifiers, multiple-quantum-well semiconductor lasers, tunable laser diodes, nanowire structures, quantum-dot nanolayer structures for quantum-dot semiconductor lasers) on the basis of lattice mismatched semiconductor crystals by means of choosing technological regimes (elaborated to provide exact sizes of structures consisting of a few atomic layers) and buffer

layers, buffer super-lattices, quantum wells, nanowires, nanolayers with quantum dots and to suggest methods for the improvement of their characteristics.

INTRODUCTION

During the design and fabrication of semiconductor devices with low-dimensional structures the issues of obtaining a) high-quality hetero-interfaces and b) exact sizes of semiconductor structures formed on a few atomic layers become actual. The sizes of defects conditioned by lattice mismatch are sometimes close to those of nano-layer structures made up of a few atomic layers. Elimination or passivation of such defects becomes important in the elaboration of high-quality semiconductor nanostructured optoelectronic devices. So, it is unavoidable to develop new technological processes and elaborate adequate regimes, which will allow to considerably decrease:

a) the sizes of defects in the hetero-interface from the characteristic sizes of the structure (thickness of the thin layer etc.),
b) big lattice mismatch between semiconductor crystals,
c) or passivate the density of defects and dislocations, generation and recombination centers in the hetero-interface, and the micro- and nano-cracks on the surface.

In the present work the big lattice mismatch of semiconductor crystals has been experimentally decreased by means of introducing buffer layers or buffer super-lattice in semiconductor nano-layers in the case of presence or absence of the surface active spices (surfactants). The density of defects and dislocations in the hetero-interface, generation and recombination centers, surface micro- and nano-cracks has been decreased by means of the following:

a) introducing the buffer layer into the thin layers in the presence or absence of the surface active spices,
b) introducing the buffer super-lattice into the nanostructures,
c) chemical treatment and secondary thermal treatment of the fabricated structure,
d) introducing a window layer into the structure,
e) shifting the hetero-interface from p-n junction in the structure, and
f) using silicon substrate with high crystallographic index (bent substrate) in the structure.

To obtain a high-quality hetero-interface and avoid the defects and dislocations it is especially important to apply a substrate with high crystallographic index, i.e. bent substrate (cutting of the crystal towards some plane at the angle of 1-6^{o}), in which case the formed terraces favor the stage-by-stage, dense arrangement of the neighboring atoms of both sides of the hetero-interface. Thus, it is possible to control the arrangement of neighboring atoms of the

hetero-interface in the atomic scale and hence prevent the process of formation of defects and dislocations.

Mainly low-doped thin layers have been used in semiconductor nanostructured optoelectronic devices to reduce the influence of compound atoms on the quality of the hetero-interface to some extent.

By solving the problem of obtaining high-quality interface and through epitaxial technologies allowing to obtain one atomic layer it is possible to a) decrease mechanical and thermal strain in the hetero-interface, b) obtain relaxed and high-quality nano-layers and finally elaborate efficient and high-quality new generation of semiconductor nanostructured optoelectronic devices based on not only lattice matched semiconductors, but also those with great lattice mismatch (≤ 7.54 %).

During the elaboration of the above-mentioned technological regimes the choice of the epitaxial method and the conditions of epitaxial growth of the crystals, such as growth temperature, the flow of materials on the substrate, the substrate temperature, surface active spices, voltage applied to the sample, the current passing through the sample and so on are very important.

In this thesis materials, geometrical and energetic band structures, parameters and characteristics of semiconductor nanostructured optoelectronic devices (monolithically integrated solar cells based on GaAs on silicon substrates with high crystallographic indices, heterostructured thermophotovoltaic cells, extremely broadband multiple-quantum-well semiconductor optical amplifiers, multiple-quantum-well semiconductor lasers, tunable laser diodes, nanowire structures, quantum-dot nanolayer structures for quantum-dot semiconductor lasers) are also described.

1. MONOLITHICALLY INTEGRATED SOLAR CELLS ON THE SILICON SUBSTRATES WITH HIGH CRYSTALLOGRAPHIC INDICES

For decades, a highly sought-after heteroepitaxial system has been the monolithic integration of GaAs-based materials on Si [1, 2]. The ability to produce high-quality GaAs on a Si substrate is desirable for many reasons, including the low cost, high mechanical strength, and large area of Si substrates, as well as the possibility of integrating A^3B^5 optoelectronic devices with Si very large scale integrated (VLSI) circuitry.

Si possesses far superior substrate properties with respect to mass density, mechanical strength, thermal conductivity, cost, wafer size and availability. Unfortunately the 4% mismatch in lattice constant between Si and GaAs leads to a high density of threading dislocations in GaAs overlayers grown on Si. This severely reduces the GaAs material quality, carrier lifetimes, and

device performance. A^3B^5/Si monolithic integration has potential benefits, and is driving the investigation of many methods of controlling and reducing dislocation densities in these lattice-mismatched heterostructures. These approaches include the insertion of various A^3B^5 intermediate layers based on compositionally graded A^3B^5 buffer layers and strained layer superlattices.

Ge is a very good intermediary between GaAs and Si because of its complete miscibility with Si and the close lattice match between bulk Ge and GaAs (0.07% at room temperature).

One of the main drawbacks of monolithic integration is the mismatch of the both lattice constant and the thermal expansion coefficient between A^3B^5 material and silicon. High thermal mismatch can lead to high-density arrays of the cracks in the thin film.

In this chapter the issues of monolithic integration of solar cells based on GaAs on Si substrates are investigated, which include their structural, electrical and optical investigation with an aim to obtain efficient and high-quality nanostructured optoelectronic devices. For that reason it is important:

- to understand the mechanisms of interface formation and strain relaxation in lattice-mismatched systems, in order to create heterostructures with specific optical and electrical properties such as high carrier mobilities and high luminescence efficiencies;
- to fabricate efficient A^3B^5 semiconductor structures and devices on silicon.

By choosing optimum molecular-beam epitaxy (MBE) and low-energy plasma enhanced chemical vapor deposition (LEPECVD) growth conditions, surface active spices and introducing Ge and $In_xGa_{1-x}As$ buffer layers we succeeded in eliminating the antiphase domain formed by lattice mismatch between GaAs and Si, control and decrease the density of threading dislocations and defects in the interface, as well as micro- and nano-cracks on the surface of GaAs structure. For that reason, at first, anti-phase domain is eliminated, and then the density of threading dislocation and defects are controlled or decreased in GaAs/Si structure, as a result of which a smooth and almost perfect Ge buffer layer is grown on Si substrate. On the next step by introducing $In_xGa_{1-x}As$ buffer layer with optimum parameters (thickness and x concentration) the density of surface micro- and nano-cracks is decreased. Optimum conditions of epitaxial growth are chosen in two ways: by choosing a) technological regimes of the growth and b) the parameters of the grown devices. As a result efficient and high-quality GaAs/Si solar cells are fabricated.

Epitaxial growth equipment consists of:

1. A^3B^5 MBE system for GaAs and $In_xGa_{1-x}As$, with effusion cells for Ga, Al, In and As and reflection high-energy electron diffraction (RHEED),

2. LEPECVD system for SiGe, with a gas supply system for silane, germanium, hydrogen and two doping gases: diborane and phosphine.

SiGe epitaxial layers were grown by LEPECVD and A^3B^5 heteroepitaxial structures were monolithically integrated onto these by MBE.

1.1. INVESTIGATION OF THE Si(113) CLEAN SURFACE

1.1.1. STRUCTURE OF THE Si(113) CLEAN SURFACE

The Si(113) surface has received much attention because of its high stability and technological importance. In general, high-index Si surfaces tend to be unstable and to facet into lower-index planes upon annealing [3, 4]. However, the Si(113) surface is an exception. It has an energy that is comparable to that of the low-index surfaces and therefore it has potential as a substrate for growth [5]. Recently, a lot of effort has been made to improve epitaxial growth of such materials as Ge on Si. Although one can hardly understand initial stages of epitaxial growth without being aware of the atomic structure of the substrate, there is at least one silicon surface which is of potential interest for epitaxy [6], but which has an unknown microscopic structure [7]. Experimental and theoretical issues have been previously carried out to study the atomic structure of the Si(113) surface. The first scanning tunneling microscopy (STM) determination of the Si(113) structure was carried out by Knall and his co-workers [8]. In low electron energy diffraction (LEED) pattern a 3×1 reconstruction is observed. The second STM study on Si(113) supported the 3×1 reconstruction [9]. At the moment there is a majority of studies [3, 5, 8, 10-16] supporting a 3×2 structure at 300 K while others [9, 17] argue for a 3×1 structure. Jacobi and his co-workers [11, 18, 19] have found that at 300 K Si(113) surface has a 3×2 reconstruction that is transformed into a 3×1 structure. Despite all these studies, the atomic structures and relative stability of these reconstructed surfaces are still not completely solved. For the Si(113) 3x1 surface, several structural models have been suggested, such as Runke's "dimmer and adatom" model [20], Dabrowski's model with interstitial Si [21], and the packering model [22]. However, the detailed atomic structure of the Si(113) surface is not determined completely.

A substantial modification of the film growth may be obtained by introducing a third element which lowers the surface free energy of both Ge and Si. Surface active species (surfactant) mediated epitaxy [23] of semiconductor surfaces has attracted considerable interest recently because it enables the growth of structures, which are not achievable by conventional MBE or chemical vapor deposition (CVD). So far Sb [24] and Bi [25] have been reported to successfully act as surfactants for growth of Ge on Si(111). Both lattice strain and surface free energy help to determine whether a film undergoes layer-by-layer growth (Frank-van der Merwe), islanding (Volmer-Weber), and layer-by-layer growth followed by islanding (Stranski-Krastanov). The

study of intrinsic Ge growth on Si, however, is the basis for any analysis of surfactant mediated epitaxy.

The STM images and the LEED patterns provide information about the reconstruction and morphology of the Si(113) surface and Ge/Si(113) interface. The experiments were carried out in an ultrahigh (UHV) STM system. Nominally undoped Si(113) samples with a resistance of 10 ohm cm and a size of 2 mm×5 mm were used for substrates. The samples were cut from highly oriented Si(113) wafers with a remaining miscut of less than 0,02 degrees. After cleaning in methanol, the samples were inserted into UHV system through a load lock and degassed at about 600°C for more than 24 hours. The substrates were flashed by short annealing cycles up to 1200°C for nearly 15 seconds in order to remove any contamination. The samples were resistively heated directly by DC current and the sample temperature was measured using an infrared pyrometer. This procedure reliably resulted in the removal of the native oxide layer and in the formation of a well-ordered Si(113) surface reconstruction, which was checked by LEED and STM.

For the growth of Ge films atomic Ge was evaporated from Ge Knudsen cell. The Ge growth deposition was set between 300° and 600°C. Subsequently LEED and STM measurements were performed at room temperature. The base pressure in the UHV system was below 5×10^{-11} mbar and did not exceed 1×10^{-10} mbar during Ge deposition.

Before epitaxial growth it is important to get information on the surface of the substrate by spectroscopy [26-41], electronic microscopes [42-44] and surface analyzing techniques [42, 44].

In this section the STM images and the LEED patterns were used for the analysis of the atomic structure, morphology and reconstruction of the Si(113) clean surface. Surface reconstruction and atomic model of Si(113) surface is determined, which is not finally determined yet [41]. The STM images of the Si(113) clean surface at different scales as well as the LEED patterns taken at various energies of electrons are shown in Figs. 1.1 and 1.2, respectively.

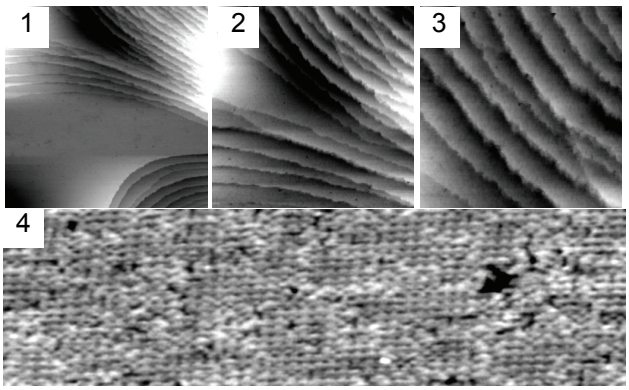

Fig. 1.1. The STM images of the clean surface of Si(113)-3×2 reconstruction. The scan areas are 1000 nm × 1000 nm (1), 500 nm × 500 nm (2), 250 nm × 250 nm (3), 56 nm × 13 nm (4) using sample voltage of –2 V and tunnelling current of 0.3 nA.

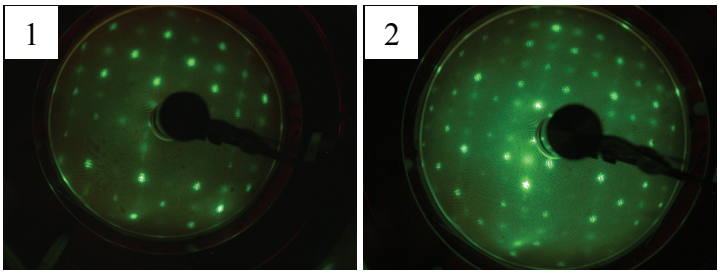

Fig.1.2. The Lof Si(113)-3×2 reconstruction. Electron energies are 40 eV (1), 75 eV (2).

For large-area scans, individual steps are found for the Si(113) clean surface according to the remaining miscut of the substrate. No indication for facet formation was found. The LEED images were recorded at 40 eV and 75 eV electron energy. Investigations of the STM (at atomic scales) (Fig. 1.1) and LEED (Fig. 1.2) images allow to differentiate single atoms of the Si(113) clean surface (Fig. 1.1, images 4) and determine the surface reconstruction. Both the STM images and the LEED patterns of the Si(113) clean surface show a 3x2 reconstruction.

1.1.2. INSPECTION OF THE Si(113) SUBSTRATES BEFORE EPITAXIAL GROWTH

Before epitaxial growth of semiconductor multilayers by MBE the wafers (Si substrates with Ge virtual substrates) grown by LEPECVD were inspected by atomic force microscopy (AFM). Then different heterostructures based on GaAs were grown by MBE using the optimum growth conditions.

1.2. MBE AND LEPECVD GROWTH OF HIGHLY PURE A^3B^5 SEMICONDUCTOR THIN FILMS AND SUPERLATTICES ON THE SILICON SUBSTRATES WITH HIGH CRYSTALLOGRAPHIC INDICES

1.2.1. INITIAL GROWTH STAGE, MODE AND BEHAVIOR OF GERMANIUM CRYSTALLISATION ON SILICON

In this section the initial stage, mode and behavior of the submonolayer and multilayer epitaxial growth of Ge on Si(113) (growth kinetic and the morphology of grown surface) at high temperature sphere of the substrate (300-600^{o}C) in the absence and presence of surfactants (Sb and Bi) [42, 43], as well as the surface reconstruction and morphology of Ge/Si(113) [244] with an aim to obtain Ge smooth thin film on Si(113) clean surface are investigated.

The growth of Ge epilayer on Si substrate is prospective for elaboration of the devices with low cost and high velocity (i.e. transistor), and nano-islands grown by Stranski-Krastanow method - for low-dimensional structures. The structure of Ge surface (like Si surface) has decreasing atomic step monolayer, which does not favor the growth of smooth thin films. Thus,

the growth of Ge on Si mostly takes place by islands. There are several approaches to change the growth mode of Ge islands on Si, such as by introducing a) buffer layer, b) surfactant, and c) anti-surfactant to obtain certain surface morphology, i.e. smooth two-dimensional thin films or three-dimensional islands.

For the beginning let's discuss the sub-monolayer growth of Ge on the Si(113) clean surface. During 15 minutes' deposition of Ge atoms on the clean Si(113) surface at 300°C temperature of the substrate there is sub-bilayer coverage of Ge on the Si(113) surface (Figs. 1.3 and 1.4). Scattering Ge islands were formed on the Si(113) surface with single atomic steps. As the mobility of atoms at 300°C growth temperature is low, they are not able to reach the edges of atomic steps and generate a chemical bond. Hence, at 300°C temperature Ge islands were formed on Si(113) surface and there is no layer-by-layer growth. In other words, Ge coverage can't cover the whole surface and only Ge piles are observed. STM and LEED investigations at atomic scale show that the Ge/Si(113) structure has 3×2 reconstruction with some row-like structures in the STM images (Figs. 1.3 and 1.4).

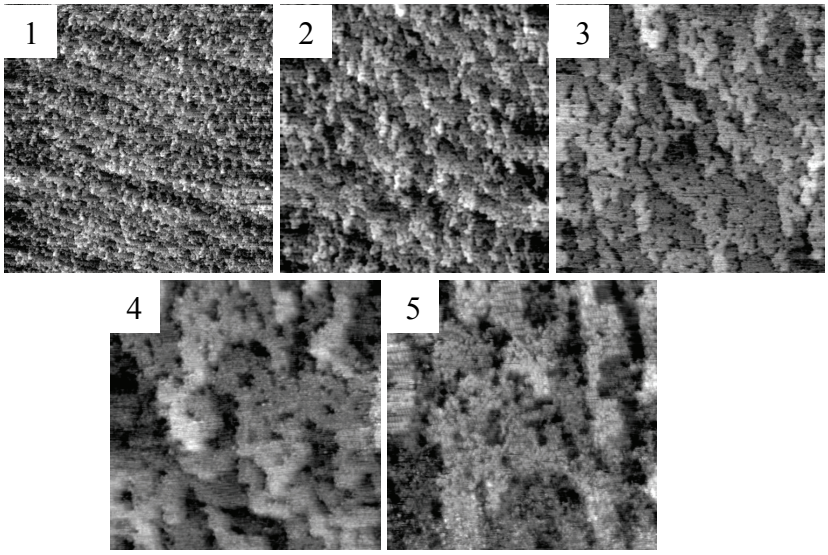

Fig. 1.3. The STM images of the Si(113) surface after 15 minutes' Ge deposition grown at 300°C, The scan areas are 1000 nm × 1000 nm (1), 500 nm × 500 nm (2), 150 nm × 150 nm (3), 100 nm × 100 nm (4), 75 nm × 75 nm (5) using sample voltage of - 2 V and tunneling current of 0.3 nA.

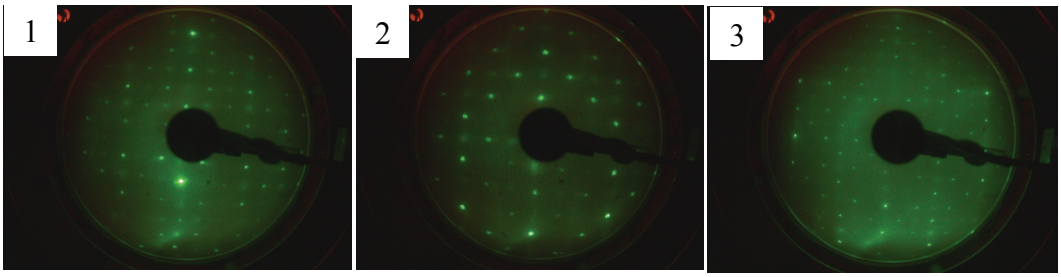

Fig. 1.4. The LEED patterns of Si(113) reconstructions, after 15 minutes' Ge deposition at 300°C sample temperature. Electron energies are 53 eV (1), 81 eV (2), 130 eV (3).

Then, the temperature on Si(113) substrate was increased from 300°C to 430°C. The STM and the LEED images after 2 minutes' deposition of Ge atoms on the clean Si(113) surface at a substrate temperature of 430°C are shown in Figs. 1.5 and 1.6, respectively. After 2 minutes' deposition of Ge atoms only very few patches of Ge atoms were observed on the clean Si(113) surface at the 430°C substrate temperature (Fig. 1.6). Investigation of the Ge/Si(113) surface via UHV STM and LEED (Figs. 1.5 and 1.6) patterns showed that the surface with Ge piles has 3×2 reconstruction, which coincides with the reconstruction of the Si(113) surface of the substrate. The reason for this coincidence is that the amount of Ge on the surface is considerably small and the Si(113) substrate surface with Ge piles is very close to the Si(113) clean surface. The LEED pattern is the same as the initial (3×2)-surface: sharp spots, very low background intensity, indicating a nearly perfect surface.

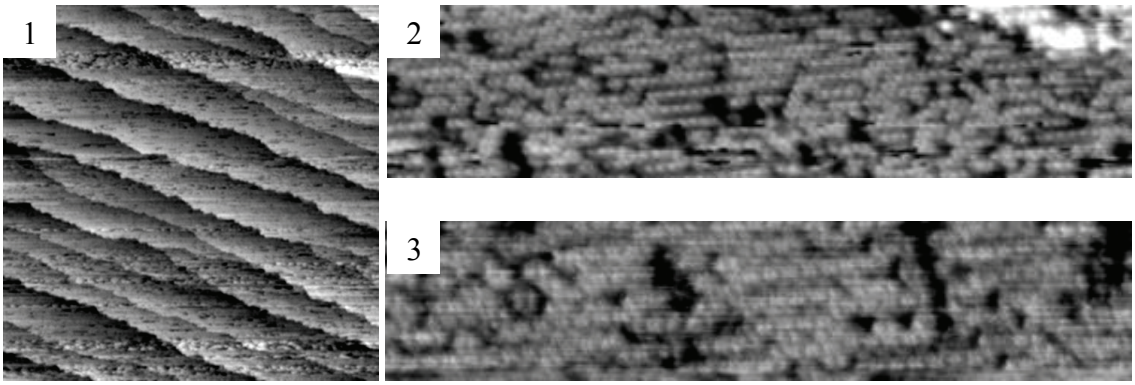

Fig. 1.5. The STM images of Si(113)-3×2 surface with Ge coverage after 2 minutes' deposition at 430°C sample temperature. The scan areas are 500 nm × 500 nm (1), 70 nm x 17 nm (2), 43 nm × 8 nm (3) using sample voltage of -2 V and tunneling current of 0.3 nA.

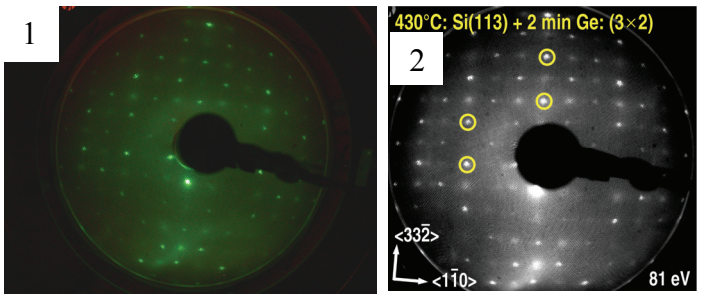

Fig. 1.6. The LEED patterns of Si(113)-3×2 reconstruction, after 2 minutes' Ge deposition at 430°C sample temperature. Electron energies are 53 eV (1), 81 eV (2).

After increasing the duration of the deposition of Ge atoms on the clean Si(113) surface up to 15 minutes at the same temperature of the substrate (Figs. 1.7 and 1.8) the sub-layer coverage of Ge atoms is observed at the atomic step edges of the Si(113) surface. Ge growth is by islands and not layer-by-layer. Preferential nucleation of Ge at step edges can be attributed to a larger number of dangling bonds available at the steps. As Ge does not wholly cover Si substrate, the

STM and the LEED investigations at atomic scale showed that Si(113) surface has the 3×2 reconstruction and Ge/Si(113) structure – the 2×2 reconstruction (Fig. 1.7, image 5 and Fig. 1.8, image 2). The 2×2 reconstruction of the obtained Ge coverage surface coincides with the results obtained in [45]. The 2×2 model of Ge atomic structure on the Si(113) surface is shown in Fig. 1.9.

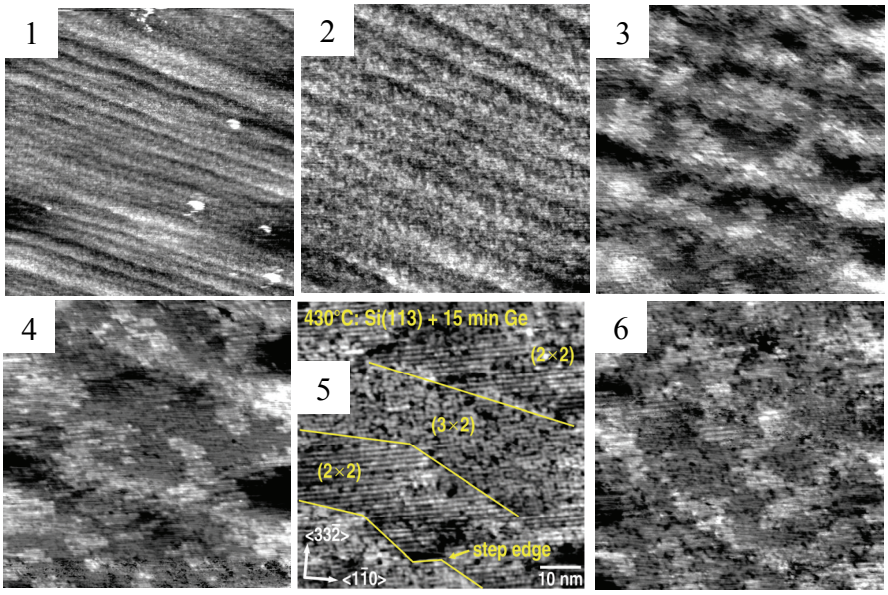

Fig. 1.7. The STM images of Si(113)-3×2/3×1 surface with Ge coverage after 15 minutes' deposition grown at 430°C sample temperature. The scan areas are 1000 nm × 600 nm (1), 500 nm x 500 nm (2), 200 nm × 200 nm (3), 100 nm × 100 nm (4), 70 nm × 70 nm (5), 50 nm × 50 nm (6) using sample voltage of - 2 V and tunnelling current of 0.3 nA.

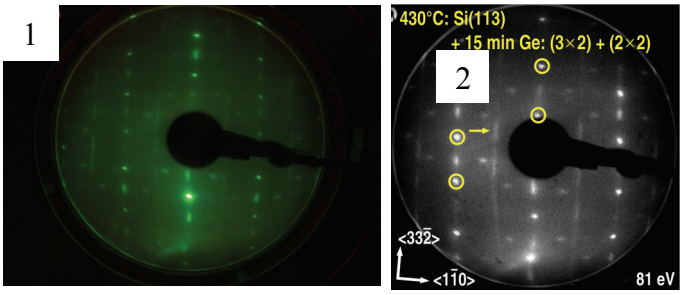

Fig. 1.8. The LEED patterns of Si(113)-3×2/3×1 reconstructions, after 15 minutes' Ge deposition at 430°C sample temperature. Electron energies are 53 eV (1), 81 eV (2).

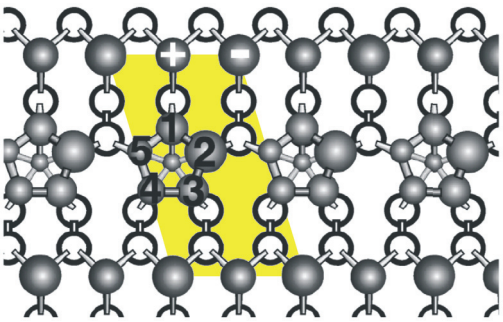

Fig. 1.9. 2×2 model of Ge atomic structure on the Si(113) surface

By further increasing growth duration of Ge atoms (30 min) at 430°C substrate temperature the growth occurs by islands as well, which are formed on the smooth part of the Si(113) surface steps (Fig. 1.10 and 1.11). Average sizes of islands are 100-200 nm and the height - 4–6 nm (Fig. 1.12, image 1). At atomic scale STM and LEED investigations show that the Ge/Si(113) surface has a mixture of the reconstruction of 3×2 and 2×2, which can be attributed to remaining by open Si(113) and Ge coverage areas, respectively.

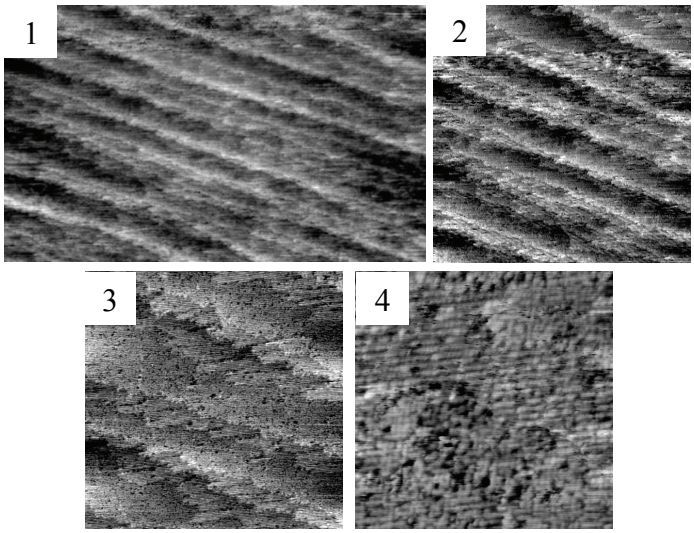

Fig. 1.10. The STM images of the Si(113)-3×2 surface with Ge coverage at different areas (nm^2) at 430°C substrate temperature, deposition time of Ge - 30 min, voltage applied to the sample - 2 V, tunneling current - 0.3 nA, 1 - 1000 × 600, 2 - 500 × 500, 3 - 200 × 200, 4 - 70 × 70

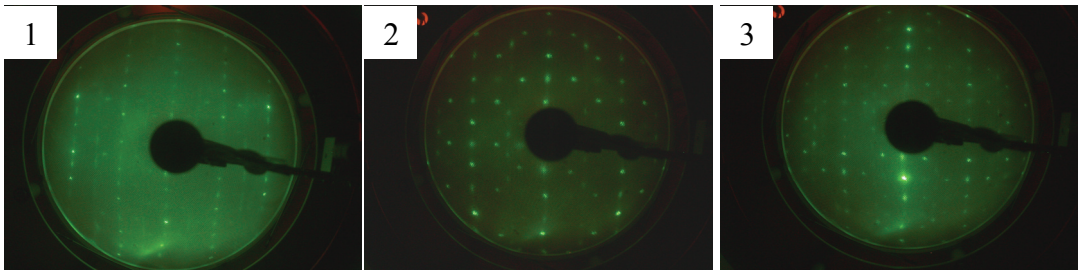

Fig. 1.11. The STM images of Si(113)-3×2 surface with Ge coverage at different electron energies and at 430°C substrate temperature after 30 minutes Ge deposition (eV), 1 - 53, 2 - 81, 2 - 130

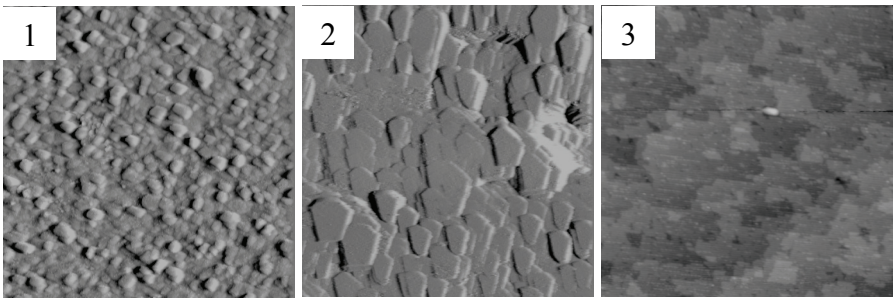

Fig. 1.12. The STM images of the Si(113)-3×2 (1 and 2) surface and the Si(113):Sb (3) interface with the Ge coverage at different temperatures and areas at voltage applied to the sample - 3 V, tunneling current - 0.5 nA, 1) 430°C (1000 nm^2), 2) 600°C (1000 nm^2), 3) 600°C (200 nm^2)

By increasing Si(113) substrate temperature (from 430°C to 600°C) Ge growth on the Si(113) surface again occurs by islands (Fig. 1.12, image 2). Besides, at 600°C temperature the lengths of the islands increase by several times, and the height and density decrease (compared with 430°C substrate temperature). The height of islands decreases by 2–3 times and makes ~2 nm (Fig. 1.12, image 2). That is, it can be said that a very small coverage of the islands of Ge is formed, which is very close to the smooth thin layer.

To obtain smoother and considerably homogeneous Ge thin layer, surfactants (Sb or Bi) are used. The Si(113) surface with Ge coverage at Ge growth temperature of 600°C in the presence of Sb surfactant is shown in Fig. 1.12, image 3. As a result, smooth and almost perfect thin layers are obtained (Fig. 1.12, image 3). Such a result is obtained when bismuth is used as a surfactant.

Analysis of the RHEED images also shows that the Ge/Si(113) surface has a high quality and the 2x2 reconstruction (Fig. 1.13). This result coincides with those obtained by us and other authors.

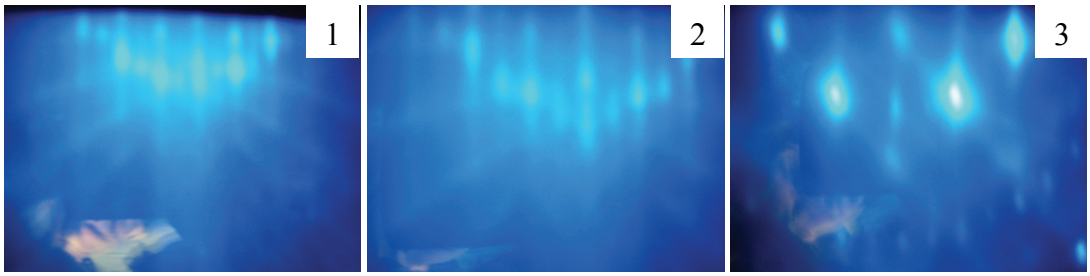

Fig. 1.13. The RHEED patterns of Ge/Si(113) interface at different crystallographic directions 1 - [110], 2 - [$\bar{1}$10], 3 - [010]

Thus, in the case of the sublayer growth the STM and LEED investigations of initial stage, shape and behavior of Ge crystallization on the Si(113) surface confirmed that the presence of the surfactant favours the change of growth method (growth by islands becomes layer-by-layer) and an almost perfect, atomic smooth thin layer on the Si(113) surface is obtained (Fig. 1.12, image 3), which have 2×2 reconstruction. Roughness of the surface of relaxed Ge thin layer with thickness of 5 nm is a few Angstroms.

LEEM investigations of the initial stage, mode and behaviour of multilayer growth (6.5-15 monolayer) at 380-590° substrate temperature sphere confirm the above-mentioned results (Fig. 1.14) [46]. Ge growth on the Si(113) substrate occurs by three-dimensional round nano-islands at 380° substrate temperature (Fig. 1.14, image 1), which is also observed at STM and LEED investigations. Analysis of the LEED images is hows that the surface of islands has 2×2 reconstruction, which is conditioned by Ge wet layer [47]. Parallel to the temperature growth the

shape of nano-islands changes from round to lengthy (440-590°) and is oriented towards [332] crystallographic direction (Fig. 1.12, image 2), because of relaxation of anisotropic mechanical strain. This growth crystallographic direction coincides with the results obtained in [48, 49]. By increasing temperature the Ge islands get stretched and are oriented towards [332] crystallographic direction, and the density of islands decreases. Thus, in the case of multilayer (6.5-15 monolayer) growth, the sizes of islands increase parallel to the temperature growth (380-590°C), and their density decreases. At 380° temperature and at 6.5 monolayer of Ge the density of islands is 1100×10^6 cm^{-2} (a), 440°C - 118×10^6 cm^{-2} (b), 490°C - $26\cdot10^6$ cm^{-2} (c), at 540°C – 5.2×10^6 cm^{-2} (d), and at 590°C – 0.7×10^6 cm^{-2} (e) (Fig. 1.14). The dependence of the density of Ge islands on growth temperature is shown on Fig. 1.15. At 590°C growth temperature Ge islands grow more and the length and the width of islands are - 5 μm and 1 μm, respectively. In the case of further growth of Ge coverage the sizes of islands grow, without essentially changing the density of the islands. This means that crystallization stage is over and further grown Ge is diffused to the island.

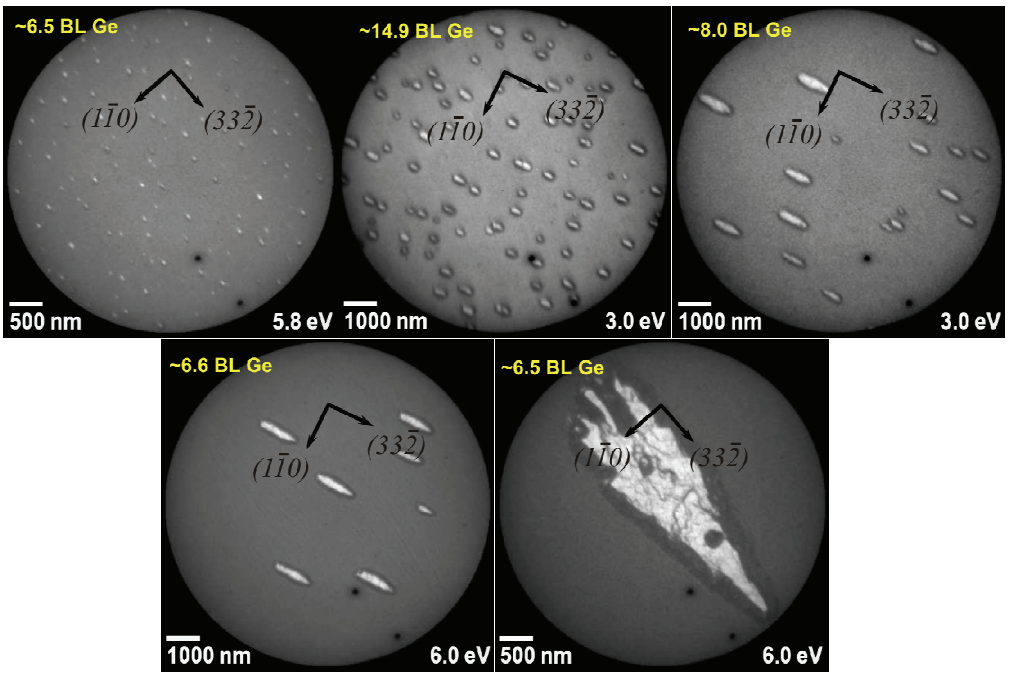

Fig. 1.14. The LEEM patterns of the Ge/Si(113) interface at different substrate temperatures (1 - 380°C; 2 - 440°C; 3 - 490°C; 4 - 540°C; 5 - 590°C), thicknesses of Ge layers (1 – 6.5 bi-layer, 2 – 14.9 monolayer, 3 - 8 monolayer, 4 – 6.6 monolayer, 5 – 6.5 monolayer), electron energies (eV) 1 – 5.8; 2 and 3 – 3.0; 4 and 5 – 6.0, scanning areas of sample (μm^2), 1 - 4 – 12.4; 5 – 6.2 [46].

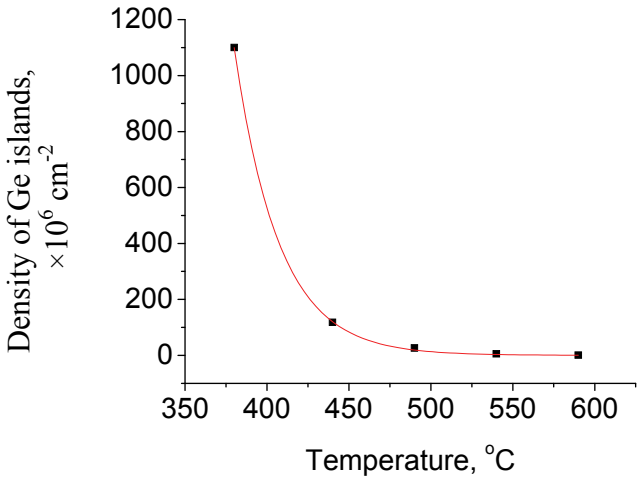

Fig. 1.15. The dependence of the density of Ge islands on the growth temperature.

That is, results of LEEM investigations (Figs. 1.14 and 1.15) coincide with the STM results (Fig. 1.12) and the sizes of islands change depending on the growth temperature: the length and width increase, while the height and density decrease. Thus, STM, LEED and LEEM systemized investigations of initial stage, shape and behavior of Ge crystallization on the Si(113) surface in the case of the sublayer (in the case of a small amount of Ge - 2-30 min) and multilayer (in the case of a great amount of Ge - 6,5-15 monolayers) growth of Ge on the Si(113) clean surface at high temperature sphere of the Si(113) substrate (300–600^{o}C) in the presence and absence of surfactants showed that the growth takes place in the shape of nano-islands. Their sizes depend on the growth temperature. At low growth temperatures (300–400^{o}C) Ge crystallization takes place in small round islands and at high temperatures (440–590^{o}C) the islands stretch, oriented to the crystal direction, the height decreases and the density increases. Thus, it becomes possible to grow smooth and high quality Ge thin films on Si by STM at optimum growth conditions (at 600^{o}C growth temperature of substrate and in the presence of Bi and Sb surfactants). Besides, it was shown that the surfactant favours the change of growth mode and growth by islands is substituted by layer-by-layer growth, as a result of which smooth thin layers are grown on the Si(113) substrate. The mode and behavior of sublayer and mulilayer growth coincide. The surface reconstruction of the partial or the sublayer Ge coverage on Si is (3×2)+(2×2), and in the case of full or multilayer coverage - 2×2.

1.2.2. CRACK FORMATION PROCESS DURING EPITAXIAL GROWTH

In recent years interest has arisen towards monolithic integration of optoelectronic devices based on Si substrate, especially solar cells on the silicon substrates with high crystallographic indices. The aim of the latter is to find ways, which would increase the efficiency of solar cells and decrease the cost. One such way is substitution of a valuable substrate with a cheaper and

lighter one (e.g., Si). Development of such technology can be used in the devices operating on the Earth as well as in space [50].

GaAs and Si are lattice mismatched (the difference between lattice constants is ~ 4%). Besides, Ge growth on the Si substrate at room temperature takes place in the shape of a decreasing monolayer steps and at high temperatures - in the shape of decreasing bi-layer steps. As a result, there is some difficulty concerning the growth process of GaAs thin layer on the surface of Ge/Si heterostructure, as antiphase domain is formed. Formation of the latter is the reason for the formation of surface defects and micro-cracks, which in its turn hinders fabrication of high-quality and efficient devices.

In this section the process of heteroepitaxial growth of heterostructures based on GaAs ($In_xGa_{1-x}As$ and $GaAs/In_xGa_{1-x}As$) on Ge/Si heterostructures has been investigated. $In_xGa_{1-x}As$ and GaAs thin layers and then multilayer GaAs structures have been epitaxially grown on Ge/Si(113) heterostructures by the LEPECVD and surfactant mediated epitaxy methods. Because of the presence of mechanical and thermal strain, antiphase domain and decreasing monosteps during the growth of the $In_xGa_{1-x}As$ layer on Ge/Si heterostructures are formed. Two ways of reducing the density of defects in the interface and micro-cracks on the surface have been suggested:

a) applying a bent substrate and then depositing a buffer layer to the bent substrate, and
b) applying a bent substrate and then depositing a buffer super-lattice to the bent substrate.

APPLYING THE BENT SUBSTRATE. A fundamental problem for the preparation of high quality A^3B^5 semiconductors on surfaces like Ge and Si is antiphase domain formation. The surface of Ge(100), like that of Si, is structurally characterized by dimer-reconstructed terraces separated by monolayer steps. The nature of the surface steps directly affects the quality of the GaAs buffer layer, which serves as a seed for the overgrowth of the cap layer. A common method for minimization of the densities of defects and microcracks is bent substrate. By saying a bent substrate we understand the substrate, which is cut at some angle ($1\text{-}6^o$) to the crystal direction of the semiconductor crystal planes ((110), (111), etc.). We use Si(113), as well as Si wafers, which are miscut by 6° away from the normal (001) surface towards [110]. At high annealing temperatures the surface develops a surface structure with bi-layer steps, which is aligned to the crystalline plane of the substrate. As those crystallites grow and merge into a larger crystal, they will be more likely to have matched crystallographic orientation by having started with a common orientation defined by the high quality surface. The tilted surface does appear to have caused a significant reduction in defect density.

STM and LEED investigations showed that the application of the bent substrate makes it possible to control the arrangement of neighboring atoms of the interface in the atomic scale and hence eliminate the antiphase domain, reduce the density of defects and surface microcracks and obtain a high quality and smooth GaAs thin layers on the Ge/Si heterostructure via $In_xGa_{1-x}As$ buffer layers.

APPLYING THE BENT SUBSTRATE AND THEN DEPOSITING A BUFFER LAYER ONTO THE BENT SUBSTRATE: In the case of depositing a compound semiconductor buffer layer onto the bent substrate, it is very important to determine the optimum concentration of components and optimum thickness of the buffer layer, which allow to grow structures with less amount of the micro-cracks and thermal strain and fabricate monolithically integrated efficient solar cells. The surface of heterostructure and the crack formation process during epitaxial growth were investigated by optical microscope with and without Nomarski contrast. The thickness of heterostructure layers is measured by Mirau Interferometer. The influence of the amount of indium and thickness of buffer layer on the crack formation process are investigated.

At first the influence of the concentration of components in the compound buffer epilayer on the formation process of surface micro-cracks of heterostructures are determined. For that purpose five $In_xGa_{1-x}As/Ge/Si$ heterostructures have been epitaxially grown, where the x concentration of indium is different and admits of the following values: 0.096: 0.068: 0.048: 0.036 and 0.024 (Fig. 1.16).

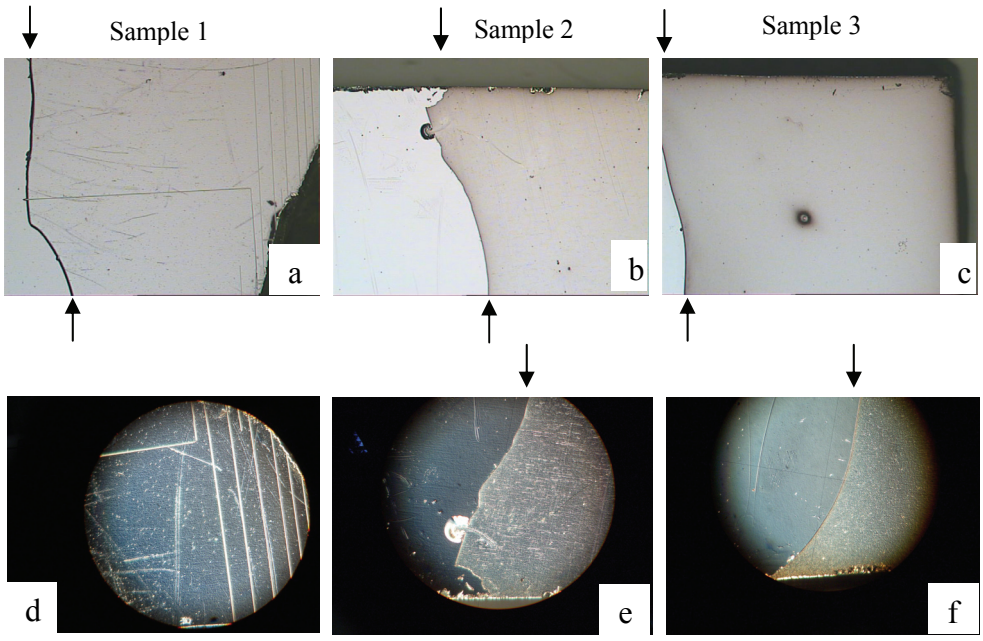

Fig. 1.16. Optical microscope images of $In_xGa_{1-x}As$ heterostructures (500 μm × 380 μm) in absence (a, b and c) and presence (d, e and f) of Nomarski contrast. Arrows show the borders of chemical etching.

The thickness of the Si substrate is 525 μm, and those of buffer layers of Ge and $In_xGa_{1-x}As$ are 1 μm and 3,5 μm, respectively. To control the x composition of indium in the heterostructures after hetero-epitaxial growth the photoluminescence spectra of the heterostructures have been measured at 15 K, using an excitation density of about 7 W/cm^2. Indium x concentration in the heterostructures are determined from maximum energetic values of photoluminescence spectra of $In_xGa_{1-x}As$/Ge/Si heterostructures: 9.6; 6.8; 4.8; 3.6 and 2.4 %. This result coincides with the above-mentioned growth values and the results obtained by X-ray diffraction [50]. Making sure that the indium concentration values obtained by different methods are exact, surface micro-cracks of heterostructures have been investigated. As the surface micro-cracks of the heterostructures aren't seen with an unaided eye, the above-mentioned heterostructures have been chemically etched in order to investigate their surface. For comparison one part of the surface of heterostructures was covered with photoresist and the other - wasn't. Photo-resist prevents etching of the part of heterostructures covered with photo-resist. As a result, the presence of micro-cracks in etched (the depth is 3 μm) and non-etched areas of the samples can be compared (Fig. 1.16).

Investigations of the deposition of the buffer layer on the bent substrate show that the majority of heterostructures have micro-cracks [51] and surface strain [52], which affect the efficiency of semiconductor heterostructures devices being elaborated. The surface micro-cracks are evident on the etched part of the heterostructures, which isn't observed on the non-etched part (Fig. 1.16). Information on the density of surface micro-cracks on the indium concentration and thickness of $In_{0.048}Ga_{0,952}As$ buffer layer in five epitaxial heterostructures is shown in Fig. 1.17.

High-quality $In_xGa_{1-x}As$/Ge/Si and GaAs/$In_xGa_{1-x}As$/Ge/Si heterostructures are formed in case of optimum 4.8 % concentration of indium (Fig. 1.17 a). Besides, calculations showed that parallel to the decrease in indium concentration in the heterostructures (9.6 – 2.4 %) thermal strain decreases from 1.5×10^{-3} to 2.6×10^{-6}. That is, there has been chosen such an optimum concentration of the changeable elements of compound buffer epilayer (4.8 %), in which case the density of thermal strain of the surface micro-cracks are minimal. The thickness of $In_{0.048}Ga_{0.952}As$ buffer layer changes from 0.5 μm to 3.5 μm, and the total thickness of GaAs and $In_{0.048}Ga_{0.952}As$ layers is 3.5 μm. When the thickness of $In_{0.048}Ga_{0.952}As$ layer changes from 0.5 μm to 3.5 μm the minimum density of surface micro-cracks is formed in the case of 1 μm epilayer thickness (Fig. 1.17 b).

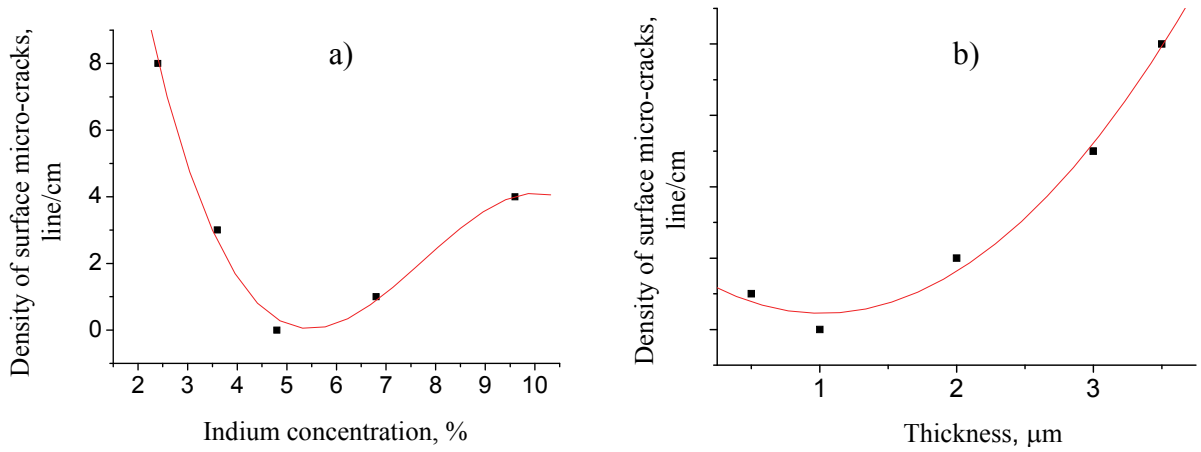

Fig. 1.17. Dependence of the density of surface micro-cracks on indium concentration (a) and thickness (b) of $In_xGa_{1-x}As$ buffer layer

After that GaAs top epilayer with thickness of 10 nm is grown on the structure. Our results, the reciprocal map (Fig. 1.18) and the RHEED images (Fig. 1.19) testify to the high quality of GaAs top epilayer. Reciprocal map shows that Ge buffer layer and GaAs are nearly fully relaxed. The FWHM of the GaAs peak is about 3 times greater than the Si peak one. The RHEED images, obtained at [110] direction (perpendicular atomic steps) show that the surface has the 2×2 reconstruction, at [110] direction (parallel to atomic steps) - 2×4 reconstruction (like As reconstructed surface). It is clearly seen that, the antiphase domain is missing in the GaAs epilayer and the GaAs monolayer has 2×4 reconstruction. That is, high-quality GaAs/$In_xGa_{1-x}As$/Ge/Si heterostructures with high mobility and different concentrations have been obtained.

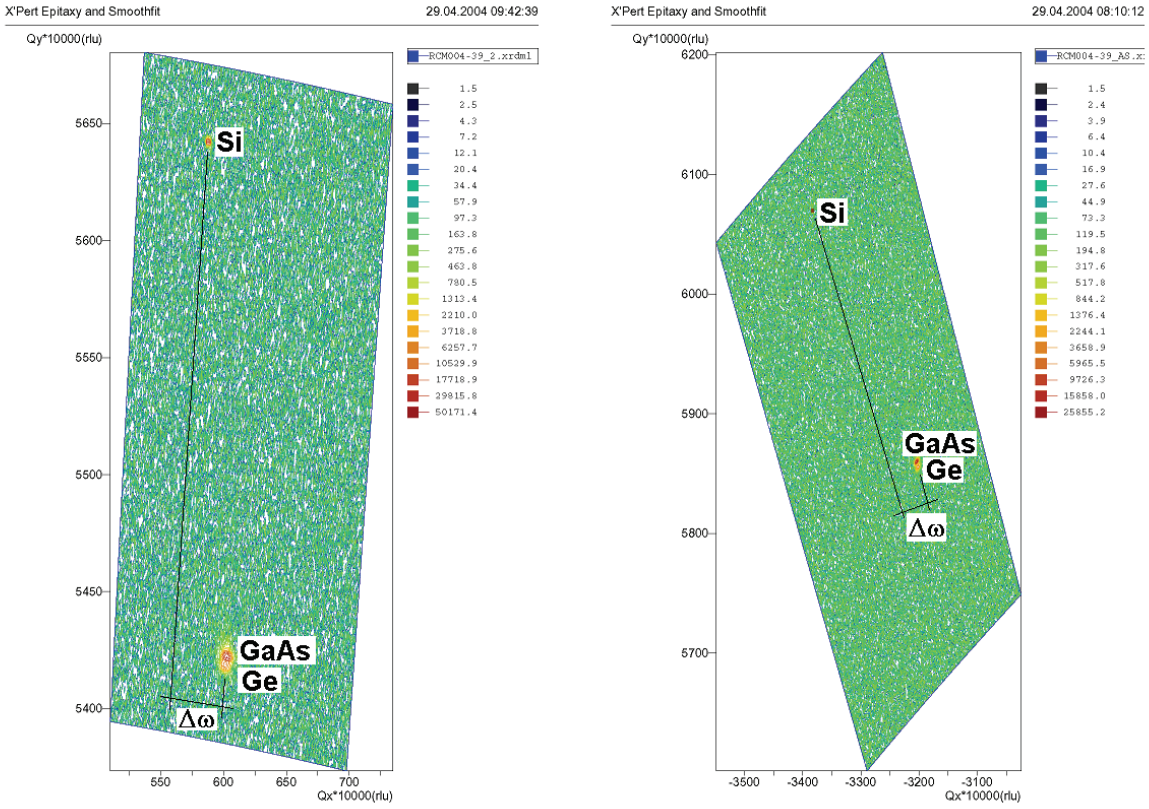

Fig. 1.18. The reciprocal space map of the heterostructure GaAs/ $In_xGa_{1-x}As$/Ge/Si(001)-6^0 off towards [110] direction near 004 and 224 reflections. Δω is the tilt between crystal planes of the substrate and epilayers resulting from the miscut of the substrate

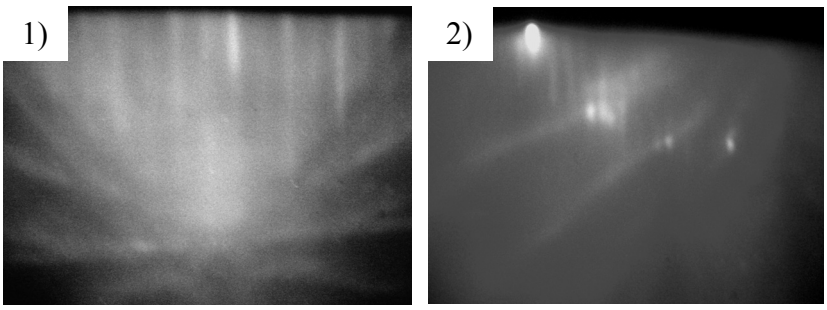

Fig. 1.19. The RHEED images of GaAs/$In_xGa_{1-x}As$/Ge/Si heterostructure at different crystallographic directions; 1 - [110] and 2 - $[\bar{1}10]$

APPLYING THE BENT SUBSTRATE AND THEN DEPOSITING A BUFFER SUPPERLATTICE TO THE BENT SUBSTRATE. The influence of the buffer super-lattice on surface micro-cracks of the heterostructure have been investigated. For that purpose GaAs|$In_xGa_{1-x}As$ superlattices with 10 and 20 period (e.g., 10×GaAs|$In_xGa_{1-x}As$/Ge/Si) and thicknesses of 550 nm have been monolithically integrated on the Si substrate through Ge buffer layer. GaAs nanolayer has thickness of 25 nm (5 nm), and $In_xGa_{1-x}As$ nanolayer - 30 nm (5 nm)

in the GaAs|$In_xGa_{1-x}As$ super-lattice with 10 (20) period. Investigations show that the buffer superlattice also favours the decrease of the surface micro-cracks in the heterostructures and as its result the elaboration of high quality heterostructure devices.

Thus, under optimum conditions (4.8% composition of indium and 1 μm thickness of $In_{0.048}Ga_{0.952}As$ buffer layer) it is possible to monolithically integrate high-quality structures based on GaAs on Si substrate with high crystallographic indices by MBE method.

1.3. FABRICATION OF THE MONOLITHICALLY INTEGRATED SOLAR CELLS

1.3.1. PROCESSING OF A^3B^5 SEMICONDUCTOR HETEROSTRUCTURES ONTO THE SOLAR CELLS

p^+-n-n^+ GaAs structures have been monolithically integrated on Si substrates through buffer layers. These structures have been processed into the solar cells. Standard photolithography (photoresist coating, exposure under appropriate solar mask and development), wet-chemical mesa etching and metallization were used to fabricate round mesa structures with 3, 5 and 10 mm diameter. For the fabrication of p^+-GaAs/n-GaAs/n^+-GaAs/$In_xGa_{1-x}As$/Ge/Si structures for the solar cells are heated in the plate, which has 100°C temperature, after which the heterostructures is covered with photo-resist coverage to obtain an etched structure and then it is heated at 100°C temperature for 1.5 min (Fig. 1.20). The structure covered with photo-resist is placed under the sun mask, is illuminated for 1.5 minutes, is dried by a rotating drier and is heated to 100°C for 11 minutes. Then for 7 minutes the structure is etched in H_2SO_4:H_2O_2:H_2O = 2:2:25 liquid. The thickness of etched layers is measured by the Mirau interferometer. p^+-GaAs/n-GaAs/n^+-GaAs solar cells with 3, 5 and 10 mm diameter (p^+-GaAs/n-GaAs/n^+-GaAs/$In_xGa_{1-x}As$/Ge/Si have been monolithically integrated by MBE method. The etched structure of solar cell with 10 mm diameter is shown in Fig. 1.21. p^+-GaAs, n-GaAs and n^+-GaAs epilayers have 0.5 μm, 2.0 μm and 0.7 μm thicknesses, respectively. Ohmic contacts were formed by the methods described below.

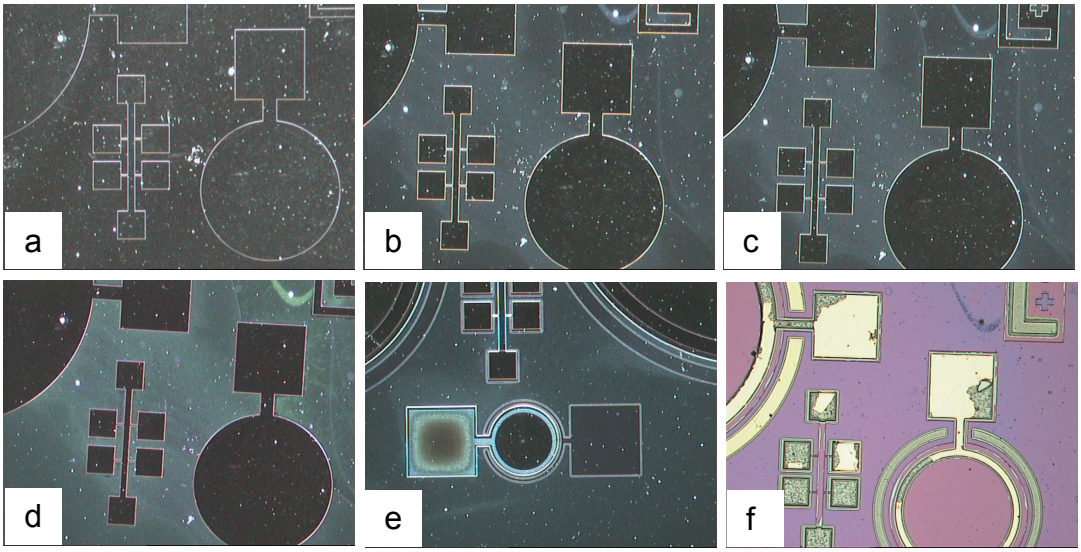

Fig. 1.20. Optical microscope images of photolithography steps of elaboration of the monolithically integrated p^+-GaAs/n-GaAs/n^+-GaAs solar cell on silicon substrate with high crystallographic index: a) photoesist deposition for mesa formation, b) development and removal of exposed photo-resist, c) mesa formation by etching, d) photoresist deposition for contact formation, e) development and removal of exposed photoresist, f) metal deposition.

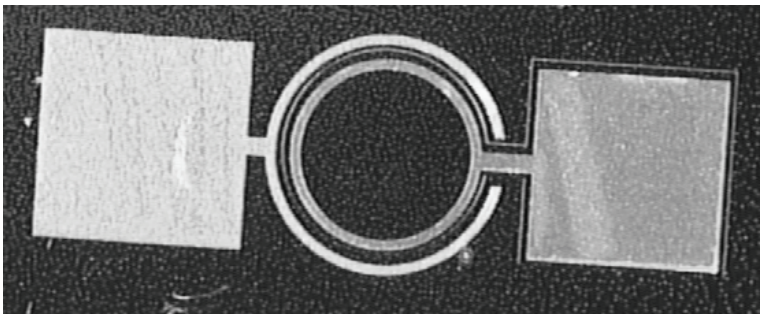

Fig. 1.21. Chemically etched structure of the monolithically integrated p^+-GaAs/n-GaAs/n^+-GaAs solar cell on silicon substrate with high crystallographic index, ohmic contacts of 1 - Ge and 2 - GaAs epilayers.

1.3.2. FORMATION OF FOUR NANOLAYER OHMIC CONTACTS

After monolithic integration of A^3B^5 heterostructures on silicon substrates the ohmic contacts are formed. It is known that the efficiency of devices based on GaAs (frequency region, noise level, gain, etc.) essentially depends on the properties (the structure and resistivity of the interface) on the ohmic contact-semiconductor system. Moreover, the influence of different factors on the properties of ohmic contacts based on GaAs has been widely investigated. Until now the formation problem of ohmic contacts (with small resistance, thermally stable and linear I-V characteristics) on GaAs top layer is not solved. The reasons for structural inhomogeneity and thermal decomposition of the ohmic contacts are the following:

1. the formation of inter-metal compounds with high resistivity (often unstable) in the interface,

2. the diffusion mixture of the contact materials in the interface, which expands transition layer and neutralizes the surrounding region of GaAs contact, and
3. the formation of mixture expanded regions in the metal-semiconductor interface (in the order of thickness of active layer).

1st and particularly 3rd reasons are possible to exclude, if as metal layer use high-temperature metal compounds. Therefore, the disadvantage of the metal systems is the fact that the anti-diffusion effects taking place in the interface of metal contacts deteriorate the thermal stability of contacts (1st and 2nd reasons). High-quality ohmic contacts should have anti-diffusion properties, small resistivity and be thermally stable. This matter becomes especially important in fabricating the ohmic contacts corresponding with the sizes of the nanostructured solar cell. While fabricating the ohmic contacts it is necessary to make an optimum choice of metal materials or metallic compounds and thicknesses of metal nanolayers promptly taking into account diffusion transport of charge carriers in the ohmic contacts and match of lattice constants of metals during thermal expansion. In order to obtain multilayer nanolayer ohmic contacts the following factors are important to take into account:

a) the thermal conductivity of materials of metallic compound,
b) the diffusion depth, which is determined by the choice of temperature of vacuum oven and duration of thermal treatment. The diffusion length depends on the thickness of epilayer.

The aim of this section is to obtain high-quality four-nanolayer ohmic contacts as well and to investigate their quality against thermal decomposition, i.e. thermal stability. For that reason thermally stable multilayer Au/Al/Ni/Sn contact structures are fabricated in electron beam evaporator, the base pressure of which is $2 \cdot 10^{-7}$ Torr, current ~100 mA, and the maximum diameter of the wafer ~10 cm. The growth rate of the metallic nanolayers is 0.1–0.5 nm/sec. The thickness of the nanolayer is measured by growth controller. For the growth of high-quality ohmic contacts the flow of electronic beam is chosen in such a way that it melt only a point (to avoid diffusion) and not the whole nanolayer.

To obtain four-nanolayer ohmic contacts metallic structure is heated at 500°C temperature during 30 minutes at vacuum condition. Metallic nanolayers are successively deposited on GaAs top layer of the surface of the etched structure of the solar cell, until thermally stable ohmic contact is formed. The latter consists of successively arranged nanolayers of Sn, Ni, Al and Au with thicknesses of 30 nm, 30 nm, 130 nm. and 30 nm, respectively. The ohmic contact' lowest Sn nanolayer contacts with GaAs top layer of the solar cell. After metallization unnecessary metallic areas of solar structure are removed. Fabricated four-layer ohmic contact structure is thermally elaborated in ultrasonic bath during 4 hours at 80°C temperature and then - in oxygen plasma (Fig. 1.21).

To investigate the thermal stability of elaborated ohmic contacts the latter are thermally treated for a short period of time at 400°C (5 min), 500°C (4 min) and 600°C (2.5 min) temperatures. The processes occurring during the formation and thermal decomposition of the contacts are analyzed by scanning electron microscopy (SEM). The stability control of the ohmic contacts shows that thermal treatment at optimum temperature of 500°C does not decompose the metallic layers of compound structure and does not form the micro-cracks, i.e. favours the formation of high-quality multilayer-structure ohmic contacts.

Thus, taking into account the diffusion transport of charge carriers and thermal conductivity of materials (lattice match of metals during thermal expansion) in the ohmic contacts, thermally stable four-layer ohmic contacts have been elaborated in the case of choosing optimum materials and the thickness of the contacts.

Optical microscope image of p^+-GaAs/n-GaAs/n^+-GaAs/$In_xGa_{1-x}As$/Ge/Si solar cell with ohmic contacts is shown in Fig. 1.22.

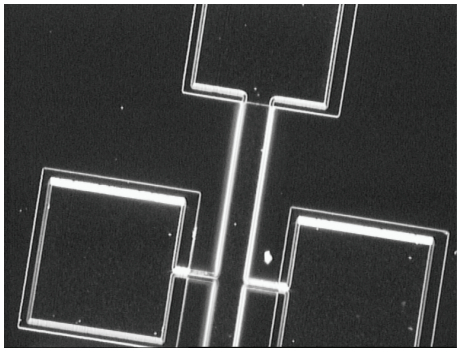

Fig. 1.22. Optical microscope image of p^+-GaAs/n-GaAs/n^+-GaAs solar cells monolithically integrated on silicon substrate with high crystallographic index after fabrication of ohmic contacts

1.3.3. ELECTRICAL CHARACTERIZATION OF THE GROWN HETEROSTRUCTURES

After formation of the ohmic contacts the structures were bonded by gold wire to the sample holders suitable for electrical and magneto-transport measurements at room and low temperatures, as well as for photoelectrical measurements. Measurements were done on rectangular samples. Electrical parameters of epitaxial heterostructures (mobility and conductivity of the majority charge carriers) have been measured by the method of Van der Pauw. For example, electronic mobility of GaAs epilayer (with doping concentration of 8×10^{14} cm^{-3}) in GaAs/$In_xGa_{1-x}As$/Ge/Si heterostructures is 2500 $cm^2/V\cdot sec$ at 77 K and 4500 $cm^2/V\cdot sec$ at 300 K. The I-V characteristics

of p^+-GaAs/n-GaAs/n^+-GaAs/$In_xGa_{1-x}As$/Ge/Si solar cells have been measured (Fig. 1.23) and their ideality factor has been calculated - 2.

Dark and photo current-voltage characteristics of p^+-n-n^+ diodes grown on silicon substrate are shown in Fig. 1.23.

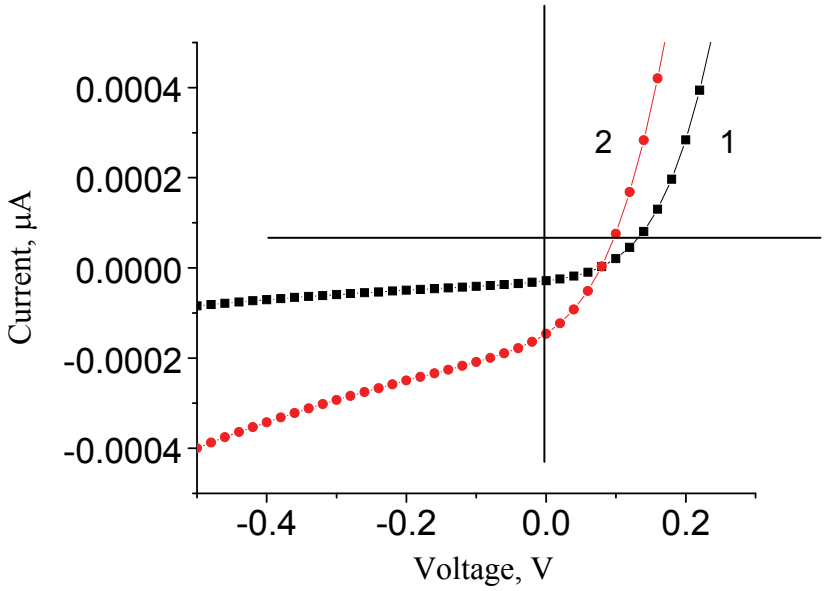

Fig. 1.23. I-V curves of two samples of the monolithically integrated p^+-GaAs/n-GaAs/n^+-GaAs solar cells on silicon substrate with high crystallographic index.

The mobility of charge carriers, the density of surface micro-cracks and the shape of I-V curve confirm the high quality of monolithically integrated solar cells.

CONCLUSION

By controlling the defects in the interface and the microcracks on the surface of the grown heterostructures formed from lattice mismatched semiconductor materials we succeeded in the fabrication of the monolithically integrated p^+-GaAs/n-GaAs/n^+-GaAs solar cells on silicon substrate with high crystallographic index at optimum growth method and conditions. Though they are less efficient than those of A^3B^5 compounds, are cheaper, have great mechanical hardness and big surface, due to the Si substrate. Since investigations of the monolithic integration of solar cells elaborated on the basis of GaAs by Ge and $In_xGa_{1-x}As$ buffer layers on silicon substrate with high crystallographic index are in the initial stage in the world, the obtained results are promising.

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