

**INCREASE IN THERMAL RELIABILITY OF INTEGRATED CIRCUITS
AT THE STAGE OF PLACEMENT OF CELLS**

A.G. Harutyunyan and A.H. Kajoyan

State Engineering University of Armenia, Yerevan, E-mail: harsh@seua.am

Keywords: Semiconductor, crystal, IC cells, refusal

1. Introduction

Now and (under forecasts) till 2012, even at use of cases with the newest heat-removing properties, operating temperatures of a semiconductor crystal of integrated circuits (IC) can reach above 100°C, and differences of temperatures between various zones of a crystal - above 10-20°C [1].

Results of accelerated tests of ICs of average complexity have shown that if their average service life at temperature 600C makes 50-75 years, at temperature 1250C - no more than 1000-1500 hours [2].

Hence, at designing IC, alongside with traditional methods of reducing the operating temperature by application of radiators and fans, the development of new methods becomes urgent. One of the ways of solving this problem can become the reduction of a difference of temperatures between various zones of a crystal at placement of IC cells. It will lead to reduction of temperatures of the hottest zones of a crystal which are the most dangerous from the viewpoint of thermal reliability.

2. Theory

For the period of normal functioning of IC, accepting the exponential law of distribution of refusals and independence of refusals of elements, a condition of providing maximal reliability of IC has the following form [3]:

$$P(t, T) = \exp \left[-t \sum_{i=1}^N \lambda_i(T_i) \right] \rightarrow \max, \quad (1)$$

where $P(t, T)$ is the probability of non-failure operation of IC depending on time t and temperatures T ; $\lambda_i(T_i)$ is the failure rate of the i -th element at temperature T_i ; N is the quantity of considered elements of IC.

As is known, dependence of the average time of non-failure operation of IC elements on temperature $t_{av}(T)$ is characterized by the Blech dependence having an exponential form [4]:

$$t_{av}(T) = AJ^{-n} \exp(E / kT), \quad (2)$$

where A is a parameter depending on technology (microstructure); J is the current density; n is the level pointer of the density of current, accepting values $n=1.0 \div 2.0$, at changing density of current within the limits of $J = (0.2 \div 2.0) \times 10^6$ A/cm²; E is the energy of activation depending on applied materials and for semiconductor IC with aluminum interconnections accepting the value $E=0.5 \div 0.6$ eV; k is the Boltzmann constant; T is the temperature of IC element in K.

As in condition (1) probability of non-failure operation $P(t, T)$ is a monotonously decreasing function of $\sum_{i=1}^N \lambda_i(T_i)$, and as considered that the failure rate $\lambda(T)$ is the inverse quantity of the average time of non-failure operation $t_{av}(T)$, the condition of maximal reliability depending on temperature with consideration of (2), it is possible to present as follows:

$$\sum_{i=1}^N \lambda_i(T_i) = \sum_{i=1}^N [t_{avi}(T_i)]^{-1} = \sum_{i=1}^N \left[t_{avi} (A_i J_i^{-n})^{-1} \exp((k / E) T_i) \right] \rightarrow \min. \quad (3)$$

Within the limits of one IC the parameters entered in (3), except temperature T , it is possible to accept elements approximately equal for all. With the purpose of giving view to condition (3), convenient for application in a problem of placing IC elements, presenting exhibitor of expression as a level row and making some transformations, it is possible to obtain the following condition:

$$\sum_{i=1}^N \left| \sum_{\substack{j=1 \\ j \neq i}}^N (T_i - T_j) \right| \rightarrow \min. \quad (4)$$

As at the stage of placing IC elements, temperatures and capacities of elements are known, then, with the purpose of reducing condition (4) to a view convenient as a criterion of placement, some transformations are made.

Assume that capacities of IC elements, coefficients of heat conductivity of separate parts of IC crystal and coefficients of heat exchange do not depend on temperature. Then, on the basis of the principle of superposition, the stationary temperature of some i -th element is defined proceeding from the mutual thermal influence of all elements [5]:

$$T_i = T_e + \sum_{k=1}^N P_k F_{ki}, \quad (5)$$

where T_e is the temperature of an environment; P_k is the power of k -th element; F_{ki} is the thermal coefficient between k -th and i -th positions.

For IC with a high degree of integration and with large regularity of the structure consisting of elementary cells of approximately identical sizes, it is possible to accept equality of values of thermal coefficients of all landing places of elements. Considering that values of the sums $\sum_{\substack{k=1 \\ k \neq i,j}}^N P_k F_{ki}$ and $\sum_{\substack{k=1 \\ k \neq i,j}}^N P_k F_{kj}$ depend on a relative positioning of i -th and j -th elements as well as the fact that $F_{i,j}$ is a decreasing function of geometrical distance of i -th and j -th elements $d_{i,j}$, in view of (4), as a criterion of placement considering homogeneous topological distribution of temperature on IC crystal, it is possible to obtain the following expression:

$$f_T = \sum_{i=1}^N \left| \sum_{\substack{j=1 \\ j \neq i}}^N (P_i - P_j) d_{i,j} \right| \rightarrow \min. \quad (6)$$

From the mathematical point of view, from a minimum of expression (6) the minimum of

expression $\left| \sum_{\substack{j=1 \\ j \neq i}}^N (P_i - P_j) d_{ij} \right|$ for $i=1,2,\dots,N$, that in its turn means achieving equality of two

sums $\left| \sum_{\substack{j \in E_1 \\ i \neq j}} (P_i - P_j) d_{ij} + \sum_{\substack{j \in E_2 \\ i \neq j}} (P_i - P_j) d_{ij} \right|$, where the first sum corresponds to elements, the power

of which is more than the power of i -th element, and the second sum corresponds to those elements, the power of which is less than the power of i -th element. If we consider the

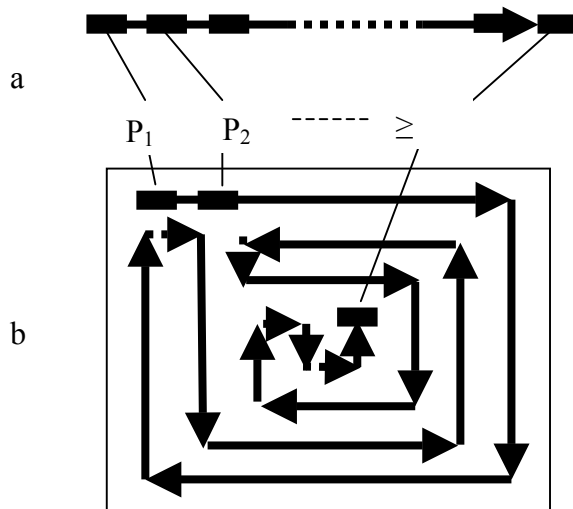


Fig. 1. A principle of placing elements.
a) linear placement;
b) packing of linear placement on a crystal.

requirements of maximal density of placing IC elements alongside with achieving equality of two sums, the condition of minimum of each of these sums follows. From the mathematical viewpoint, the minimum of each of these sums is reached when components $(P_i - P_j)$ and d_{ij} for the first sum and $(P_j - P_i)$ and d_{ij} for the second sum on the values are ranged in the opposite order.

The obtained condition (6), from the viewpoint of the designer, means that elements with great values of absolute differences of powers should be placed whenever possible more close and, on the contrary, that will lead to equalizing of a thermal field of a semiconductor crystal - to that lowering temperature of the most dangerous (from the point of view of reliability) zones.

With the use of condition (6), the elementary algorithm of consecutive placement based on the linear ranking of placed topological cells on decrease of their powers, with the further packing a line in square-law topology under the scheme resulted in Fig. 1 is realized.

The imitating model of topological distribution of powers and temperatures has been developed, in which dark colors correspond to higher powers and temperatures and on the contrary.

In Fig. 2 an example of computer modeling of a thermal field of a crystal on an example of test circuit ISCAS85 c499 is shown.

Results of modeling of a thermal field of some test circuits have shown that the proposed approach of initial placement of IC cells, in comparison with casual placement, provides the increase in homogeneity of a thermal field more than 50%, and differences of temperatures between various zones of a crystal do not exceed 80°C.

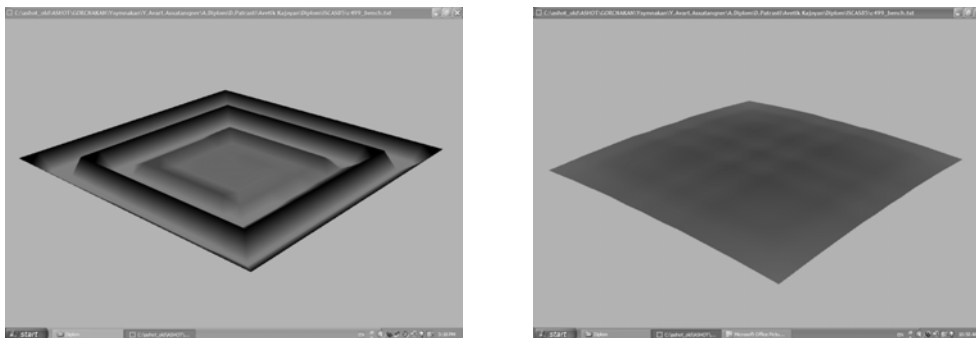


Fig. 2. An example of computer modeling of a thermal field of a crystal on an example of test circuit ISCAS85 c499. Distribution of powers of logic cells; topological distribution of a thermal field

3. Conclusions

Criteria and the corresponding approach for initial placement of IC cells, providing topological homogeneity of a thermal field and increase in thermal reliability are proposed. The developed imitating model of topological distribution of powers and temperatures, allows replacing of expensive physical methods of research of thermal field of IC by much more convenient computer methods.

Comparative results of variants of placing some test circuits have shown appreciable improvement of homogeneity of a thermal field of IC crystal and, hence, appreciable increase in the thermal reliability of IC.

REFERENCES

1. Ching-Han Tsai and Sung-Mo Kang. IEEE Transactions on Computer-Aided Design, v. 19, 253 (2000).
2. <http://www.ixbt.com/cpu/Pentium4-athlonxp-thermal-managment.shtml>.
3. Mikroelektronika: Ed. L.A. Koledova, no. 4, I.Ya. Kozir'. Kachestvo i nadezhnost' integral'nikh mikroskhem. M.: Vishshaya. Shkola, 1987.
5. Vijay Reddy. International reliability physics symposium. Hyatt regency Dallas, Texas, topic 111, 1 (2003).
6. G.N. Dul'nev, E.M. Semyashkin. Teploobmen v radielektronnykh aparaturakh. Energiya, L., 1968.